3-4 Q

DATA BOOK

Linear IC

1986

HITACHI

LINEAR IC DATABOOK

■ GENERAL INFORMATION

■ DATA SHEETS

INDEX

GENERAL INFORMATION

- REFERENCE GUIDE
- PACKAGE INFORMATIONS
- RELIABILITY OF LINEAR ICs

REFERENCE GUIDE

Function			Type No.	Operating Temp. Range			Package Code					Page
				0 to +70°C	−20 to +75°C	−40 to +85°C	DG	DP	SP	MP	FP	
Operational Amp.	J-FET Input	Single	HA17080GS			■	8					26
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			HA17082PS		■			8				26
			HA17083G			■	14					26
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			HA17458	■				8				44
			HA17458GS		■		8	8				44
			HA17458PS		■			8				44
			HA17558	■				8				51
			HA17558GS		■		8					51
			HA17558PS		■			8				51
			HA17747	■				14				73
			HA17747G		■		14					73
			HA17747P		■			14				73
			HA17904GS			■	8					42
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	Quad.		HA17301G			■	14					32
			HA17301P		■			14				32
			HA17324	■				14				38
			HA17324G		■		14					38
			HA17324P					14				38
			HA17474	■				14				49
			HA17474G		■		14					49
			HA17474P		■			14				49
			HA17902	■				14				75
			HA17902G			■	14					75
			HA17902P		■			14				75
Voltage Comparator	Single		HA1813PS		■			8				90
	Universal		HA1812GS		■		8					98
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			HA17903PS		■			8				86
			HA1807		Note 1		14					90
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			HA17901G			■	14					82
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(to be continued)

(continued)

Function			Type No.	Operating Temp. Range			Package Code †					Page
				0 to +70°C	−20 to +75°C	−40 to +85°C	DG	DP	SP	MP	FP	
Voltage Regulator	Switching Regulator		HA16664FP		Note 2						14	106
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			HA17524G				16					114
			HA17524P					16				114
			HA1835P					14				151
	Precision		HA17723					14				120
			HA17723G				14					120
	1A	5V	HA17805						3			128
			HA17805P						3			128
		6V	HA17806						3			128
			HA17806P						3			128
		7V	HA17807						3			128
			HA17807P						3			128
		8V	HA17808						3			128
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		12V	HA17812						3			128
			HA17812P						3			128
		15V	HA17815						3			128
			HA17815P						3			128
		18V	HA17818						3			128
			HA17818P						3			128
		24V	HA17824						3			128
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	100mA	2.5V	HA178L02						3			141
			HA178L02P						3			141
		5V	HA178L05						3			141
			HA178L05P						3			141
		5.6V	HA178L56						3			141
			HA178L56P						3			141
		6V	HA178L06						3			141
			HA178L06P						3			141
		8V	HA178L08						3			141
			HA178L08P						3			141
		9V	HA178L09						3			141
			HA178L09P						3			141
		10V	HA178L10						3			141
			HA178L10P						3			141
		12V	HA178L12						3			141
			HA178L12P						3			141
		15V	HA178L15						3			141
			HA178L15P						3			141
	500mA	5V	HA178M05						3			147
			HA178M05P						3			147
		6V	HA178M06						3			147
			HA178M06P						3			147
		7V	HA178M07						3			147
			HA178M07P						3			147

Note) 1. −30 to +80°C 2. −20 to +85°C

(continued)

Function			Type No.	Operating Temp. Range			Package Code †					Page
				0 to +70°C	−20 to +75°C	−40 to +85°C	DG	DP	SP	MP	FP	
Voltage Regulator	500mA	8V	HA178M08						3			147
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		12V	HA178M12						3			147
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		15V	HA178M15						3			147
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			HA13432		Note 4			24				216
			HA13432MP		Note 4					28		216
			HA13440MP	Note 7						28		225
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			HA16632AP	Note 8				28				249
			HA16640NT					42				258

Notes) 3. −10 to +75°C 4. $T_{j(opr)}$ = −20 to +125°C 5. $T_{j(opr)}$ = −40 to +125°C 6. $T_{j(opr)}$ = −20 to +135°C 7. $T_{j(opr)}$ = 0 to +125°C 8. 0 to +60°C 9. −20 to +70°C

• : The chip product for sale •• : Side Brazed Ceramic DIP

(continued)

Function		Type No.	Operating Temp. Range			Package Code †					Page
			0~ +70°C	−20~ +75°C	−40~ +85°C	DG	DP	SP	MP	FP	
Micro-computer Peri-pheral	Floppy Disk Controller	HA16642MP	■						44		264
		HA16642NT	■				42				264
		HA16643MP	■								269
		HA16651MP	■						44		280
	Hard Disk Controller	HA16652P	■				22 / 28				283
		HA16652MP	■						28		283
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		HA16663MP	■						18		306
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		HA17592G		■		14					338
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		HA17733G		■		14					340
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	Precision Timer	HA17555	■				8				331
		HA17555GS		■		8					331
		HA17555PS		■			8				331
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		HA16619P		■			18				323
		HA16721MP	■						44		326
		HA16722MP	■						44		326

Notes) 10. −20 to +85°C

† : The package codes of DG, DP, SP, MP and FP are applied to the package materials as follows.
DG : Cerdip, DP : Plastic DIP, SP : Plastic SIP, MP : Plastic Mini-square package,
FP : Plastic Flat Package (SOP)

PACKAGE INFORMATIONS

HA 17741 P

- Package Code ; letters P : Plastic DIP
  - letters G : Cerdip
  - leters FP : Small Outline Package (SOP)
  - leters MP : Mini-square Package
- 17×××; Standard Linear IC
  - Circuit Description of 1 st Vendor's Name (Three Figures of Low Rank)
- Other Circuit Description ; Hitachi Original
- Prefix : HA ; Hitachi Linear (Analog) IC

DIMENSIONAL OUTLINE

● Plastic Dual-in-line Package

Unit: mm (inch), scale 1/1

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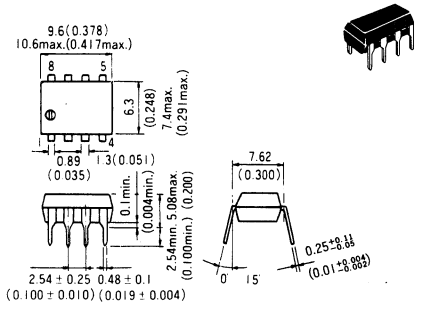

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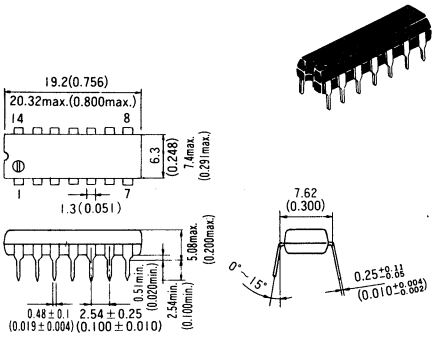

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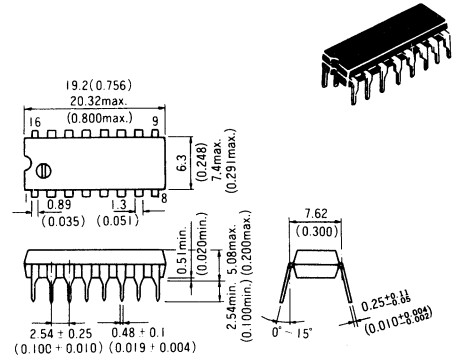

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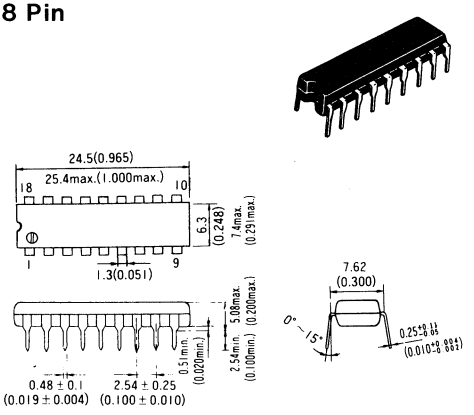

(DP-18A)

Unit: mm (inch), scale 1/1

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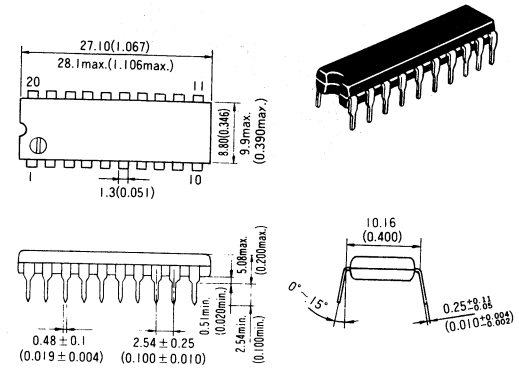

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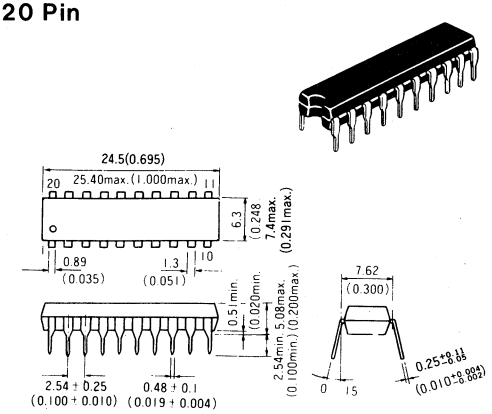

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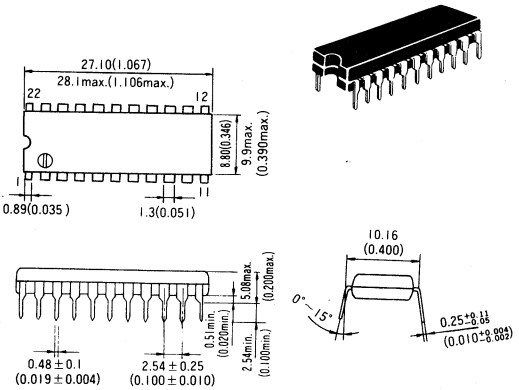

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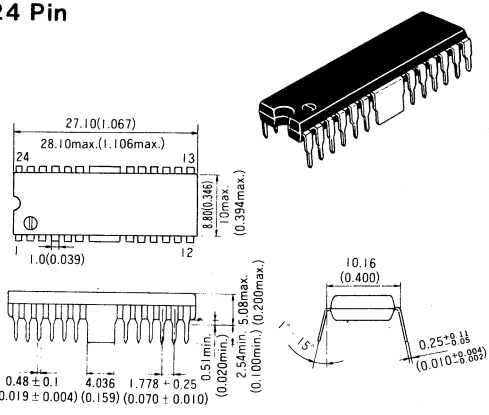

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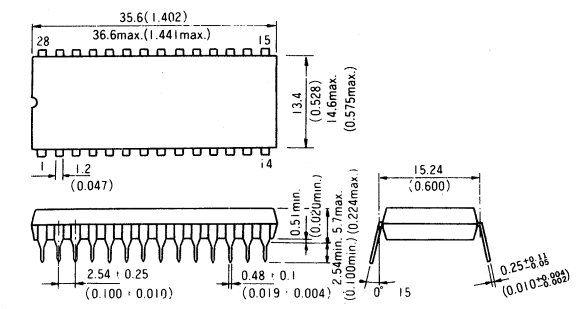

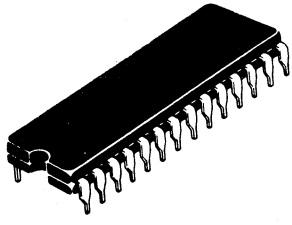

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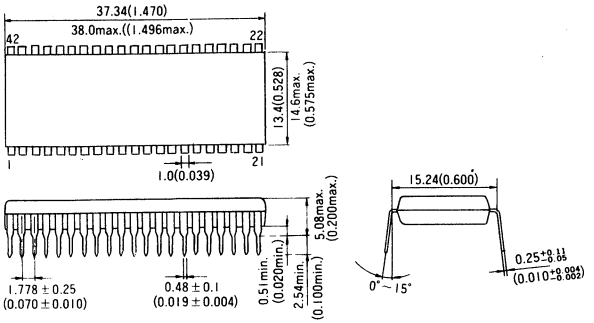

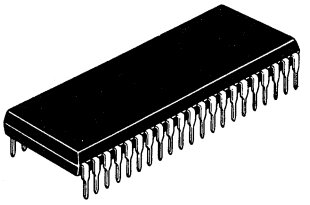

(DP-42SA)

■ **Cerdip**

Unit: mm (inch), scale: 1/1

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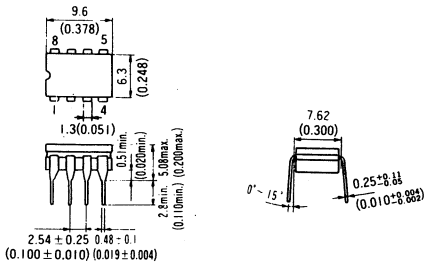

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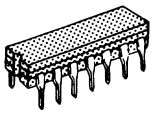

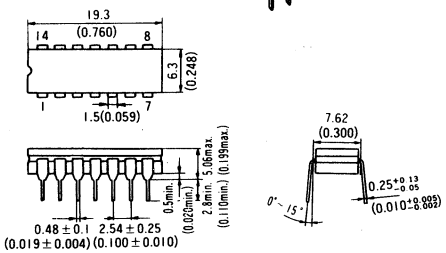

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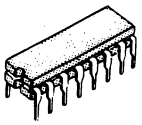

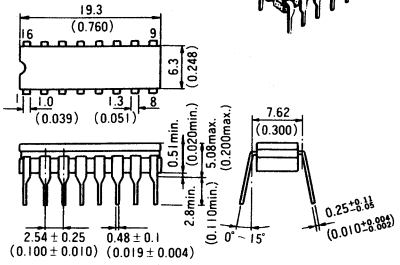

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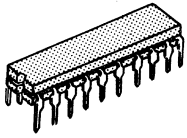

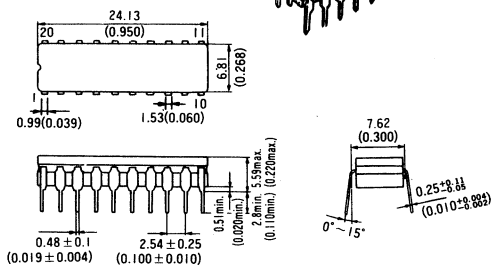

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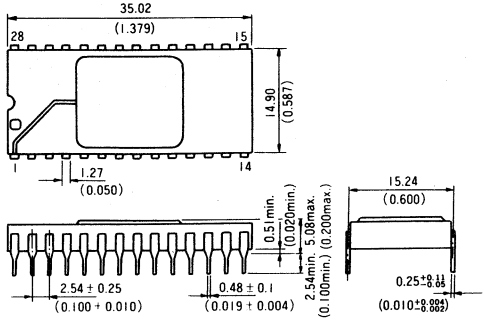
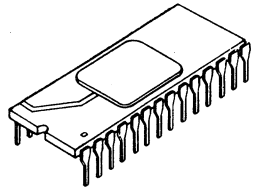


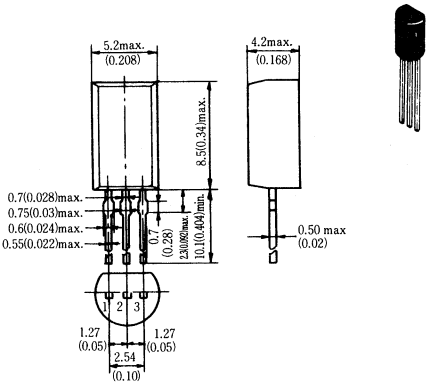


(DC-28)

■ **Plastic Single-in-line Package**

Unit mm (inch), scale: 1/1

3 Pin



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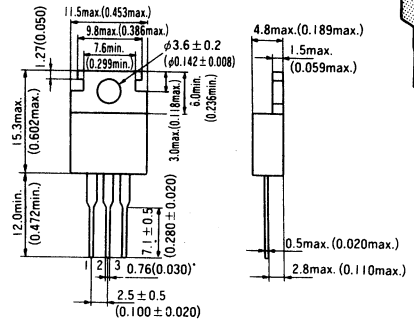

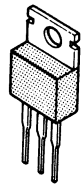

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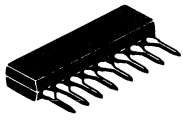

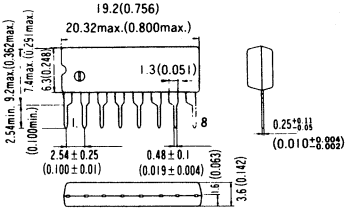

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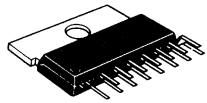

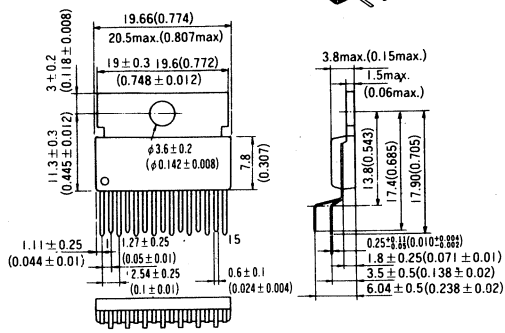

(SP-15TA)

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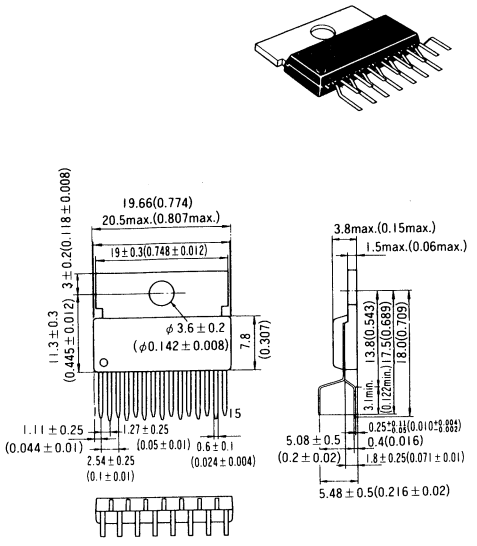

(SP-15TB)

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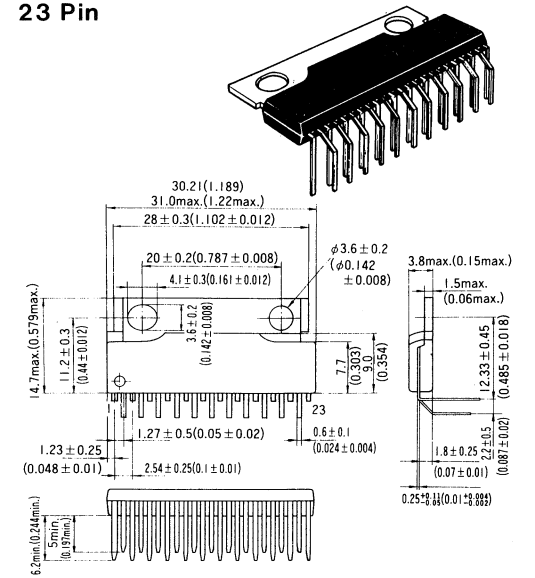

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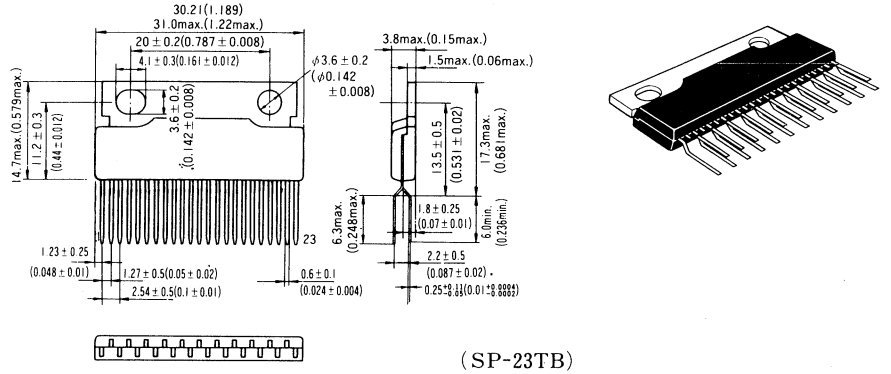
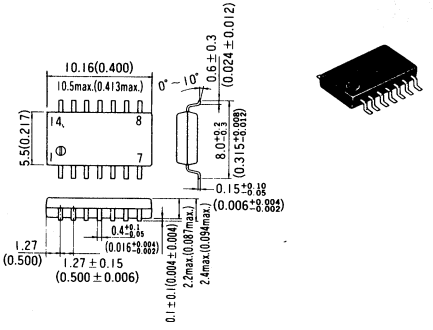


(SP-23TB)

■ **Plastic Flat Package**

Unit: mm (inch), scale: 1½

14 Pin

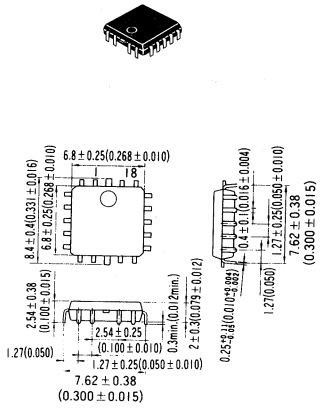


(FP-14D)

■ **Plastic Mini-square Package**

Unit: mm (inch), scale 1½

18 Pin



(MP-18)

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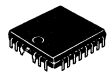
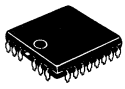


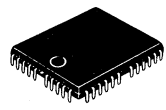
(MP-28T)

28 Pin



(MP-28)

44 Pin



(MP-44)

RELIABILITY OF LINEAR ICs

In the following we review the reliability of linear ICs. The introduction of this linear IC series marks a big step forward in reliability and meets the user's needs through their improvided reliability resulting from Hitachi's mass production technology and quality control.

1. CONCEPT OF QUALITY AND RELIABILITY

Hitachi's fundamental concept of product quality consists in meeting the requirements of individual users and maintaining a high quality of materials taking into consideration the marketability of the product from a broad and general aspect. The quality of product required by a user is determined according to the specifications listed in the agreement; however, there are occasions when it is not specified. In either case, out company makes every effort to ensure that the delivered semiconductor devices are able to display their full performance under the service environment in order to secure their reliability. Establishment of a quality control system in the process and enhanced quality comscopismess are keys to bringing about such reliable product quality in the manufacturing process. In the market of late, the user's requirements for quality of semiconductor devices have become steadily more stringent because the performance of electronic systems is rapidly improving and their scale and applications are widening. In order to cope with this trend, the following points have been adopted as the basic policy in Hitachi's actual operations.

(1) In the design stage of developing new products, full consideration is given to their reliability.
(2) The quality of product is made up at the each step of the manufacturing process.
(3) Inspection of finished products and confirmation of their reliability are to be intensified.
(4) Field data should be fully utilized to improve the quality of products.

Table 1 gives an example of the reliability programs drawn up to the meet the user's requirements. Moreover, we are making efforts to firmly establish higher quality and reliability of our semiconductor devices by pooling the efforts of our research and manufacturing departments. Based on the above concept and measures, our company is doing its utmost to meet the user's demand for product quality.

2. RELIABILITY OF SEMICONDUCTOR DEVICES

2.1 RELIABLITY TARGET

Reliability target is an important factor along with the function and price in the courses of manufacturing and selling products. It is not practical to classify the reliability target merely by the failure rate under a certain testing condition. Our company sets the reliability target by taking into account the design, manufacture, quality control in the process, screening, testing method, etc. with the contents corresponding to the characteristic nature of each item of equipment comprehensively considering the service envikonment of the equipment to which the device is applied, purpose design, operating, condition, maintenance, etc.

2.2 HOW TO CARRY FORWARD RELIABILITY DESIGN:

In order to achieve desired reliability based on the reliability target, timely examination and execution of such items as design standardization, device design (including process design and structural design), design review, reliability test are required beforehand.

(1) Standardization of design:

Establishment of design rule and standardization of parts, materials and processes are necessary. When establishing respective rules of design concerning circuit design, element design, layout design, critical items regarding the quality and reliability are always examined. Accordingly, where standardized processes or materials are used, even newly developed products can minimize risks affecting reliability unless special functional requests are made.

(2) Device design:

It is important to carry out device design taking into consideration the total balance between circuit, layout, process and structural designs. Particularly when using new processes and materials, technical examinations prior to development of the device are carried out to the full.

(3) Evaluation of reliability by TEG:

TEG (Test Element Group), sometimes called test pattern, is an effective method to evaluate the reliability of design and process of ICs and LSIs containing complicated functions. For transistors, it is useful to increase the sensitivity of detecting troubles caused when applying new processes. As to TEG, further expalanation is provided in the following.

1. Purpose of use of TEG;

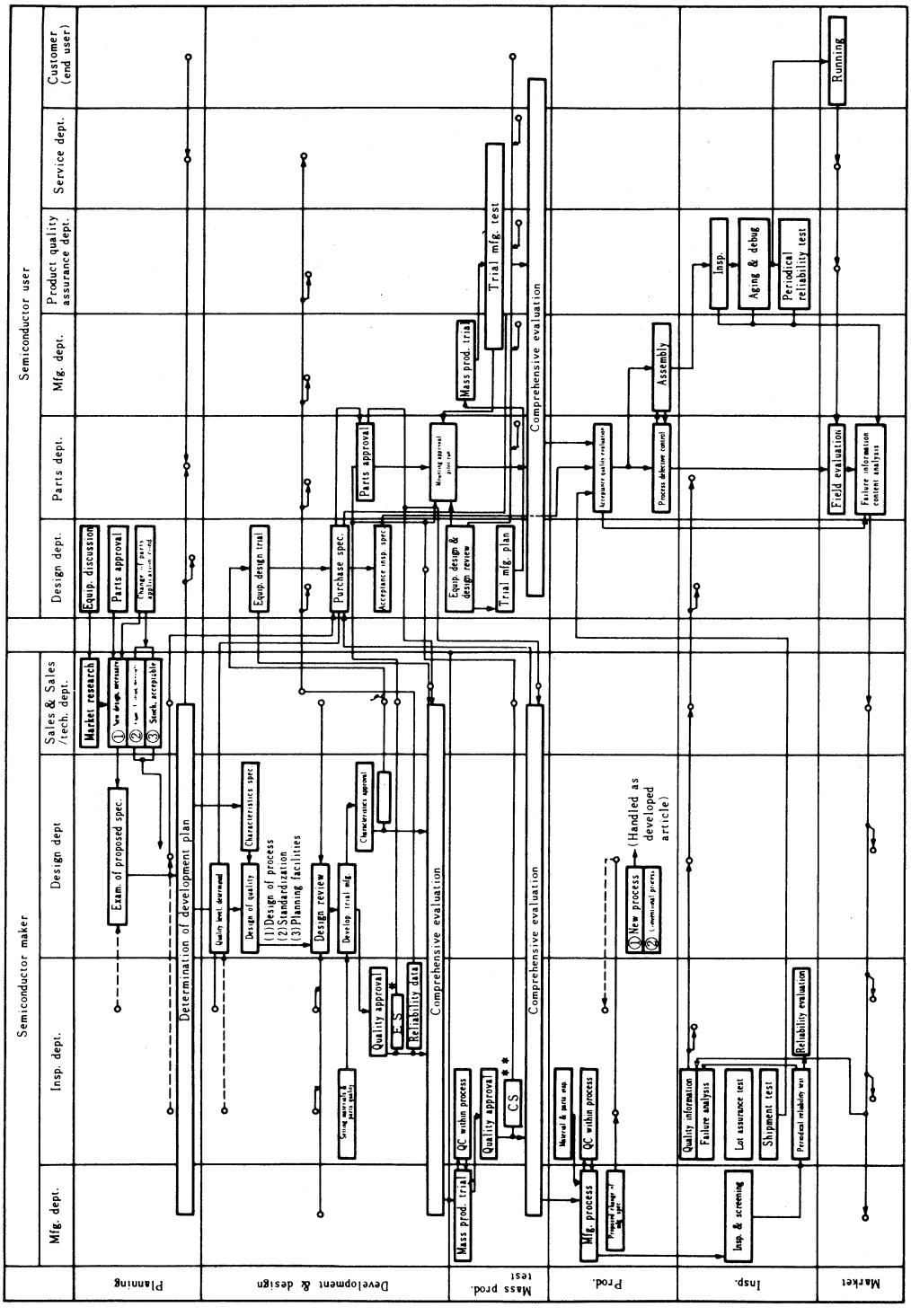
- Clarifying the basic failure mode.
- Grasping the relation between failure mode and manufacturing process condition.
- Obtaining a clue to analysis of failure mechanism to analyze the mechanism of failure.
- Establishing QC point for manufacture.

2. Effectiveness of evaluation by TEG;

- Possible to evaluate the basic failure mode and failure mechanism common to each type of products.
- Possible to compare the process having the failure with the process having records of marketabilily by clarifying the factors controlling the failure mode.
- Easy to grasp the connection between the cause of failure and that of the manufacturing process.
- Easy to perform test.

Here described several concrete examples of reliability evaluation by TEG.

Table.1 Example of Reliability Program



*Engineering Samole **Commercial Samole

Table.2 Standard for Design Review

		Hitachi Standard for Design Review	NASA Space System Standard for Design Review.
Purpose		Securing reliability required in the market.	Assurance of performance required by the program.
Definition		Systematical and organic confirmation and promotion of broad technical capacity.	Systematical and orderly application of broad technical capacity.
Item of review		Correction of defects in design.	Correction of defects in design.
Subject of review		Designated types of products.	Contracted projects.
Time		Concept Intermediate design Final design.	Preliminary Before mounting Before rejease of drawing.
Composition	Chairman	Collector of designs.	Designation of project manager.
	Member	Related responsible person and reliability technician.	Person in charge or higher rank, and reliability technician.
Authority		Recommendation of improvement.	Presentation of advice.

2.3 DESIGN REVIEW:

Design review is a procedure to systematically check whether the design satisfies the performance required by a user, the designing work is performed according to the specified form, and the items of technical improvement which have been obtained from the accumulated experimental field data in each specialized department are efficiently used. It is also performed mainly for ensuring the quality and reliability of the products in order to strengthen the competitive power of our products. In Hitachi, new products and design-changed products are subjected to design review from conceptional stage. This method is extensively used by NASA. Table 2 shows the comparison between the standards for design review of our company and NASA: The following are the contents of the review.

(1) Description of the contents of products according to the design document.
(2) The design document is reviewed from the standpoint of each specialist who participates in the review. If any unclear item is found, a sub-program for calculation, experiment or investigation is drawn up and executed.
(3) The contents or method of a reliability test is determined according to the design document and the contents of the drawing.
(4) Checking whether the process capacity of the manufacturing plant is sufficient to achieve the design goal.
(5) Conference for preparation of production.
(6) Planning and execution of a sub-program for test, or experiment, calculation, etc. for change and confirmation of the design proposed by each specialist.
(7) Referance to past failure examples of similar types of articles and confirmation of preventive measures against recurrence of such failures, and planning and execution of a testing program for confirmation.

Careful discussions for the above made at the design review are carried out according to the check list specially device and prepared according to each subject.

3. QUALITY ASSURANCE STRUCTURE OF SEMICONDUCTOR DEVICES:

3.1 ACTIVE OF QUALITY ASSURANCE:

The general concept of Hitachi's overall quality assurance is described below.

(1) The problems of each process are to be settled within the process concerned. Accordingly, in the stage of finally finished products, latent defective factors are eliminated.
(2) In order to maintain the process capacity at a goodlevel, feedback of information is performed.
(3) Quality assurance aims at securing the desired reliability obtained as a result of the above.

Device design, recognition of quality at the time of mass production, quality control with the process inspection of products and assurance test of reliability are described below.

3.2 QUALITY RECOGNITION:

In order to secure the desired quality and reliability, quality of products recognition is carried out at the time of design and trial; manufacture of devices and their mass production according to the reliability design. The concept for recognition of the quality of products is described below.

(1) Performing an objective recognition putting the company itself in its customer's place and by a third party.
(2) Taking into full consideration past failure examples and field information.
(3) Carrying out recognition of its quality, in case of change of design or operation.
(4) In the case of parts, materials and process, emphasis is placed on the recognition of their quality.
(5) The process capacity and causes of variations are examined, and the control points at the time of mass production are established.

Quality recognition is performed by incorporating the above concept.

3.3 QUALITY AND RELIABILITY CONTROL IN MASS PRODUCTION

For quality assurance of mass production, the quality control work is systematically and functionally assigned to the manufacturing and inspection departments including the related departments. The entire function is shown in the flow chart of Fig. 1.

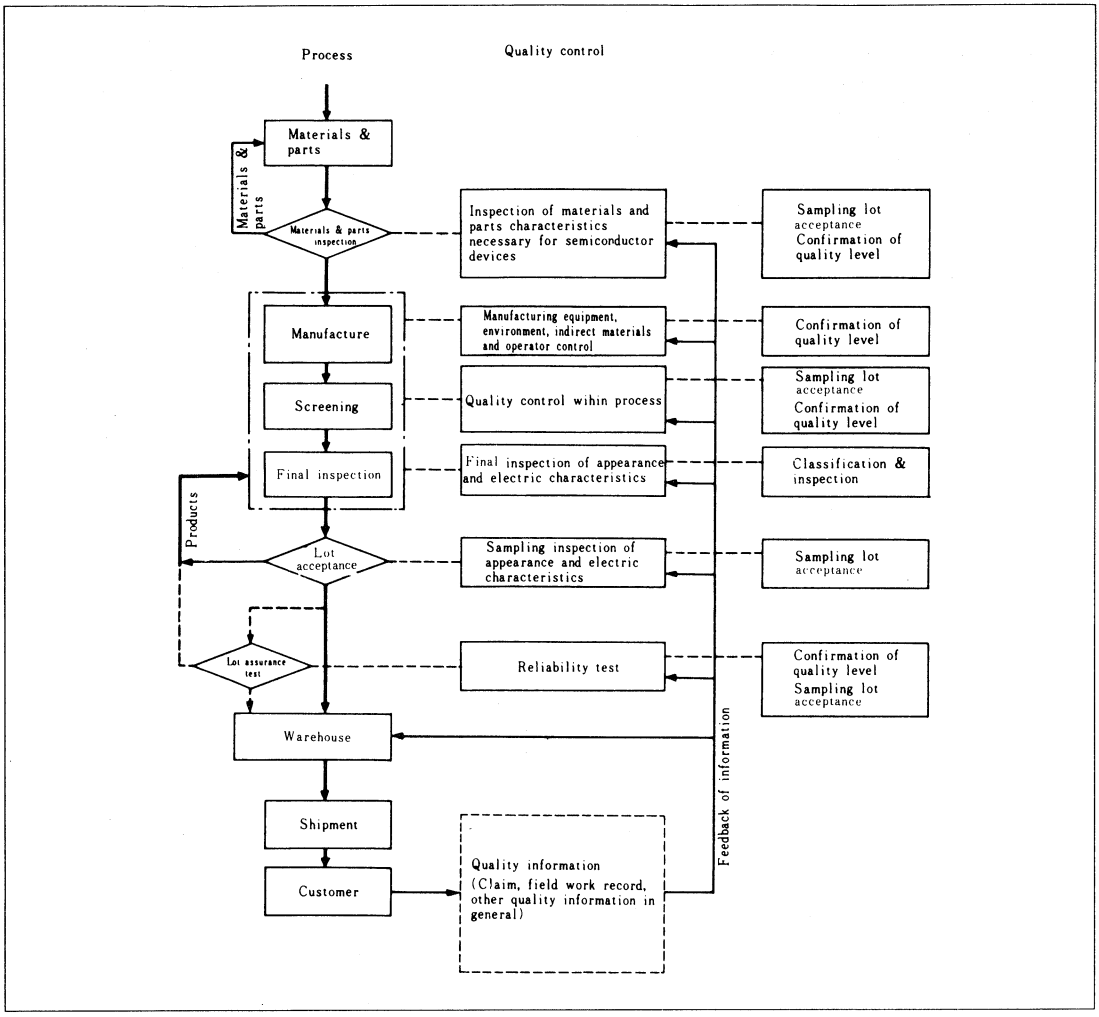


Fig.1 Flow Chart of Quality Control in Manufacturing Process

4. SELECTION OF PACKAGE TYPE AND RELIABILITY

4.1 SELECTION OF PACKAGE TYPE

Package types are generally classified into two; one is the harmetic sealed type using metal or glass, and the other is the plastic molded type. Selection of package types should be done with considering the purpose of system, environment, reliability cost etc. The reliability of plastic molded-type semiconductor devices has been greatly improved. Recently, their applications have also been expanded to automobiles, measuring and control systems, and computer terminal equipment operated under relatively severe conditions. Actually, field application data has revealed that their trouble factors under favorable indoor environmental conditions are equivalent to those of the hermetically sealed type. However, in the view of the guaranteed reliability (specifically, durability against environmental conditions), the hermetically sealed type passes inspection on a leak test 100%. Due to poor screening technology, the plastic molded type involves problems of moisture absorption or pereation inherent to their plastics materials. Therefore, Hitachi recommends users employ hermetically sealed-type semiconductor devices for certain types of systems which require high durability against environmental conditions, long service life, and high reliability. On the other hand, it is obvious that production output and applications of plastic molded-type semiconductor devices will be increased or expanded over the years that lie ahead. To fulfill such demands, Hitachi has exerted considerable efforts to improve moisture resistance, resistance against humidity cycles, operation stability, and chips and plastics manufacturing process. At present, Hitachi is confident that products featuring high durability against

environmental conditions will be available in the near future.

4.2 RELIABILITY OF PLASTIC MOLDING TYPE IC

Open and intermittent open troubles are major causes of reliability failure of the plastic-molded type IC. Fig. 2 indicates open fraction failure rate in terms of year. In recent years, the reliability in this aspect has been remarkably improved. Fig. 3 shows the data of moisture resistance.

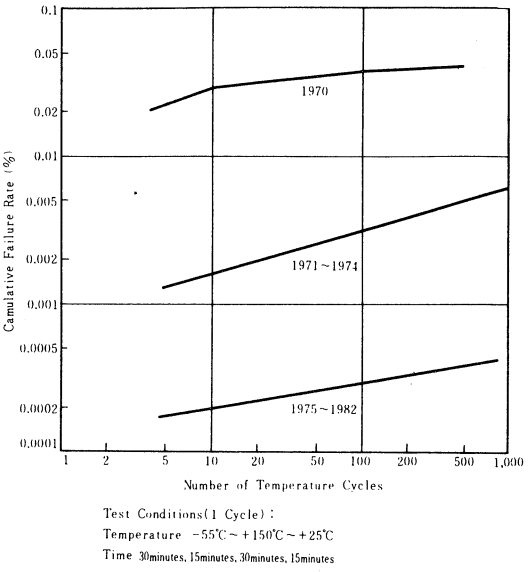


Fig.2 Changes in Terms of lear of Open Failure Rate in Temperature Cycle Test

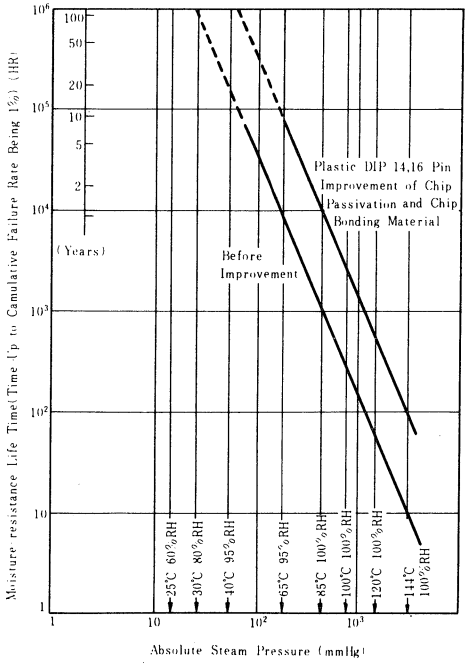


Fig.3 Moisture Resistance of Plastic-encapuslated IC's

5. RELIABILITY DATA

Here, we describe the results of reliability tests, data of failure rate, failure mode etc.

5.1 CRITERIA OF FAILURES

Table 3 shows the failure criteria in linear IC reliability test. The items of criteria and measuring conditions vary with the types of products.

Table.3 Criteria for Failures of Linear ICs (Example)

	Item	Criteria of failure (Note) min	Criteria of failure (Note) max	Unit	Remarks
Electric characteristics	Voltage gain	U−3	U+3	dB	
	Rated output	L×0.9	—	W	
	Total harmonic distortion	—	U×1.5	%	
	Output noise voltage	—	U×1.5	V	Including pulse noise.
	Input limiting voltage	—	U+3	dBμ	
	Power supply current	—	U×1.1	A	
	Input offset voltage	—	U×1.5	V	
	Input offset current	—	U×1.5	A	
	Input current & input bias current	—	U×1.3	A	
	Max. output voltage swing	L×0.9	U×1.1	V	
	Common mode input voltage range	L×0.9	—	V	
	Common mode rejection ratio	—	U+3	dB	
	Slew rate	—	U×1.5	V/μs	
	Open & short	Open, Intermittent, Short, Half-short. Including high & low temp. defects.		—	
Appearance & others	Airtight leak	Major leak & minor leak.			Applied to airtight sealing type devices.
	Appearance	According to limit sample.		—	
	Rusting & discoloration	According to limit sample.		—	
	Solderability	According to limit sample.		—	
	Marking	According to limit sample.		—	

Note) U : Initial limit max. value. L : Initial limit min. value.

Table.4 Results of Reliability Test on Linear ICs

Test Item	Test Condition	Plastic-molded Type No. of samples (pcs)	Plastic-molded Type Total testing time	Plastic-molded Type No. of failures (pcs)	Plastic-molded Type Failure rate* (1/hr)	Hermetic sealed Type (Cerdip) No. of samples (pcs)	Hermetic sealed Type (Cerdip) Total testing time	Hermetic sealed Type (Cerdip) No. of failures (pcs)	Hermetic sealed Type (Cerdip) Failure rate* (1/hr)
High temp. Operating life	Ta=125°C, $V_{CC}=V_{CC\ MAX}$ ($V_{EE}=V_{EE\ MAX}$)	1,660	1,190,000	5	5.3×10^{-6}	2,345	2,424,600	0	3.8×10^{-7}
Storage life	Ta=150°C	829	793,000	0	1.2×10^{-6}	485	463,700	0	2.0×10^{-6}
	Ta=−55°C	509	509,000	0	1.8×10^{-6}	—	—	—	—
	Ta=−65°C	—	—	—	—	376	376,000	0	2.4×10^{-6}
Humidity	Ta=65°C, 95%RH	3,110	2,727,000	0	3.4×10^{-7}	—	—	—	—
Bias humidity	Ta=85°C, 85%RH, $V_{CC}=V_{CC\ MAX}$ ($V_{EE}=V_{EE\ MAX}$)	443	443,000	0	2.1×10^{-6}	—	—	—	—
Temp. cycle	−55°C ~ +150°C 10 Cycles	10,043	—	0	—	2,198	—	0	—
Temp. cycle life	−55°C ~ +150°C 200 Cycles	4,280	—	0	—	900	—	0	—
Thermal shock	0°C ~ 100°C 10 Cycles	398	—	0	—	311	—	0	—
Solder heat	260°C, 10sec	404	—	0	—	305	—	0	—
Free drop	1,500G, 0.5ms, directions of X, Y, and Z, each. 3 times	160	—	0	—	260	—	0	—
Vibration fatigue	60Hz, 20G, directions of X, Y, and Z, each. 32hrs	160	—	0	—	260	—	0	—
Variable freq. vibration	100~2,000Hz, 20G, directions of X, Y, and Z, each. 3 times	160	—	0	—	260	—	0	—
Constant acceleration	20,000G, directions of X, Y, and Z, each. 1 minute	160	—	0	—	260	—	0	—
PCT	Ta=121°C, 2atoms t=60hrs	360	—	0	—	—	—	—	—
Solderability	230°C, 5 sec with rosin flux	160	—	0	—	300	—	0	—
Lead bend	225g, 90°, 3 times	90	—	0	—	45	—	0	—

*Confidence level : 60%

5.2 RELIABILITY TEST DATA OF LINEAR IC:

Table 4 is the results of linear IC life test and environmental test.

The reliability data concerning individual test results are available as they have already been prepared.

6. FAILURE RATE AND DERATING

Fig. 4 indicates the relation between the failure rate and the operating junction temperature obtained from various types of reliability tests and field records. With respect to the plastic-molded type and metal package type, the operating junction temperature is selected as a stress factor, and then the above relation is obtained from test data (mainly the high temperature operating life test) and field data. In the case of linear IC, it greatly depends on temperature on the average, so that it is confidently anticipated that the reliability can be effectively improved by temperature derating.

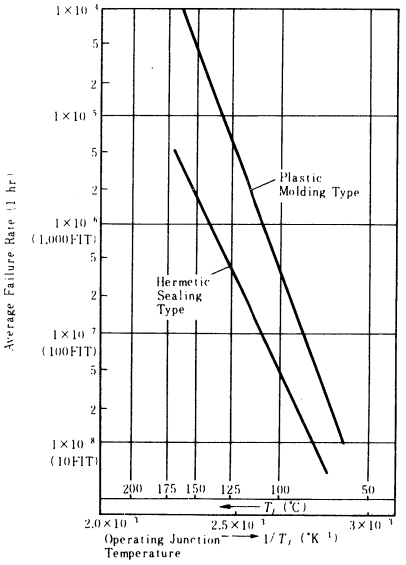


Fig.4 Derating Characteristics of Linear IC

7. HANDLING FOR MEASUREMENTS

Special attention should be paid about static electricity, noise of surge-voltage when semiconductor devices are measured. It is possible to prevent device breakdown by shorting their terminals to equalize electrical potential during transportation. However, when the devices are to be measured or mounted, they have to be left with terminals open and there is the possibility that they may be accidentally touched by a worker, measuring instrument, work bench, soldering iron, belt conveyor, etc. The device will be broken if it touches something which leaks current or has a static charge. Take care not to allow curve tracers, synchroscopes, pulse generators, D.C. stabilizing power supply units etc. to leak current through their terminals or housings. Especially, while the devices are being tested, take care not to apply surge voltage from the tester, or to attach a clamping circuit to the tester or not to apply any abnormal voltage through a bad contact from a current source. During measurment, pay special attention to miswiring and short-circuiting. When inspecting a printed circuit board, confirm that no soldering bridges or foreign matter is observed prior to turning the power switch ON. As these precautions depend upon the types of semiconductor devices, please contact Hitachi for further details.

8. PRECAUTIONS FOR PHYSICAL HANDLING

There are considerable precautions to install semiconductor devices to a printed circuit board. In order not to impaire the reliability of a semiconductor device during installation, cares should be taken when forming or cutting the leads, soldering and removing surplus flux.

8.1 FORMING AND CUTTING LEADS

When forming and cutting the lead wires of semiconductor devices, be careful of the following points:

(1) When bending the lead wires, hold the lead wires securely between the package and the point to be bent with a pair of pliers. Then, bend them, holding the open end of the leads with your fingers, so that no bending stress is applied to the package. Do not bend the leads by holding the package. The same consideration should be paid when many devices the simultaneously bent using lead forming machines.

(2) When bending the lead wires at right angles, make the bend at least 3 mm away from the package end. Do not bend them more than 90°. When they must be bent less than 90°, allow a space of more than 1.5 mm.

(3) Do not repeatedly bend the leads.

(4) Do not bend them sideways.

(5) Do not pull the leads with excessive force, to prevent the device from being broken. The prescribed tensile strength depends on their cross-sectional areas.

(6) Take care not to use any improper jig or pliers for bending, since the surfaces in contact with the plated surfaces of the lead wires may be damaged. It is advisable to use a tool with a contact area of 0.5 mm radius.

8.2 SOLDERING

It is not desirable in general to leave semiconductor devices at high temperature for a long time. Regardless of the soldering method, whether it may be a soldering iron or the flowing solder method, soldering must be done in the shorter time and at the lowest temperature possible. Your soldering work must meet test conditions of soldering heat, tolerability, namely, 260°C for 10 seconds and 350°C for 3 seconds at a point 1 to 1.5 mm away from the end of the device. Use of a strong alkali or acid flux may corrode the lead wires, deteriorating device characteristics. The recommended soldering iron is the type that is operated with a secondary voltage supplied by a transformer and grounded to prevent current leads. Try to solder the lead wires at the farthest point from the device surface.

8.3 REMOVING RESIDUAL FLUX

To ensure the reliability and lifetime of electronic systems, residual flux must be removed from circuit boards. Detergent or ultrasonic cleaning is usually applied. If cholorous detergent is used for the plastic molded devices, package corrosion may occur. Since cleaning over extended periods or at high temperatures will cause swollen chip coating due to solvent permeation, pay special attention to these precautions prior to dissolution and toxity. Do not use any trichlorethylene solvent. For ultrasonic washing, the following conditions are advisable:

Frequency: 28 to 29 kHz (to avoid device resonation)

Ultrasonic output: 15W/1 (once)

Do not allow the devices to contact the generator source directly.

Washing time: Less than 30 seconds

DATA SHEETS
Operational Amplifiers

HA17080 Series ●J-FET Input Operational Amplifiers

J-FET Input Operational Amp. provides excellent characteristics including high input impedance and low input bias current, since its input differential amp. is constructed by J-FET Pair Transistor. Accordingly it finds wide application of general controlling instrument, medical instrument. Especially it is optimum in signal precessing from sensor of high impedance. Hitachi prepares J-FET Input Operational Amp. series of one monolithic bipolar chip, HA17080, HA17082, HA17083, HA17084.

■PRODUCT OUTLINE

J-FET Input Operational Amp. series provides single, dual, quad, and they are all internal phase compensated type excepting HA17080, and include condenser for phase compensation use. And HA17080 and HA17083 are capable of offset adjustment. Package provides two types of plastic sealing and glass sealing, and "A" glade with rigid electrical characteristic specification. Use satisfying uses.

Item	HA17080	HA17082	HA17083	HA17084
The number of Operational Amplifier (the number of channel)	Single	Dual		Quad.
Offset Adjusting Terminal	Exist	Not exist	Exist	Not exist
Phase Compensating Method	External	Internal		

■FEATURES

- Wide operating supply voltage range ±5 to ±18V
- Low input bias current 30pA
- Low input offset current 5pA
- High input impedance $10^{12}\Omega$
- High slew rate 13V/μs
- Wide common mode input voltage range
- Operation to input near supply voltage (Vcc) is possible.
- High voltage gain 106dB
- HA17080, HA17083 are capable of offset adjustment.
- Pin for pin compatible with Texas TL080 series

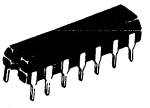
■NOTE

Since this IC is high input impedance operational amp, handling by hand may cause the input bias current and input offset current to be rise due dirt. Care shealed be taken for handling.

HA17080PS, HA17082PS

(DP-8)

HA17083P, HA17084P



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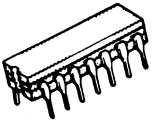
HA17080GS, HA17082GS

(DG-8)

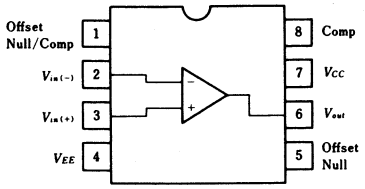
HA17083G



(DG-14)

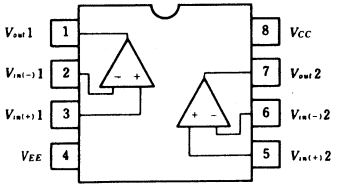
■PIN ARRANGEMENT

●HA17080



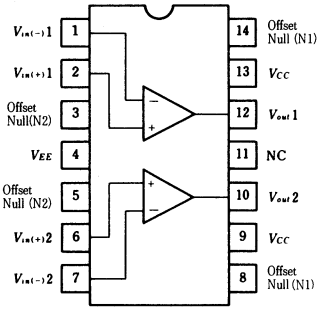
(Top View)

●HA17082



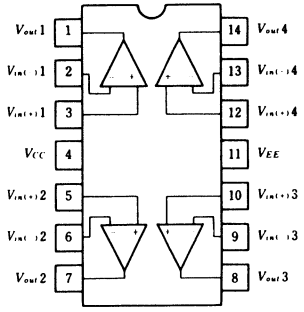
(Top View)

●HA17083



(Top View)

●HA17084



(Top View)

■ABSOLUTE MAXIMUM RATINGS (Ta=25°C)

Item	Symbol	P, PS series	G, GS series	Unit	Note
Supply Voltage	V_{CC}	+18	+18	V	
Supply Voltage	V_{EE}	−18	−18	V	
Differential Input Voltage	$V_{in(diff)}$	±30	±30	V	
Input Voltage	V_{in}	±15	±15	V	1
Power Dissipation	P_T	625	625	mW	2
Operating Temperature	T_{opr}	−20 to +75	−40 to +85	°C	
Storage Temperature	T_{stg}	−55 to +125	−65 to +150	°C	

Notes 1. If supply voltage is less than ±15V, input voltage is to supply voltage.
2. P and PS are permissible values to Ta=50°C, and beyond that, derate with 8.3mW/°C. G and GS are permissible values to Ta=70°C, and beyond that, derate with 7.8mW/°C.

■ELECTRICAL CHARACTERISTICS (V_{CC}=−V_{EE}=15V, Ta=25°C)

Item	Symbol	Test Condition		min	typ	max	Unit	Note
Input Offset Voltage	V_{IO}	R_S=50Ω	Non A	—	5	15	mV	1
			A version	—	3	6		
Input Offset Current	I_{IO}	$I_{IO}=\|I_{I(+)}-I_{I(-)}\|$	Non A	—	5	200	pA	1
			A version	—	5	100		
Input Bias Current	I_I		Non A	—	30	400	pA	1, 2
			A version	—	30	200		
Common Mode Input Voltage Range	V_{CM}		Non A	±10	—	—	V	1
			A version	±11	—	—		
Peak To Peak Output Voltage	V_{OP-P}	R_L≧10kΩ		24	27	—	V	
		R_L≧2kΩ		20	24	—		
Voltage Gain	A_{VD}	R_L≧2kΩ, V_O=±10V	Non A	88	106	—	dB	1
			A version	94	106	—		
Common Mode Rejection Ratio	CMR	R_S≦10kΩ	Non A	70	86	—	dB	1
			A version	80	86	—		

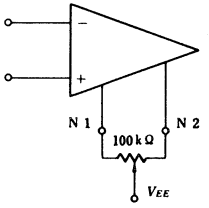
(to be continued)

■ ELECTRICAL CHARACTERISTICS (Continued)

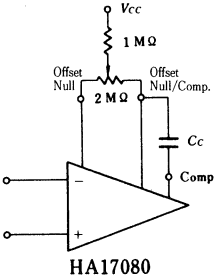
Item	Symbol	Test Condition		min	typ	max	Unit	Note
Line Regulation	*PSRR*	$R_S \leqq 10k\Omega$	Non A	70	86	—	dB	1
			A version	80	86	—		
Supply Current	I_{CC}			—	1.4	2.8	mA	3
Band Width	*BW*	$A_{VD}=1$		—	3	—	MHz	
Slew Rate	*SR*	$V_{in}=10V$, $R_L=2k\Omega$, $C_L=100pF$, $A_{VD}=1$		—	13	—	V/μs	
Channel Separation	*CS*	$A_{VD}=100$		—	120	—	dB	
Rise Time	t_r	$V_{in}=20mV$, $R_L=2k\Omega$,		—	0.1	—	μs	
Overshoot	V_{over}	$C_L=100pF$, $A_{VD}=1$		—	10	—	%	
Input Resistance	R_{in}			—	10^{12}	—	Ω	
Input Noise Voltage	V_n	$R_S=100\Omega$, $f=1kHz$		—	35		$nV/\sqrt{Hz}$	

Notes) 1. Non A is the standard to HA17080, HA17082, HA17083, HA17084.
A version is the standard to HA17080A, HA17082A, HA17083A, HA17084A.
2. It's Gate Leak Current of J-FET, and depends on temperature.
At the time of measurement, it is necessary to keep junction temperature.
3. It's the value per 1 channel.

■ VOLTAGE OFFSET ADJUSTING CIRCUIT

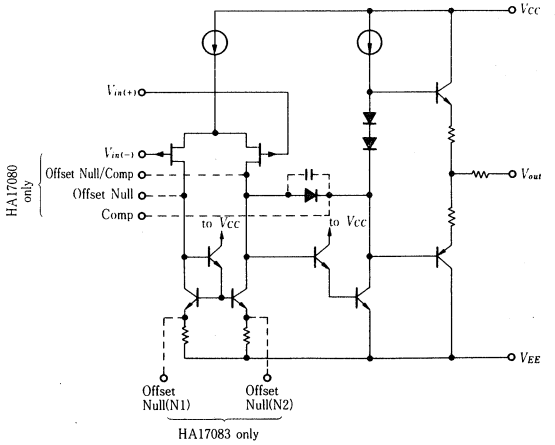


HA17083

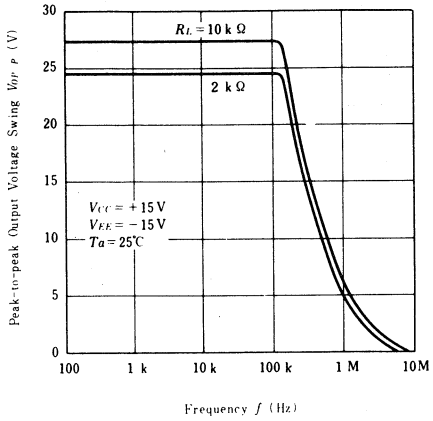


HA17080

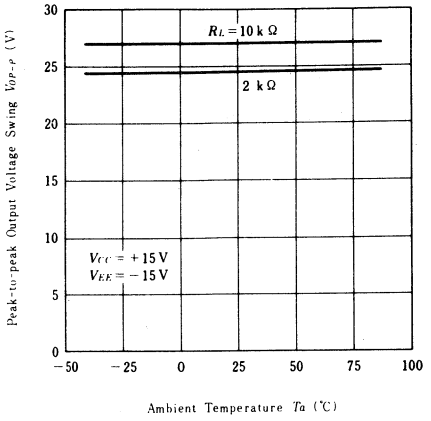
■ CIRCUIT SCHEMATIC



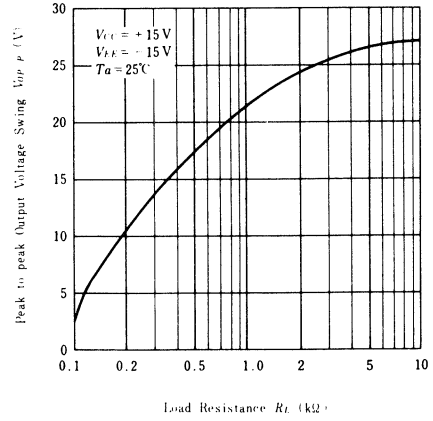
PEAK TO PEAK OUTPUT VOLTAGE SWING VS FREQUENCY



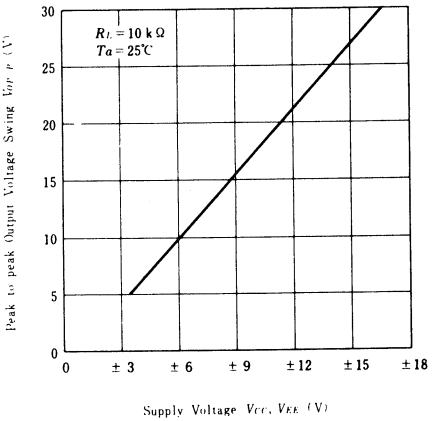
PEAK TO PEAK OUTPUT VOLTAGE SWING VS AMBIENT TEMPERATURE



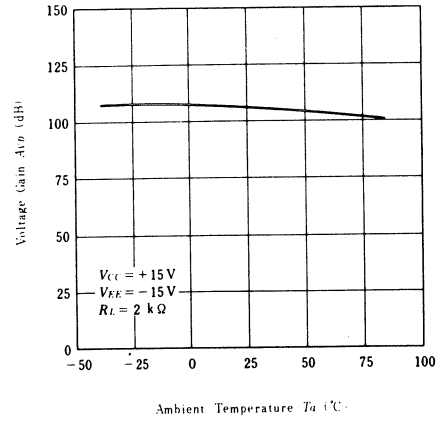
PEAK TO PEAK OUTPUT VOLTAGE SWING VS LOAD RESISTANCE



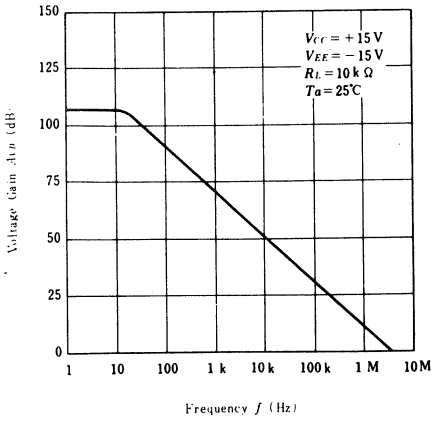
PEAK TO PEAK OUTPUT VOLTAGE SWING VS SUPPLY VOLTAGE



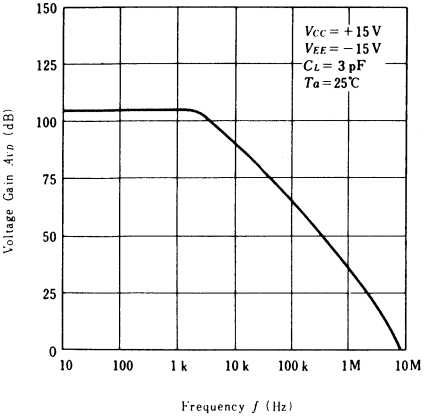
VOLTAGE GAIN VS AMBIENT TEMPERATURE



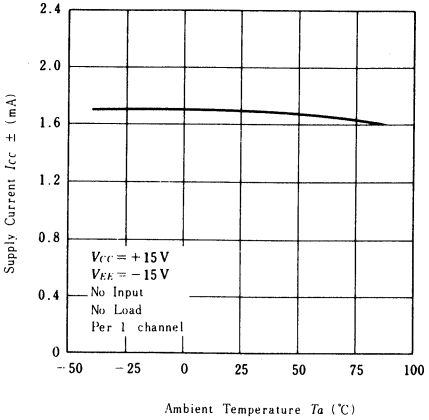
VOLTAGE GAIN VS FREQUENCY



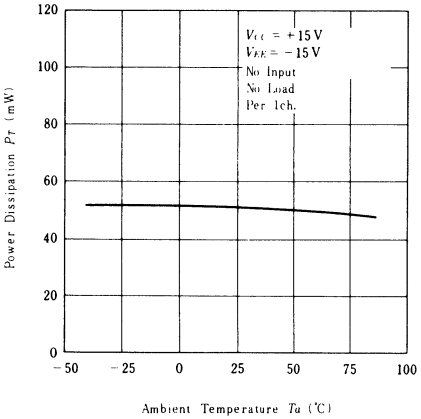
HA17080 VOLTAGE GAIN VS FREQUENCY



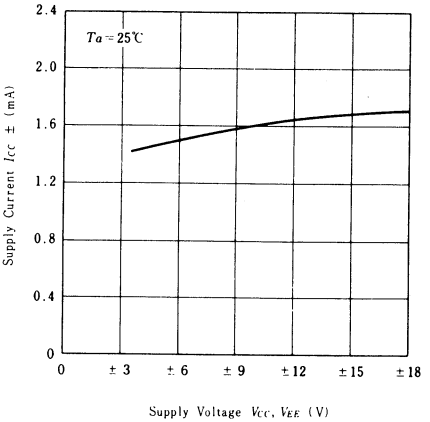
SUPPLY CURRENT VS AMBIENT TEMPERATURE



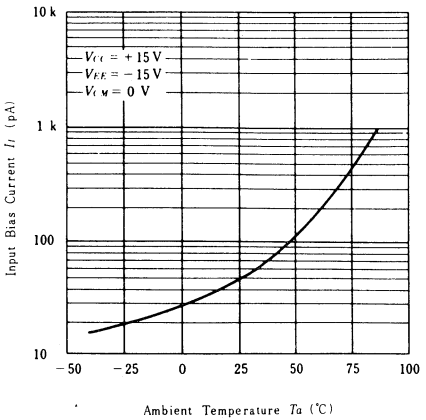
POWER DISSIPATION VS AMBIENT TEMPERATURE



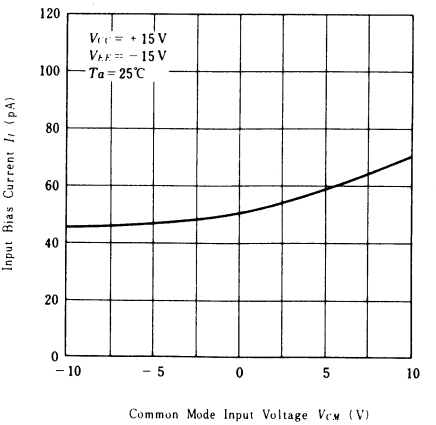
SUPPLY CURRENT VS SUPPLY VOLTAGE



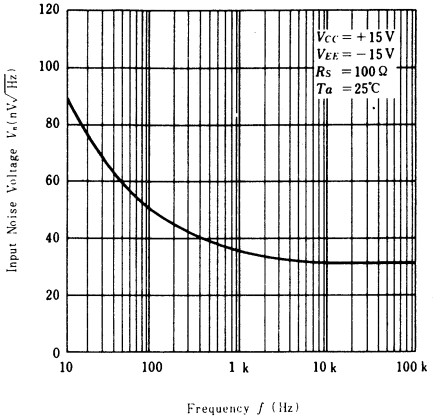
INPUT BIAS CURRENT VS AMBIENT TEMPERATURE



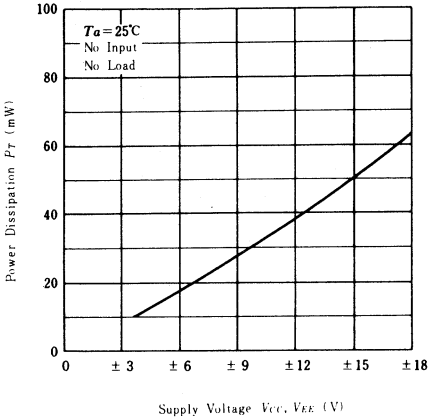
INPUT BIAS CURRENT VS COMMON MODE INPUT VOLTAGE



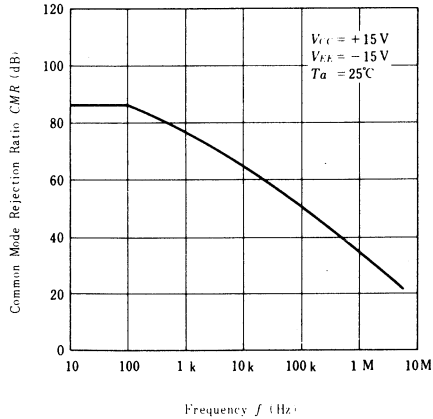
INPUT NOISE VOLTAGE VS FREQUENCY



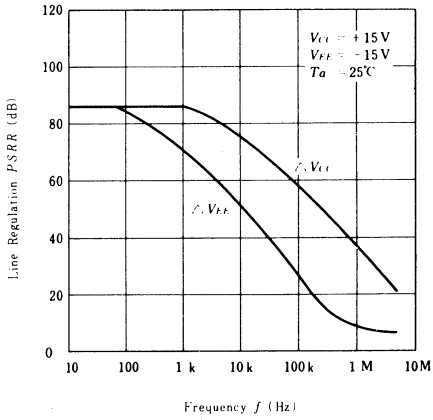
POWER DISSIPATION VS SUPPLY VOLTAGE



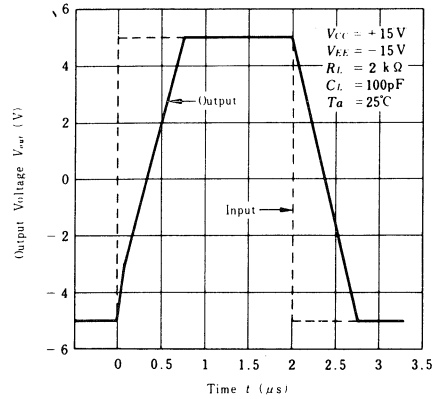
COMMON MODE REJECTION RATIO VS FREQUENCY



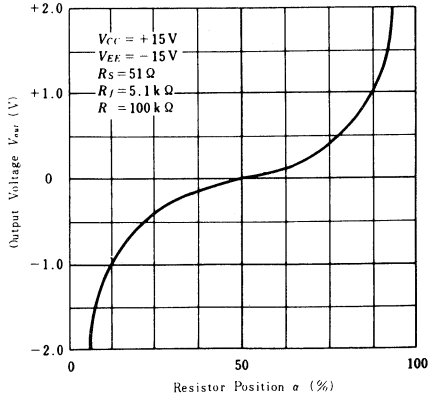
LINE REGULATION VS FREQUENCY



VOLTAGE FOLLOWER LARGE SIGNAL PULSE RESPONSE



HA17083 OFFSET ADJUSTING



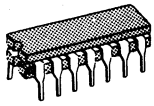
HA17301 Series ● Quad. Operational Amplifier

HA17301 is a quad. operational amplifier which provides internal phase compensation, and mono power source operational is possible. Generally, it can used for waveform generator, voltage regulator, logical operation circuit, voltage control oscillator, etc.

HA17301P

(DP-14)

HA17301G

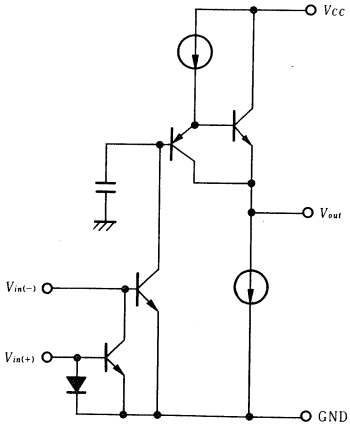


(DG-14)

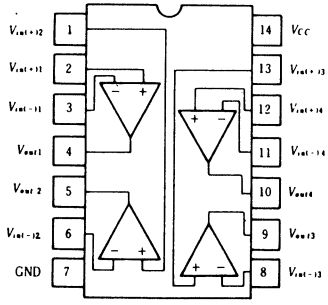
■ FEATURES

- Wide range of Operating Temperature
- Mono Power Source Operation is possible
- Internal Phase Compensation
- Small Input Bias Current

■ CIRCUIT SCHEMATIC (1/4)



■ PIN ARRANGEMENT



(Top View)

■ ABSOLUTE MAXIMUM RATINGS ($Ta = 25°C$)

Item	Symbol	HA17301P	HA17301G	Unit
Supply Voltage	V_{CC}	28	28	V
Non-inverted Input Current	I_r	5	5	mA
Sink Current	I_{sink}	50	50	mA
Source Current	I_{source}	50	50	mA
Power Dissipation*	P_T	625	625	mW
Operating Temperature	T_{opr}	−20 to +75	−40 to +85	°C
Storage Temperature	T_{stg}	−55 to +125	65 to +150	°C

* In HA17301P, it is a value under $Ta = 50°C$. In case of more than it, 8.3mW/°C derating shall be done.
In HA17301G, it is a value under $Ta = 70°C$. In case of more than it, 7.6mW/°C derating shall be done.

■ ELECTRICAL CHARACTERISTICS-1 ($V_{CC} = +15V$, $R_L = 5.0k\Omega$, $Ta = 25°C$)

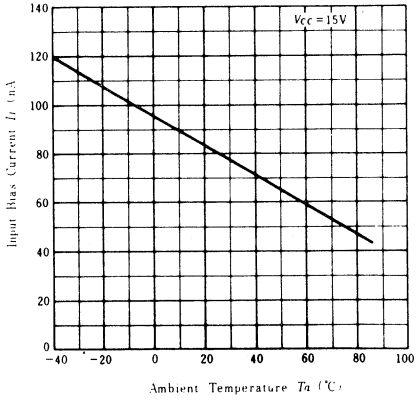
Item	Symbol	Test Condition	min	typ	max	Unit
Voltage Gain	A_{VD}		1000	1400	—	V/V
Supply Voltage	I_{DD}	Non-inverted input: open	—	7.7	10	mA
	I_{DD}	Non-inverted input: GND	—	8.3	14	mA
Input Bias Current	I_I	R_I = 0	—	80	300	nA
Current Mirror Gain	A_I	I_r = 200μA	0.80	0.94	1.16	A/A
Source Current	I_{source}	V_{OH} = 0.4V	3	13	—	mA
		V_{OH} = 9.0V	—	10	—	mA
Sink Current	I_{sink}	V_{OL} = 0.4V	0.5	0.75	—	mA
Output Voltage	V_{OH}		13.5	13.9	—	V
	V_{OL} (inv)	Inverted Input Driving	—	0.04	0.1	V
	V_{OL} (non-inv)	Non-inverted input Driving	—	0.55	—	V
Output Resistance	R_O	Inverted input Only	0.1	1.0	—	MΩ
Slew Rate	SR	C_L = 100pF, R_L = 5.0kΩ	—	0.2	—	V/μs
Bandwidth	BW	A_V = 1	—	2.6	—	MHz
Phase Margin	ϕm		—	87	—	deg
Power Source Rejection Ratio	$PSRR$	f = 100Hz	—	63	—	dB
Channel Separation	CS	f = 1.0kHz	—	63	—	dB

■ ELECTRICAL CHARACTERISTICS-2 ($V_{CC} = +15V$, $R_L = 5.0k\Omega$, $-40°C \leq Ta \leq 85°C$)

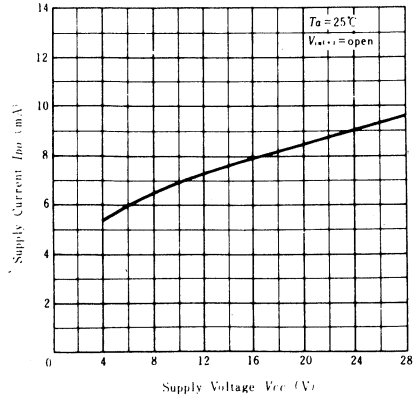
Item	Symbol	Test Condition	min	typ	max	Unit
Voltage Gain	A_{VD}		—	1400	—	V/V
Input Bias Current	I_I		—	80	—	nA
Current Mirror Gain Drift	A_I		—	+2.1	—	%

Note In HA17301P: $V_{CC} = +15V$, $R_L = 5.0k\Omega$, $-20°C \leq Ta \leq 75°C$

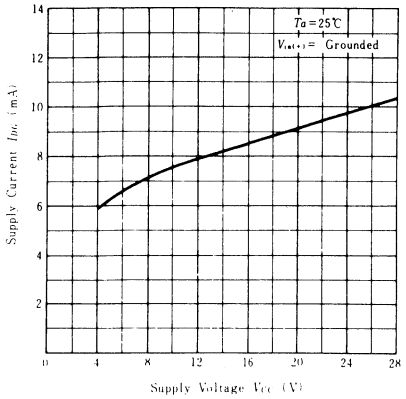
INPUT BIAS CURRENT VS. AMBIENT TEMPERATURE



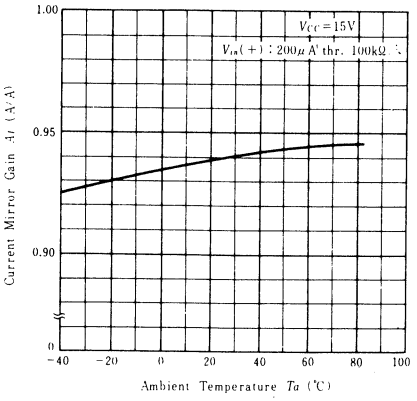
SUPPLY CURRENT VS. SUPPLY VOLTAGE (1)



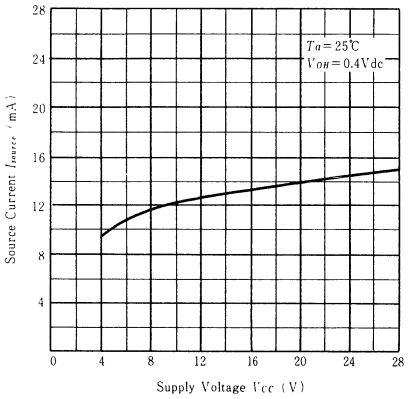
SUPPLY CURRENT VS. SUPPLY VOLTAGE (2)



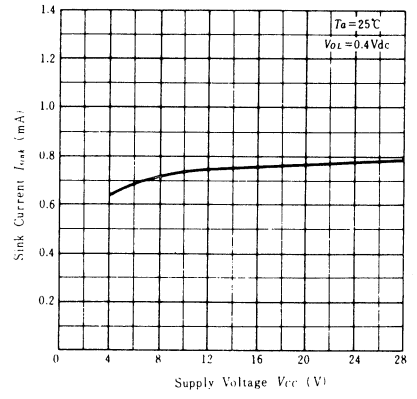
CURRENT MIRROR GAIN VS. AMBIENT TEMPERATURE



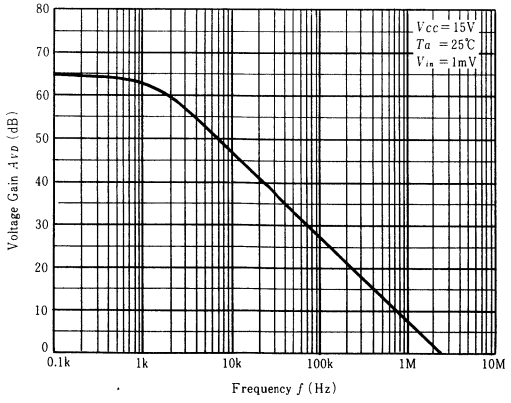
SOURCE CURRENT VS. SUPPLY VOLTAGE



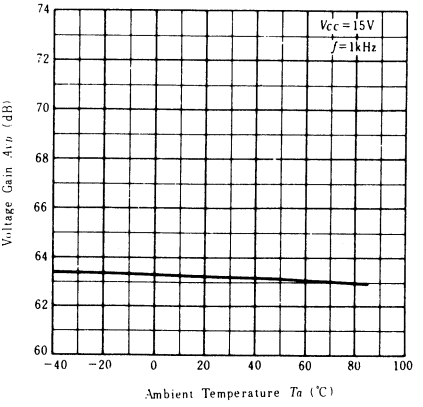
SINK CURRENT VS. SUPPLY VOLTAGE



VOLTAGE GAIN VS. FREQUENCY



VOLTAGE GAIN VS. AMBIENT TEMPERATURE



■ HA17301 APPLICATION

HA17301 is a Quad. Operational Amplifier, and it's consisted of four operational amplifiers which operate independently, and a bias circuit. It can be widely used with the features such as wide range of operating temperature, mono power source operation, internal phase compensation, wide 0-cross bandwidth, small input bias current, large open loop voltage gain, etc.

HA17301 applications will be explained below.

1. HA17301 Circuit Operation

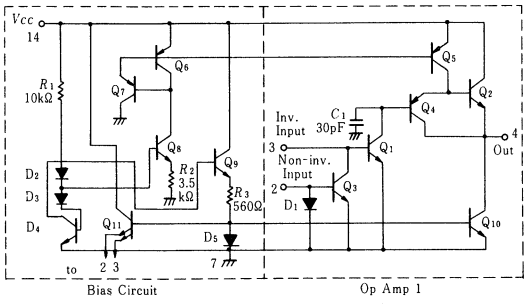


Fig.1 HA17301 Internal Equivalent Circuit

Fig.1 shows HA17301 Internal Equivalent Circuit; Bias Circuit & Operational Amplifier (Op Amp 1).

The Op Amp 1 is a emitter GND type amplifier. The Inversion Amp is consisted of Input Transistor (Q1), Buffer Transistor (Q4), Current Source Transistor (Q5), Output Emitter Follower Transistor (Q2) and Current Source Transistor (Q10). In this circuit, the voltage gain is all depend on TRS Q1, and large open loop gain will be obtained by current source load Q5, even if the supply voltage is small.

Emitter Follower TRS Q2 lowers the input impedance. Using the Power Source TRS Q10 for load of Q2 enables to get very large dynamic range, which is actually from GND to (Vcc-1).

Buffer TRS Q4 is to lower the input current without raising the DC input voltage level. When the inversion amp is used in closed circuit, capacitor C1 is provided to keep the circuit stable, so no external compensation is required.

Next, we would like to look at Non-inverted Input.

The current flowing into a non-inverted input is, if current amplification of Q3 is large enough, flown through diode D1. The input current causes voltage drop at D1, which will be added to base-emitter junction of Q3. Therefore, if D1 and Q3 are matching, the current flown to Q3 emitter is the same as the input current. And if the current amplification of Q3 is large enough, the same current as the input current is flown to Q3 collector. This is known as "Current Mirror". When using an external feedback resistor, the same current as the non-inverted input current is flown to it, and the output voltage can be established.

Finally, we would like to explain a Bias Circuit. This circuit is to give bias voltage to current source Q_5 and Q_{10} of operational amp, in which reference voltage is voltage drop of D_2, D_3 and D_4.

Emitter current of Q_8 (I_{E8}) is;

$$I_{E8} = \frac{V_{D3} + V_{D4} - V_{BE8}}{R_2} \quad \cdots\cdots(1)$$

where; V_{D3} ..... voltage drop of D3
V_{D4} ..... voltage drop of D4
V_{BE8} ..... V_{BE} of Q_8

When these elements are all matching;

$$V_{D3} = V_{D4} = V_{BE8} = V_{BE} \quad \cdots\cdots(2)$$

$$\therefore I_{E8} = \frac{V_{BE}}{R_2} \quad \cdots\cdots(3)$$

PNP Current Source Q_5 will be set to be V_{BE}/R_2 by Q_6. Emitter current of Q_9 (I_{E9}) is;

$$I_{E9} = \frac{V_{D2} + V_{D3} + V_{D4} - V_{D5} - V_{BE9}}{R_3} \quad \cdots\cdots(4)$$

When these elements are all matching;

$$V_{D2} = V_{D3} = V_{D4} = V_{D5} = V_{BE9} = V_{BE} \quad \cdots\cdots(5)$$

$$\therefore I_{E9} = \frac{V_{BE}}{R_3} \quad \cdots\cdots(6)$$

NPN Current Source Q_{10} will be set to be V_{BE}/R_3 by D_5. The most important feature of this bias circuit is that the value of current source is not depend on the supply voltage. Q_{11} is used for protection when a negative signal is applied.

2. Inversion Amplifier

Biasing of Inversion Amplifier can be performed by one of the following three methods; mono power source biasing method, NV_{BE} biasing method and negative voltage biasing method.

2.1 Mono Power Source Biasing Method

Fig.2 shows an AC amp biased with the power source which is used for amp operation.

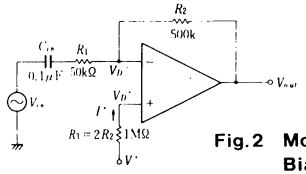


Fig.2 Mono Power Source Biasing Method

$$\frac{V_{out}}{V_{in}} = -\frac{R_2}{R_1} \quad \cdots\cdots(7)$$

2.2 NV_{BE} Biasing Method

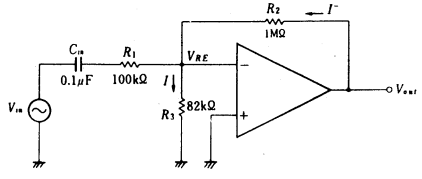


Fig.3 NV_{BE} Biasing Method

This is the most useful application of Inversion AC Amplifier. Bias voltage of the inverted input (V_{BE}) is determined by the current flowing through resistor R_3 to GND.

$$\frac{V_{out}}{V_{in}} = -\frac{R_2}{R_1} \quad \cdots\cdots (8)$$

3. Triangular Wave Generator

A triangular wave is made by integrating an AC voltage (in which positive & negative values are repeating one after the other). The relation between the input and the output is shown below.

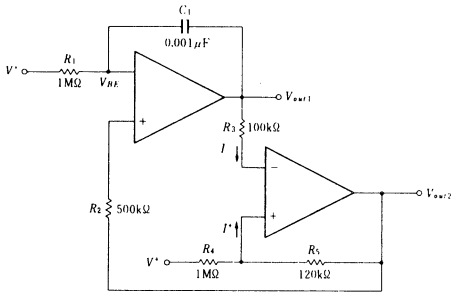


Fig.4 Triangular Wave Generator

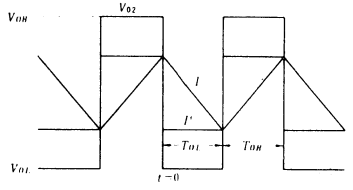


Fig.5 Operation of Triangular Wave Generator

$$T_{OL} = \frac{C_1 R_1 R_3 V_{OH}}{R_5 (V^+ - V_{BE})} \quad \cdots\cdots (9)$$

$$T_{OH} = \frac{C_1 R_3 V^+}{R_5 \left(\frac{V_{OH}}{R_2} - \frac{V^+ - V_{BE}}{R_1} \right)} \quad \cdots\cdots (10)$$

Under the conditions of $R_1 = 2R_2$, $V_{OH} = V^+$, $V^+ \gg V_{BE}$;

$$T_{OH} + T_{OL} = \frac{2C_1 R_1 R_3}{R_5} \quad \cdots\cdots (11)$$

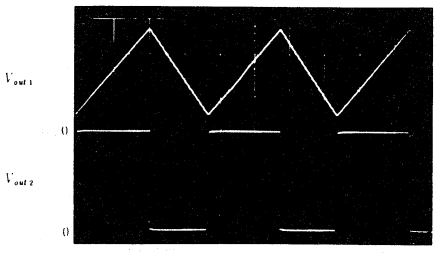


Fig.6 Operation Waveform of Triangular Wave Generator

Table 1

	Item	Test Condition	Measured Value	Calculated Value	Unit
Triangular Wave Generator	T_{OH}	V_{CC} = 15V, V^+ = 15V, C_1 = 0.001μF, R_1 = 1MΩ, R_2 = 500kΩ, R_3 = 100kΩ, R_4 = 1MΩ, R_5 = 120kΩ, Fig. 4	1.06	0.83	ms
	T_{OL}		0.82	0.83	ms
	V_{OH}		13.5	14	V
	V_{OL}		1.5	1.5	V

4. Comparator

We would like to show applications of HA17301 to comparators; Positive Input Voltage Comparator, Negative Input Voltage Comparator and Power Comparator.

4.1 Positive Input Voltage Comparator

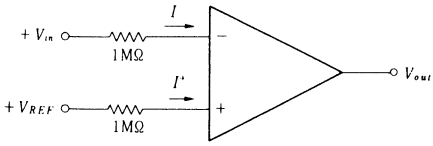


Fig.7 Positive Input Voltage Comparator

Vout is equal to V_{OH} under $I^- < I^+$, and Vout is equal to V_{OL} under $I^- > I^+$. For normal operation, the reference voltage should be more than V_{BE}.

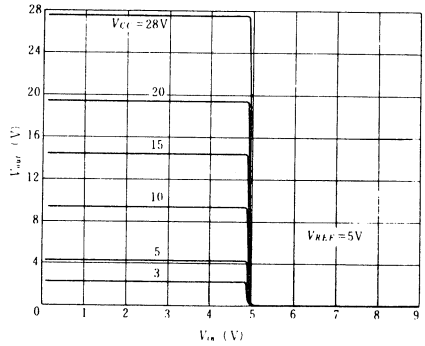


Fig.8 Operation Characteristics of Positive Input Voltage Comparator (1)

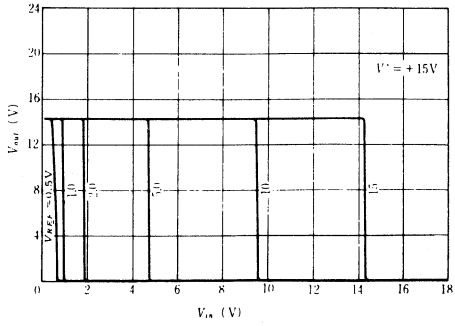


Fig.9 Operation Characteristics of Positive Input Voltage Comparator (2)

4.2 Negative Input Voltage Comparator

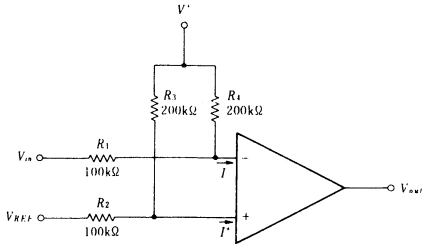


Fig.10 Negative Input Voltage Comparator

$$V_{IN} > R_1 \left\{ V_{BE}\left(\frac{1}{R_1}+\frac{1}{R_4}\right) - \frac{V^+}{R_4} \right\} \quad \cdots\cdots (12)$$

$$V_{REF} > R_2 \left\{ V_{BE}\left(\frac{1}{R_2}+\frac{1}{R_3}\right) - \frac{V^+}{R_3} \right\} \quad \cdots\cdots (13)$$

When using resistor R_4 and R_3 which meet Equation (12) and (13) respectively, negative values of V_{IN} and V_{REF} are available. As same as in the positive input voltage comparator, Vout is equal to V_{OH} under $I^- < I^+$ and Vout is equal to V_{OL} under $I^- > I^+$.

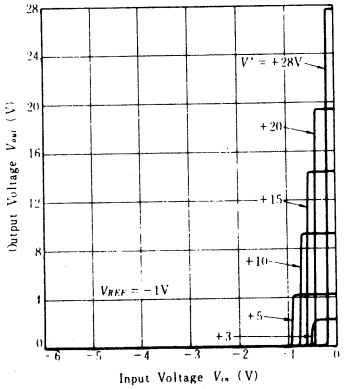


Fig.11 Operation Characteristics of Negative Input Comparator (1)

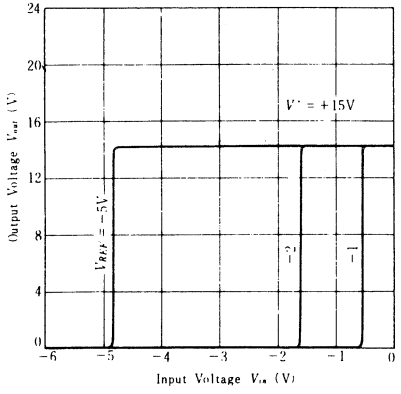


Fig.12 Operation Characteristics of Negative Input Comparator (2)

4.3 Power Comparator

By adding a TRS externally, a load that requires a current larger than the output current of HA17301 can be connected as shown below.

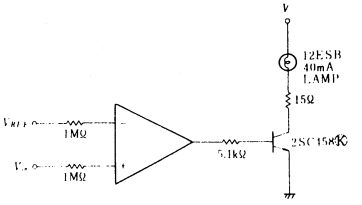


Fig.13 Power Comparator

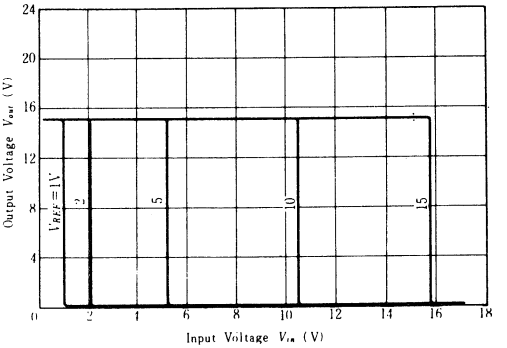


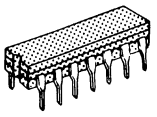
Fig.14 Operation Characteristics of Power Comparator V_{CC} = 15V

HA17324 Series ●Quad. Operational Amplifier

HA17324 is Quad. Operational Amplifier that provide high gain and internal phase compensation, and mono power source operation is possible. They can be widely used to control equipments.

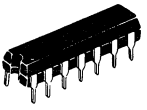
Industrial use HA17324G, HA17324P
Commercial use; HA17324

HA17324G



(DG-14)

HA17324P
HA17324

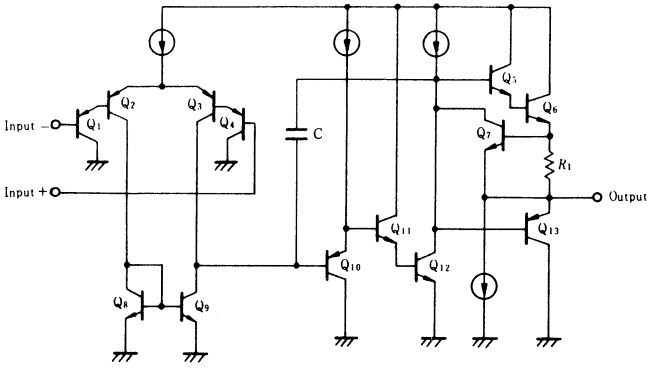


(DP-14)

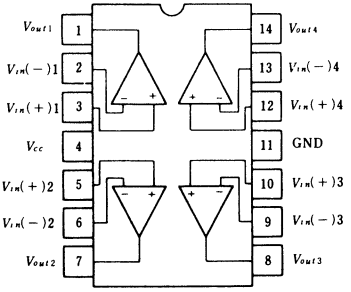
■FEATUERS

- Wide range of supply voltage, and mono power source operation is possible.
- Internal Phase Compensation
- Wide range of common mode voltage, and possible to operate with an input about 0V.

■CIRCUIT SCHEMATIC (1/4)



■PIN ARRANGEMENT



(Top View)

■ ABSOLUTE MAXIMUM RATING ($Ta = 25°C$)

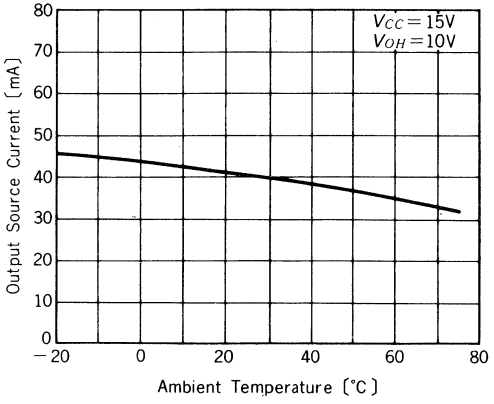
Item	Symbol	HA17324G	HA17324P	HA17324	Unit
Supply Voltage	V_{CC}	32	32	32	V
Sink Current	I_{sink}	50	50	50	mA
Power Dissipation	P_T	625*	625**	625**	mW
Common Mode Input Voltage	V_{CM}	−0.3 to V_{CC}	−0.3 to V_{CC}	−0.3 to V_{CC}	V
Differential Input Voltage	$V_{in(diff)}$	$\pm V_{CC}$	$\pm V_{CC}$	$\pm V_{CC}$	V
Operating Temperature	T_{opr}	−20 to +75	−20 to +75	0 to +70	°C
Storage Temperature	T_{stg}	−60 to +150	−55 to +125	−55 to +125	°C

* Value under $Ta \leqq 70°C$. In case of more than it, 7.6mW/°C derating shall be done.
** Value under $Ta \leqq 50°C$. In case of more than it, 8.3mW/°C derating shall be done

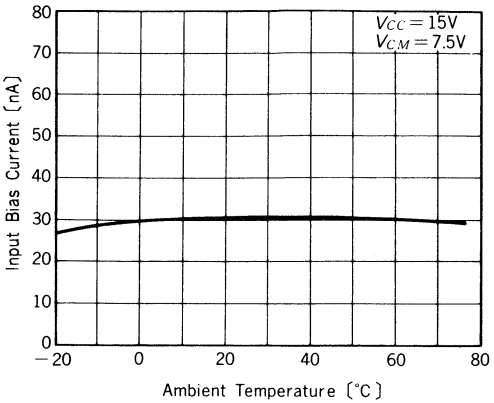
■ ELECTRICAL CHARACTERISTICS ($V_{CC} = +15V$, $Ta = 25°C$)

Item	Symbol	Test Conditions		min	typ	max	Unit
Input Offset Voltage	V_{IO}	$V_{CM} = 7.5V$, $R_S = 50\Omega$, $R_f = 50k\Omega$		—	2	7	mV
Input Offset Current	I_{IO}	$I_{IO} = \lvert I_I - I_I' \rvert$, $V_{CM} = 7.5V$		—	5	50	nA
Input Bias Current	I_I	$V_{CM} = 7.5V$		—	30	500	nA
Power Source Rejection Ratio	$PSRR$	$f = 100Hz$, $R_S = 1k\Omega$, $R_f = 100k\Omega$		—	93	—	dB
Voltage Gain	A_{VD}	$R_S = 1k\Omega$, $R_f = 100k\Omega$, $R_L = \infty$		75	90	—	dB
Common Mode Rejection Ratio	CMR	$R_S = 50\Omega$, $R_f = 5k\Omega$		—	80	—	dB
Common Mode Input Voltage Range	V_{CM}	$R_S = 1k\Omega$, $R_f = 100k\Omega$, $f = 100Hz$		−0.3	—	13.5	V
Peak-to-peak Output Voltage	$V_{op\ p}$	$f = 100Hz$, $R_S = 1k\Omega$, $R_f = 100k\Omega$, $R_L = 20k\Omega$		—	13.6	—	V
Output Source Current	I_{source}	$V_{in}^- = 1V$, $V_{in}^+ = 0V$, $V_{OH} = 10V$		20	40	—	mA
Output Sink Current	I_{sink}	$V_{in}^- = 0V$, $V_{in}^+ = 1V$, $V_{OL} = 2.5V$		10	20	—	mA
Supply Current	I_{CC}	$V_{in} = GND$, $R_L = \infty$		—	0.8	2	mA
Power Dissipation	P_T	$R_L = \infty$, $V_{in} = GND$		—	12	30	mW
Slew Rate	SR	$f = 1.5kHz$, $V_{CM} = 7.5V$, $R_L = \infty$		—	0.19	—	V/μs
Channel Separation	CS	$f = 1kHz$		—	120	—	dB
Output Sink Current	I_{sink}	$V_{in}^+ = 0V$, $V_{in}^- = 1V$	$V_{OL} = 200mV$	15	50	—	μA
			$V_{OL} = 1V$	3	9	—	mA
Output Voltage	V_{OH}	$I_{OH} = -1mA$		13.2	13.6	—	V
		$I_{OH} = -10mA$		12.0	13.3	—	
	V_{OL}	$I_{OL} = 1mA$		—	0.8	1.0	V
		$I_{OL} = 10mA$		—	1.1	1.8	

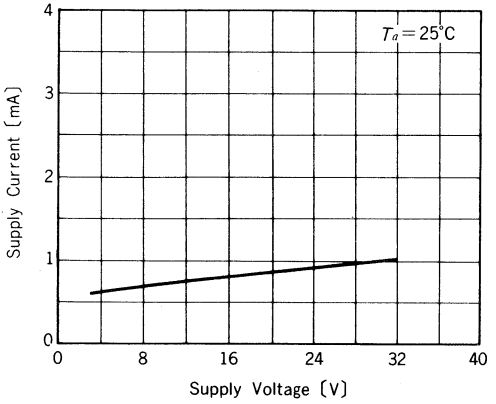
Output Source Current vs Ambient Temperature



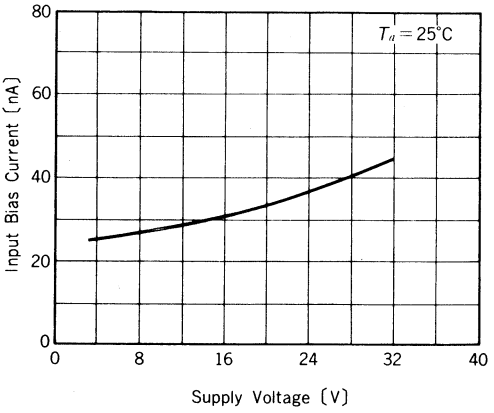
Input Bias Current vs Ambient Temperature.



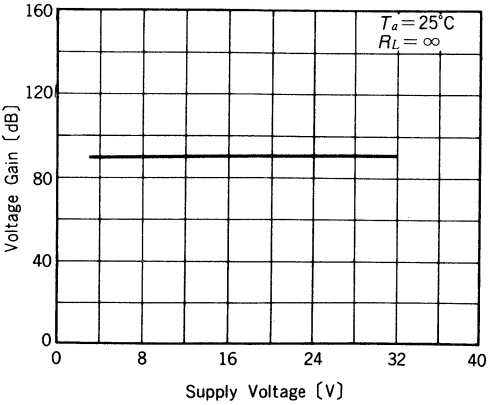
Supply Current vs Supply Voltage.



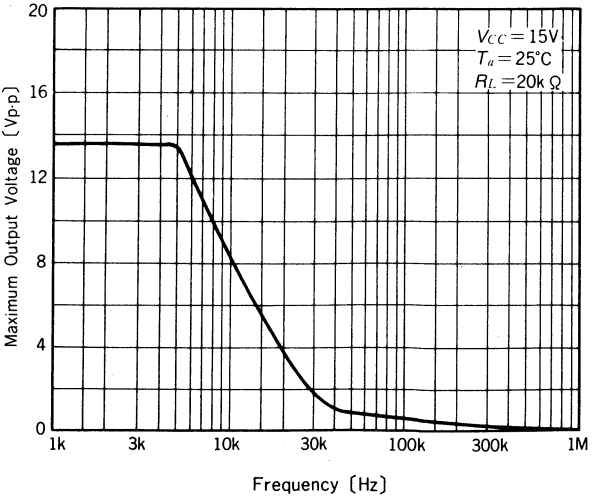
Input Bias Current vs Supply Voltage



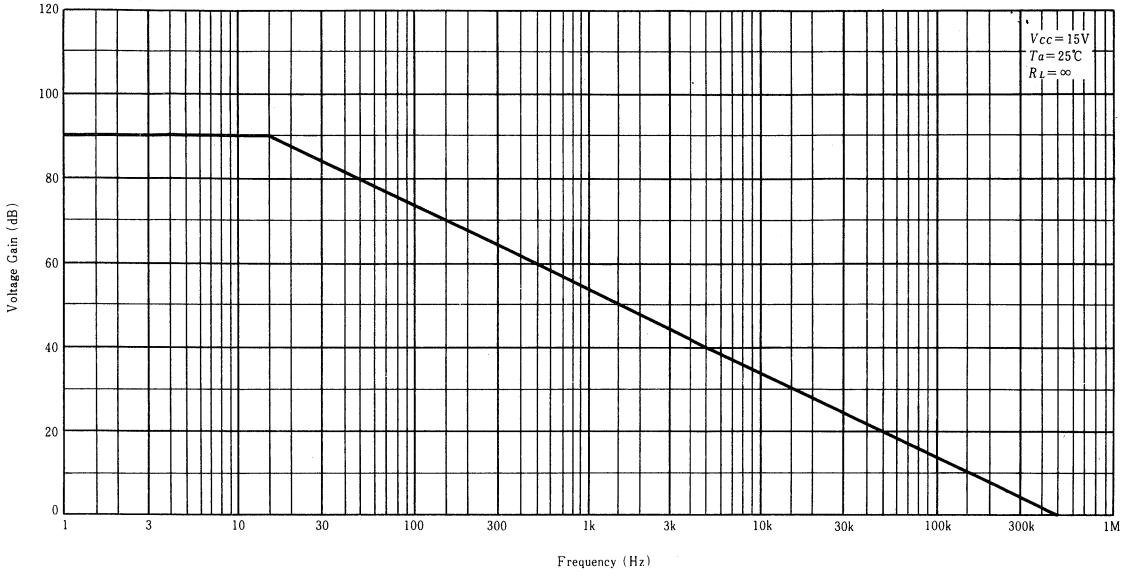
Voltage Gain vs Supply Voltage



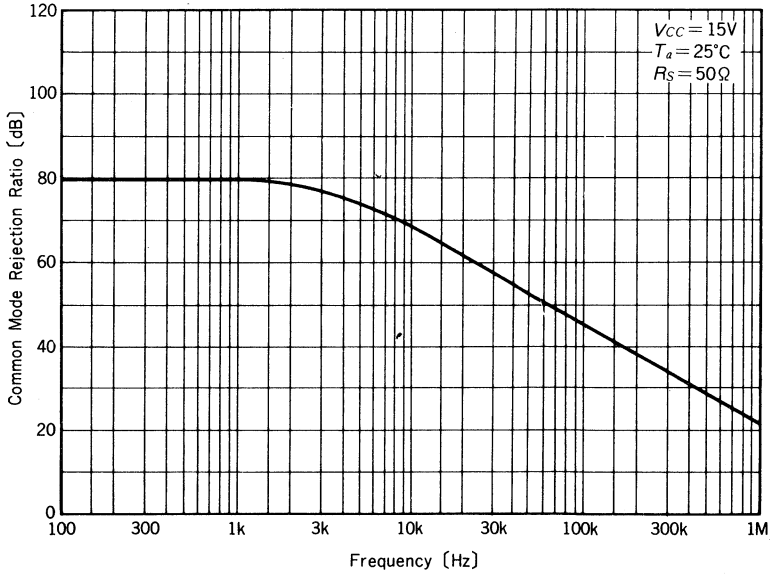
Maximum Output Voltage vs Frequency



Voltage Gain vs Frequency



Common Mode Rejection Ratio vs Frequency



HA17358, HA17904 Series ●Dual Operational Amplifier

HA17904, HA17358 are dual operational amplifiers, which provide internal phase compensation and high gain, and mono power source operation is possible. It can be widely applied to control equipment and to general use.

Industrial Use HA17904GS, HA17904PS
Commercial Use HA17358

HA17904GS

(DG-8)

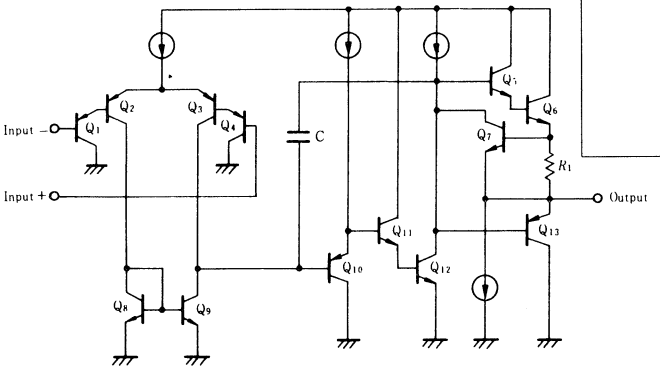
HA17904PS
HA17358

(DP-8)

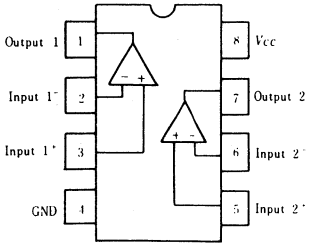
■ FEATURES

- Wide Range of Operating Supply Voltage and Mono Power Source Operation is possible.
- Wide range of Common Mode Input Voltage. Possible to operate with an input around 0V, and output around 0V is available.
- Frequency Characteristics and Input Bias Current are temperature compensated.

■ CIRCUIT SCHEMATIC (1/2)



■ PIN ARRANGEMENT



(Top View)

■ ABSOLUTE MAXIMUM RATINGS (Ta=25°C)

Item	Symbol	HA17904GS	HA17904PS	HA17358	Unit
Supply Voltage	V_{CC}	32	32	32	V
Output Sink Current	I_{sink}	50	50	50	mA
Power Dissipation	P_T	570*	570**	570**	mW
Common Mode Input Voltage	V_{CM}	−0.3 to V_{CC}	−0.3 to V_{CC}	−0.3 to V_{CC}	V
Differential Input Voltage	$V_{in(diff)}$	±V_{CC}	±V_{CC}	±V_{CC}	V
Operating Temperature	T_{opr}	−40 to +85	−20 to +75	0 to +70	°C
Storage Temperature	T_{stg}	−65 to +150	−55 to +125	−55 to +125	°C

* Value at $Ta \leqq 75$°C. In case of more than it, 7.6mW/°C derating shall be done in HA17904GS.
** Value at $Ta \leqq 55$°C. In case of more than it, 8.3mW/°C derating shall be done in HA17904PS and HA17358.

■ ELECTRICAL CHARACTERISTICS (V_{CC}=15V, Ta=25°C)

Item	Symbol	Test Condition	min	typ	max	Unit
Input Offset Voltage	V_{IO}	V_{CM}=7.5V, R_S=50Ω, R_L=50kΩ	—	3	7	mV
Input Offset Current	I_{IO}	V_{CM}=7.5V, I_{IO}=| $I_{I(+)}-I_{I(-)}$ |	—	5	50	nA
Input Bias Current	I_I	V_{CM}=7.5V	—	30	250	nA
Power Source Rejection Ratio	$PSRR$	f=100Hz, R_S=1kΩ, R_f=100kΩ	—	93	—	dB
Voltage Gain	A_{VD}	R_L=∞, R_S=1kΩ, R_f=100kΩ	75	90	—	dB
Common Mode Rejection Ratio	CMR	R_S=50Ω, R_f=5kΩ	—	80	—	dB
Common Mode Input Voltage Range	$V_{CM(+)}$	R_S=1kΩ, R_f=100kΩ	13.5	—	—	V
	$V_{CM(-)}$	R_S=1kΩ, R_f=100kΩ	—	—	−0.3	V
Peak-to-peak Output Voltage	V_{op-p}	f=100Hz, R_L=20kΩ, R_S=1kΩ, R_f=100kΩ	—	13.6	—	V
Output Source Current	I_{source}	V_{IN}^+=1V, V_{IN}^-=0V, V_{OH}=10V	20	40	—	mA
Output Sink Current	I_{sink}	V_{IN}^-=1V, V_{IN}^+=0V, V_{OL}=2.5V	10	20	—	mA
Output Sink Current	I_{sink}	V_{IN}^-=1V, V_{IN}^+=0V, V_{out}=200mV	15	50	—	μA
Supply Current	I_{CC}	V_{IN}=GND, R_L=∞	—	0.8	2	mA
Power Dissipation at no Load	P_T	R_L=∞, V_{IN}=GND	—	12	30	mW
Slew Rate	SR	R_L=∞, V_{CM}=7.5V, f=1.5kHz	—	0.2	—	V/μs
Channel Separation	CS	f=1kHz	—	120	—	dB

Note) As for the characteristic curve, refer to HA17902.

HA17458 Series ● Dual Operational Amplifier

HA17458 is a dual operational amplifier which provides internal phase compensation and high performance. It can be applied widely to measuring control equipment and to general use.

Industrial Use HA17458GS, HA17458PS
Commercial Use HA17458

■ FEATURES

- High Voltage Gain . . . . . 100dB (typ)
- Wide Output Amplitude . . . ±13V (typ) [at $R_L \geqq 2k\Omega$]
- Protected from output shortcircuit
- Internal Phase Compensation

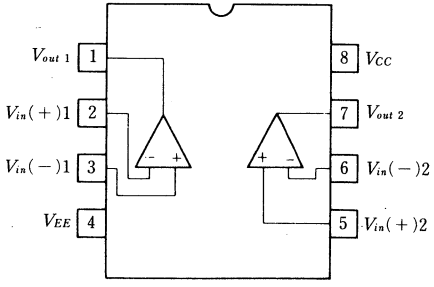
HA17458GS

(DG-8)

HA17458PS
HA17458

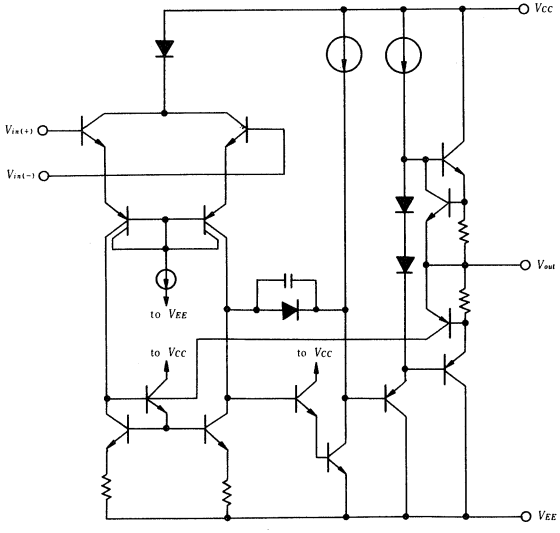
(DP-8)

■ PIN ARRANGEMENT



(Top View)

■ CIRCUIT SCHEMATIC(1/2)



■ ABSOLUTE MAXIMUM RATINGS (Ta=25°C)

Item	Symbol	HA17458GS	HA17458PS	HA17458	Unit
Supply Voltage	V_{CC}	+18	+18	+18	V
	V_{EE}	−18	−18	−18	V
Power Dissipation	P_T	670*	670**	670**	mW
Input Voltage	V_{in}***	±15	±15	±15	V
Differential Input Voltage	$V_{in(diff)}$	±30	±30	±30	V
Operating Temperature	T_{opr}	−20 to +75	−20 to +75	0 to +70	°C
Storage Temperature	T_{stg}	−65 to +150	−55 to +125	−55 to +125	°C

* Value under Ta≦65°C. In case of more than it, 7.6mW/°C derating shall be done.
** Value under Ta≦45°C. In case of more than it. 8.3mW/°C derating shall be done.
***If the Supply voltage is less than ±15V, input voltage shall be less than supply voltage.

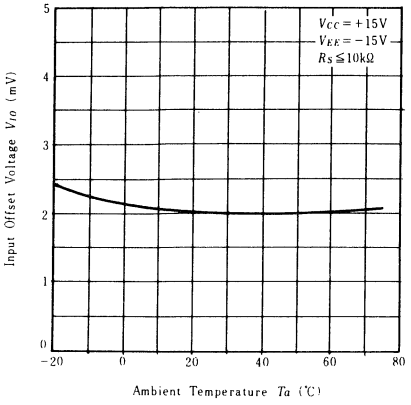
■ ELECTRICAL CHARACTERISTICS-1 (V_{CC}= −V_{EE}=15V, Ta=25°C)

Item	Symbol	Test Condition	min	typ	max	Unit
Input Offset Voltage	V_{IO}	R_s≦10kΩ	−	2.0	6.0	mV
Input Offset Current	I_{IO}		−	6	200	nA
Input Bias Current	I_I		−	30	500	nA
Line Regulation	$\triangle V_{IO}/\triangle V_{CC}$	R_s≦10kΩ	−	30	150	μV/V
	$\triangle V_{IO}/\triangle V_{EE}$	R_s≦10kΩ	−	30	150	μV/V
Voltage Gain	A_{VD}	R_L≧2kΩ, V_{out}=±10V	86	100	−	dB
Common Mode Rejection Ratio	CMR	R_s≦10kΩ	70	90	−	dB
Common Mode Input Voltage Range	V_{CM}		±12	±13	−	V
Peak-to-peak Output Voltage	$V_{op\ p}$	R_L=10kΩ	±12	±14	−	V
Power Dissipation	P_T	No load, 2 channel	−	90	200	mW
Slew Rate	SR	A_v=1	−	0.6	−	V/μs
Input Resistance	R_{in}		0.3	1.0	−	MΩ
Input Capacitance	C_{in}		−	6.0	−	pF
Output Resistance	R_{out}		−	75	−	Ω

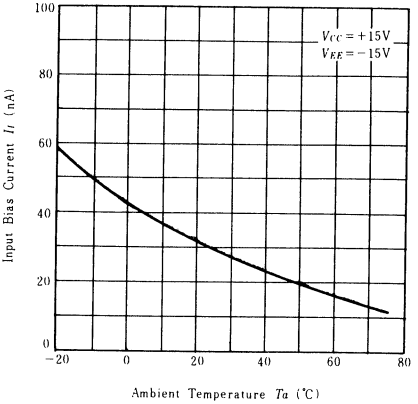
■ ELECTRICAL CHARACTERISTICS-2 (V_{CC}= −V_{EE}=15V, Ta= −20 to +75°C, For HA17458, Ta=0 to +70°C)

Item	Symbol	Test Condition	min	typ	max	Unit
Input Offset Voltage	V_{IO}	R_s≦10kΩ	−	−	9.0	mV
Input Offset Current	I_{IO}		−	−	400	nA
Input Bias Current	I_I		−	−	1100	nA
Voltage Gain	A_{VD}	R_L≧2kΩ, V_{out}=±10V	80	−	−	dB
Peak-to-peak Output Voltage	$V_{op\ p}$	R_L=2kΩ	±10	±13	−	V

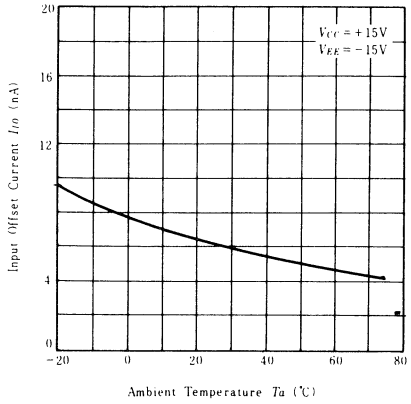
INPUT OFFSET VOLTAGE VS. AMBIENT TEMPERATURE



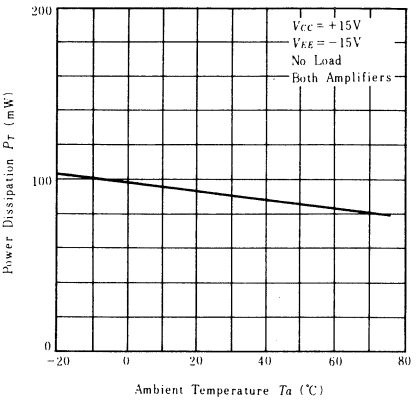
INPUT BIAS CURRENT VS. AMBIENT TEMPERATURE



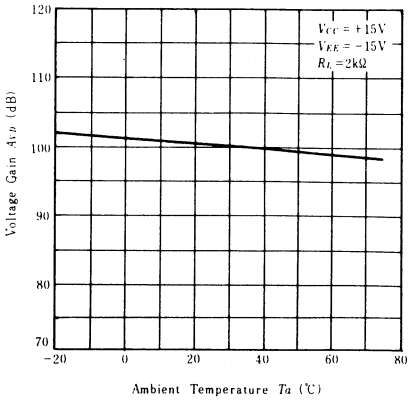
INPUT OFFSET CURRENT VS. AMBIENT TEMPERATURE



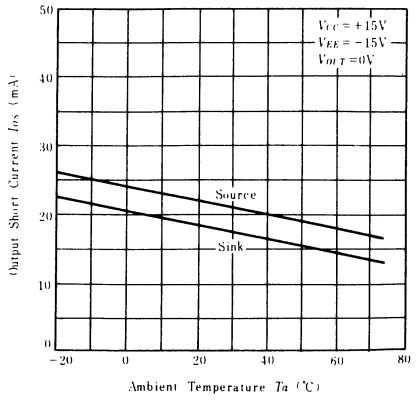
POWER DISSIPATION VS. AMBIENT TEMPERATURE



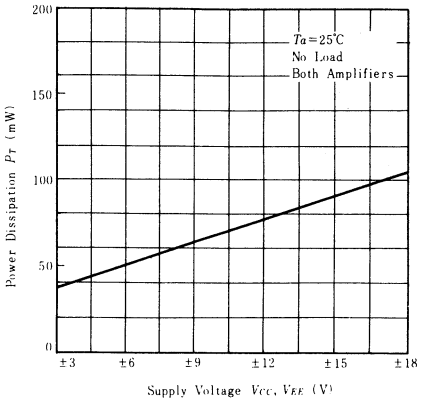
VOLTAGE GAIN VS. AMBIENT TEMPERATURE



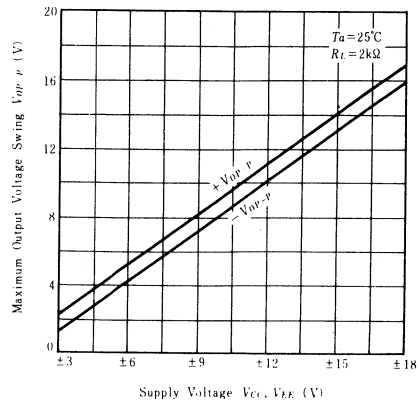
OUTPUT SHORT CURRENT VS. AMBIENT TEMPERATURE



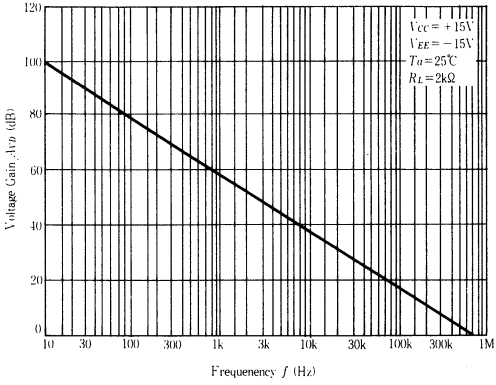
POWER DISSIPATION VS. SUPPLY VOLTAGE



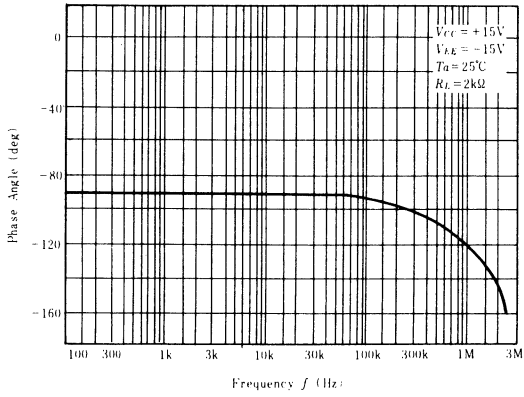
MAXIMUM OUTPUT VOLTAGE SWING VS. SUPPLY VOLTAGE



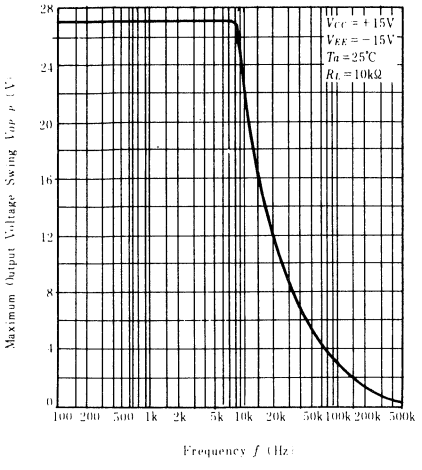
VOLTAGE GAIN VS. FREQUENCY



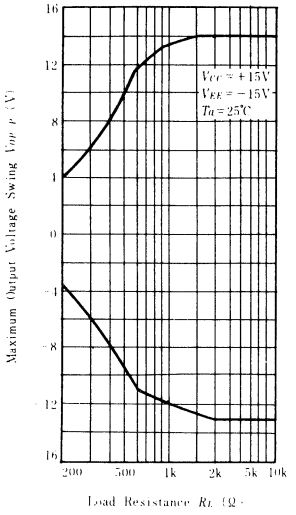
PHASE ANGLE VS. FREQUENCY



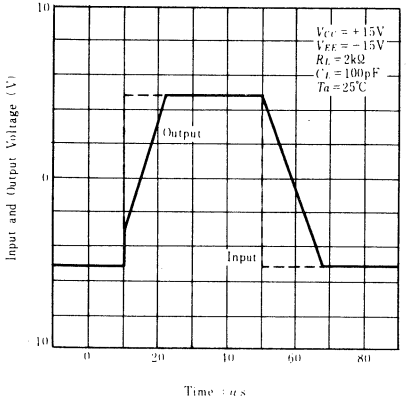
MAXIMUM OUTPUT VOLTAGE SWING VS. FREQUENCY



MAXIMUM OUTPUT VOLTAGE SWING VS. LOAD RESISTANCE



VOLTAGE FOLLOWER LARGE SIGNAL PULSE RESPONSE



HA17474 Series ●Quad Operational Amplifier —Preliminary—

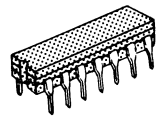
HA17474 is a quad operational amplifier with provides internal frequency compensation and high performance. If can be applied widely to measuring control equipment and to general use.

- Industrial Use . HA17474G, HA17474P
- Commercial Use HA17474

■ FEATURES

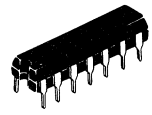
- High Speed . . 1.9V/μs
- Continuous Short-circuit Protection
- Low-noise
- Internal Frequency Compensation

HA17474G



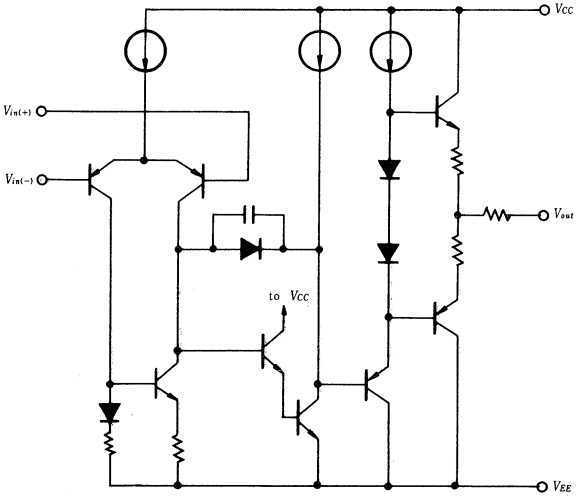
(DG-14)

HA17474P
HA17474

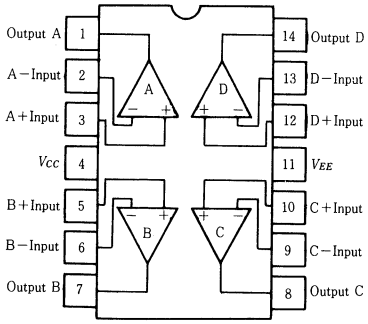


(DP-14)

■CIRCUIT SCHEMATIC (1/4)



■PIN ARRANGEMENT



(Top View)

■ABSOLUTE MAXIMUM RATINGS (T_a=25°C)

Item	Symbol	HA17474G	HA17474P	HA17474	Unit	Note
Power Supply	V_{CC}	+20	+20	+20	V	
	V_{EE}	−20	−20	−20	V	
Power Dissipation	P_T	750*	750**	750**	mW	2
Common-mode Differential Voltage	$V_{in(diff)}$	±30	±30	±30	V	
Common-mode Input Voltage	V_{CM}	±15	±15	±15	V	1
Operating Temperature Range	T_{opr}	−20~+75	−20~+75	0~+70	°C	
Storage Temperature Range	T_{stg}	−65~+150	−55~+125	−55~+125	°C	

Note 1) For supply voltage less than ±15V, the absolute maximum input voltage is equal to the supply voltage.
2) * Value under $T_a \leqq 65$°C. In case of more than it, 7.6mW/°C derating shall be done.
** Value under $T_a \leqq 45$°C. In case of more than it, 8.3mW/°C derating shall be done.

■ELECTRICAL CHARACTERISTICS (T_a=25°C, V_{CC}=+15V, V_{EE}=−15V)

Item	Symbol	Test Condition	min	typ	max	Unit
Input Offset Voltage	V_{IO}	$R_S \leqq 10$kΩ	−	1.0	5.0	mV
Input Offset Current	I_{IO}		−	30	50	nA
Input Bias Current	I_{IS}		−	100	300	nA
Voltage Gain	A_V	$R_L \geqq 2$kΩ, V_O=±10V	88	94	−	dB
Maximum Output Voltage	$V_{op\text{-}p}$	$R_L \geqq 10$kΩ	±12	±13.7	−	V
		$R_L \geqq 2$kΩ	±10	±12.5	−	V
Common-mode Input Voltage Range	V_{CM}		±12	±14	−	V
Common-mode Rejection Ratio	CMR	$R_S \leqq 10$kΩ	80	90	−	dB
Supply Voltage Rejection Ratio	SVR	$R_S \leqq 10$kΩ	−	50	100	μV/V
Power Dissipation	P_T	4-channel, No Load	−	150	210	mW
Slew Rate	SR	A_V=1	−	1.9	−	V/μs
Equivalent Input Noise Voltage	V_{NI}	R_S=1kΩ, f=1Hz~1kHz	−	9	−	nV/√Hz
Channel Separation	CS	f=1kHz	−	108	−	dB

HA17558 Series ● Dual Operational Amplifier

HA17558 is a dual operational amplifier which provides internal frequency compensation and high performance. It can be applied widely to measuring control equipment and to general use. The two amplifiers share a common bias network and power supply leads.

Industrial Use HA17558GS, HA17558PS
Commercial Use HA17558

HA17558GS

(DG-8)

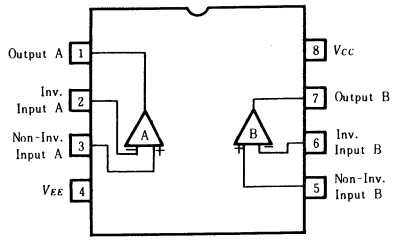
HA17558PS
HA17558

(DP-8)

■FEATURES

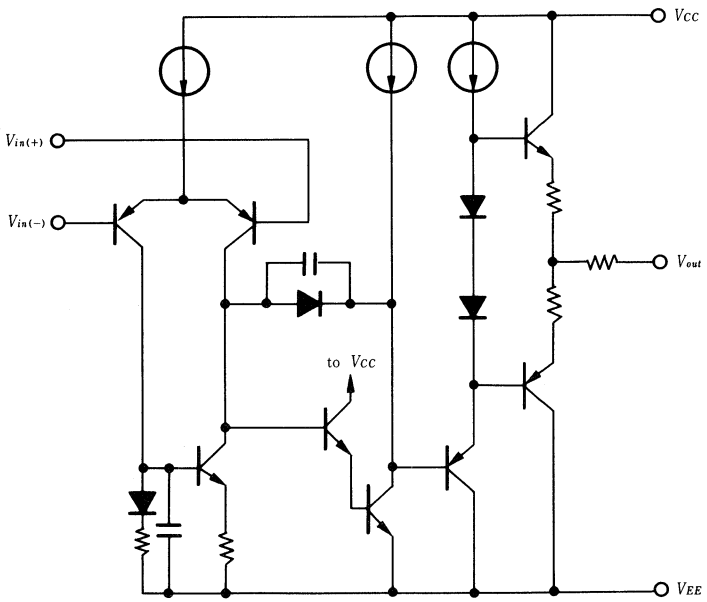
- High Voltage Gain . . . . . 104dB (typ)
- High Speed 1V/μs
- Continuous Short-circuit Protection
- Low-noise operational amplifiers
- Internal Frequency Compensation

■PIN ARRANGEMENT



(Top View)

■CIRCUIT SCHEMATIC (1/2)



■ABSOLUTE MAXIMUM RATINGS (Ta=25°C)

Item	Symbol	HA17558	HA17558PS	HA17558GS	Unit	Note
Power Supply	V_{CC}	+18	+18	+18	V	
	V_{EE}	−18	−18	−18	V	
Common-mode Differential Voltage	$V_{in(diff)}$	±30	±30	±30	V	
Common-mode Input Voltage	V_{CM}	±15	±15	±15	V	1
Power Dissipation	P_T	670*	670**	670**	mW	2
Operating Temperature Range	T_{opr}	0～+70	−20～+75	−20～+75	°C	
Storage Temperature Range	T_{stg}	−55～+125	−55～+125	−65～+150	°C	

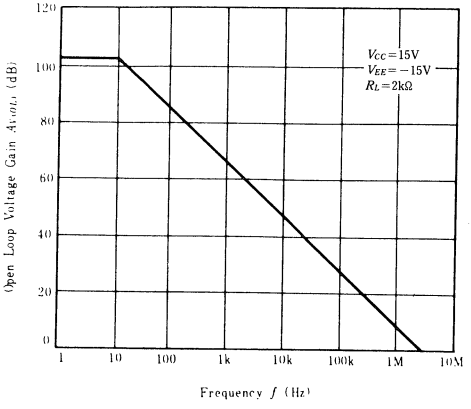
Note 1.) For supply voltage less than ±15V, the absolute maximum input voltage is equal to the supply voltage.
Note 2.) * Value under $Ta \leqq 65$°C. In case of more than it, 7.6mW/°C. derating shall be done.
** Value under $Ta \leqq 45$°C. In case of more than it, 8.3mW/°C. derating shall be done.

■ELECTRICAL CHARACTERISTICS (Ta=25°C, V_{CC}=+15V, V_{EE}=−15V)

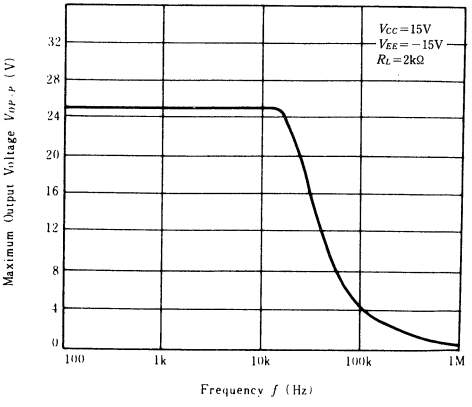
Test Item	Symbol	Test Conditions	min	typ	max	Unit
Input Offset Voltage	V_{IO}	$R_s \leqq 10k\Omega$	—	0.5	6	mV
Input Offset Current	I_{IO}		—	5	200	nA
Input Bias Current	I_{IB}		—	50	500	nA
Voltage Gain	A_v	$R_L \geqq 2k\Omega$, $V_o = \pm 10V$	86	104	—	dB
Maximum Output Voltage	V_{OP-P}	$R_L \geqq 10k\Omega$	±12	±14	—	V
Maximum Output Voltage	V_{OP-P}	$R_L \geqq 2k\Omega$	±10	±12.4	—	V
Common-mode Input Voltage Range	V_{CM}		±12	±14	—	V
Common-mode Rejection Ratio	CMR	$R_s \leqq 10k\Omega$	70	100	—	dB
Supply Voltage Rejection Ratio	SVR	$R_s \leqq 10k\Omega$	—	110	150	μV/V
Power Dissipation	P_T	2-channel, No Load	—	90	170	mW
Slew Rate	SR	$A_v = 1$	—	1.0	—	V/μs
Equivalent Input Noise Voltage	V_{NI}	$R_s = 1k\Omega$	—	6	—	μVp-p
Channel Separation	CS	f = 1kHz	—	105	—	dB

■TYPICAL PERFORMANCE CHARACTERISTICS (Ta=25°C)

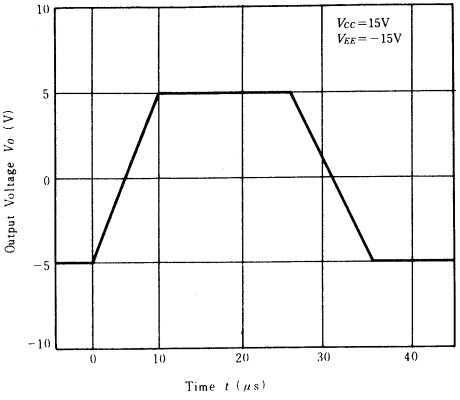
OPEN LOOP VOLTAGE GAIN VS. FREQUENCY



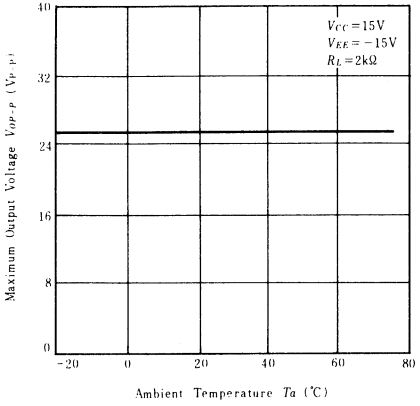
MAXIMUM OUTPUT VOLTAGE VS. FREQUENCY



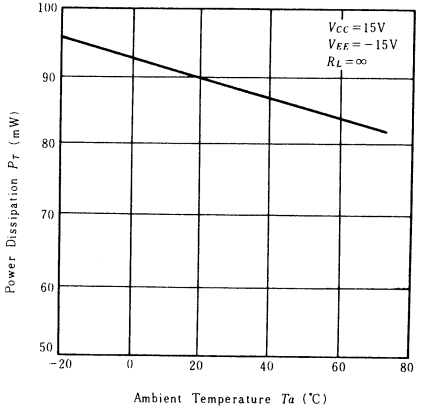
TRANSIENT RESPONSE



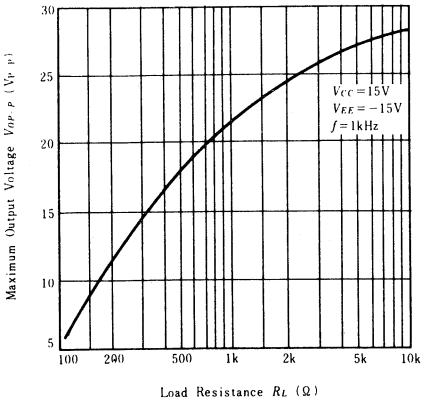
MAXIMUM OUTPUT VOLTAGE VS. AMBIENT TEMPERATURE



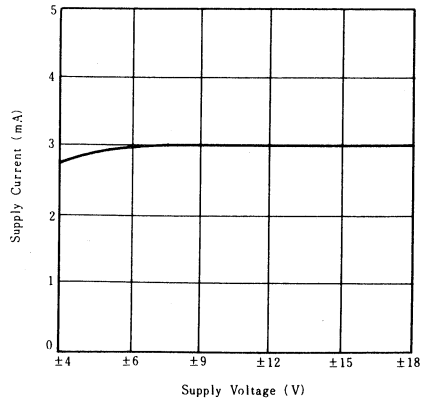
POWER DISSIPATION VS. AMBIENT TEMPERATURE



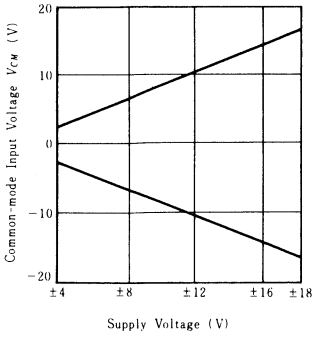
MAXIMUM OUTPUT VOLTAGE VS. LOAD RESISTANCE



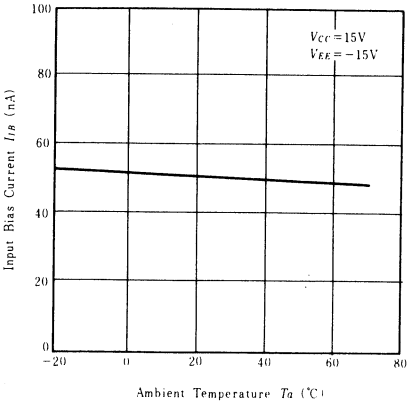
SUPPLY CURRENT VS. SUPPLY VOLTAGE



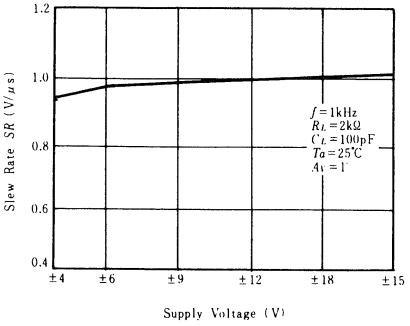
COMMON-MODE INPUT VOLTAGE VS. SUPPLY VOLTAGE



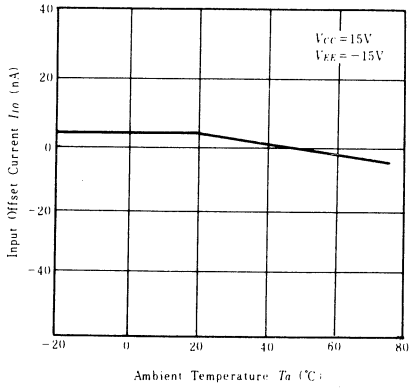
INPUT BIAS CURRENT VS. AMBIENT TEMPERATURE



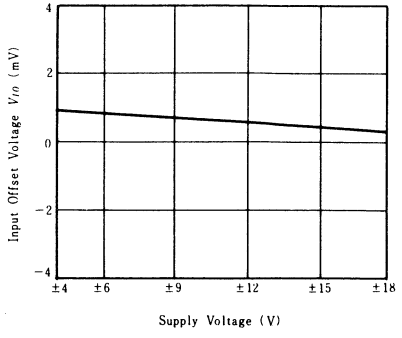
SLEW RATE VS. SUPPLY VOLTAGE



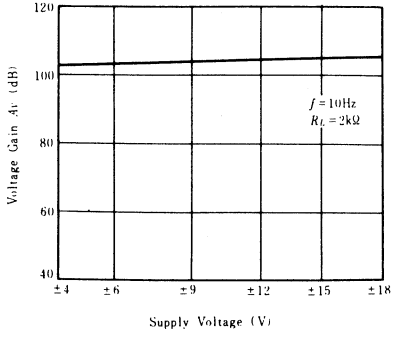
INPUT OFFSET CURRENT VS. AMBIENT TEMPERATURE



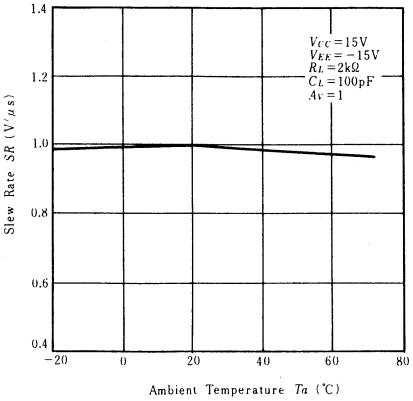
INPUT OFFSET VOLTAGE VS. SUPPLY VOLTAGE



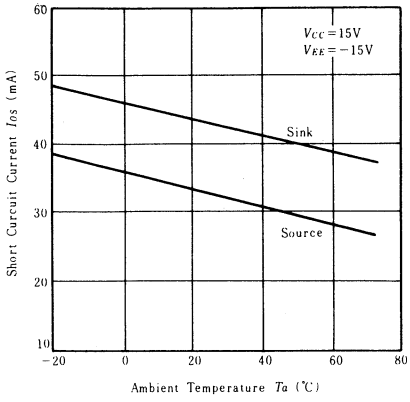
VOLTAGE GAIN VS. SUPPLY VOLTAGE



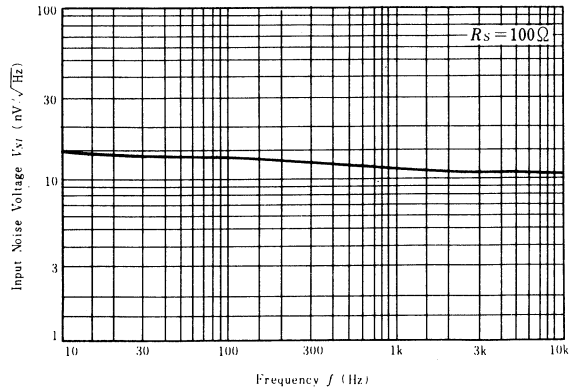
SLEW RATE VS. AMBIENT TEMPERATURE



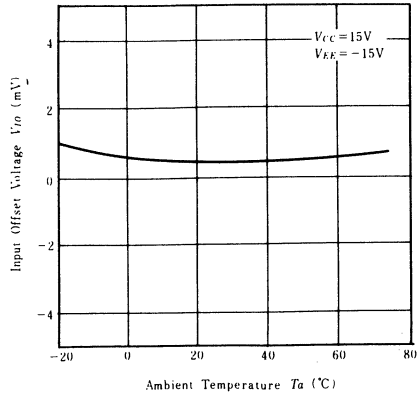
SHORT CIRCUIT CURRENT VS. AMBIENT TEMPERATURE



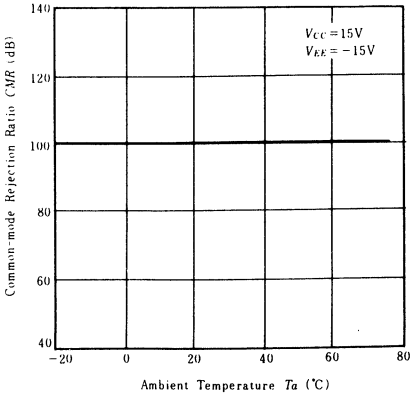
INPUT NOISE VOLTAGE VS. FREQUENCY



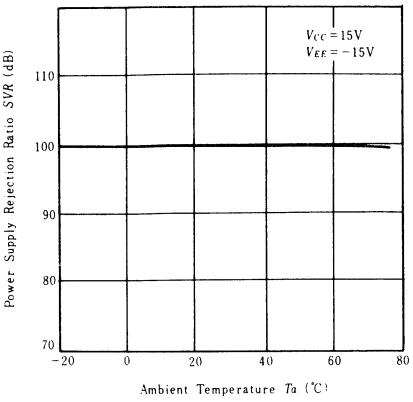
INPUT OFFSET VOLTAGE VS. AMBIENT TEMPERATURE



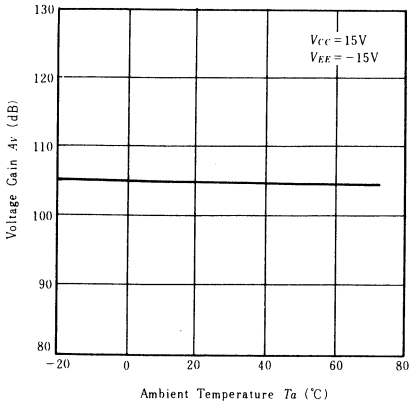
COMMON-MODE REJECTION RATIO VS. AMBIENT TEMPERATURE



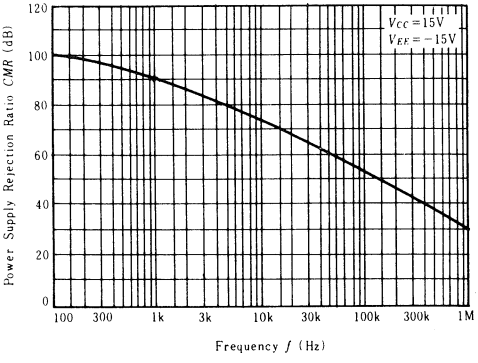
POWER SUPPLY REJECTION RATIO VS. AMBIENT TEMPERATURE



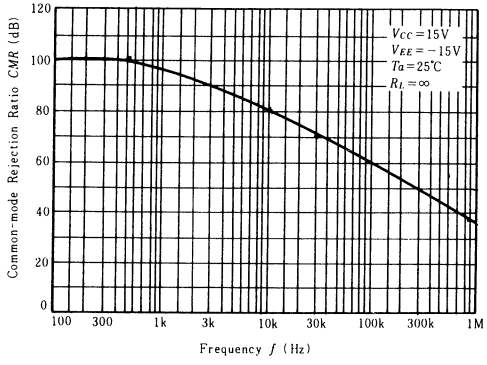
VOLTAGE GAIN VS. AMBIENT TEMPERATURE



POWER SUPPLY REJECTION RATIO VS. FREQUENCY

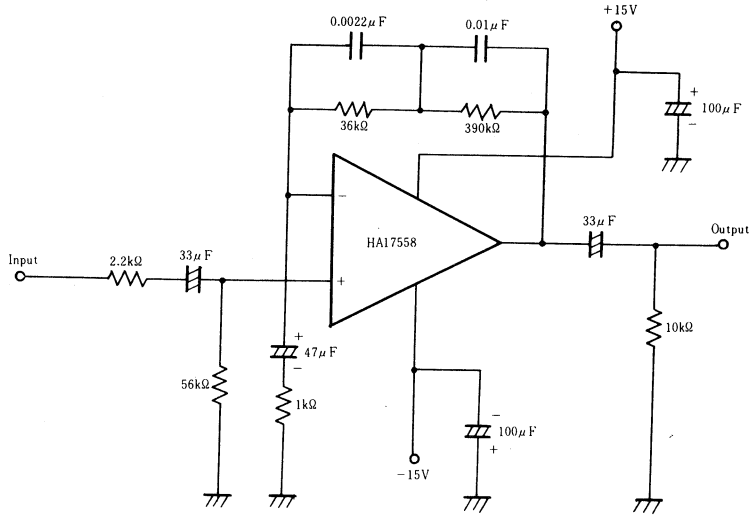


COMMON-MODE REJECTION RATIO VS. FREQUENCY

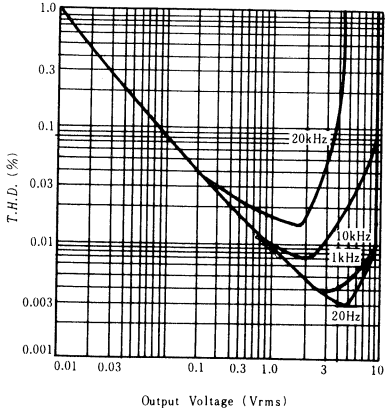


■ CIRCUIT EXAMPLE

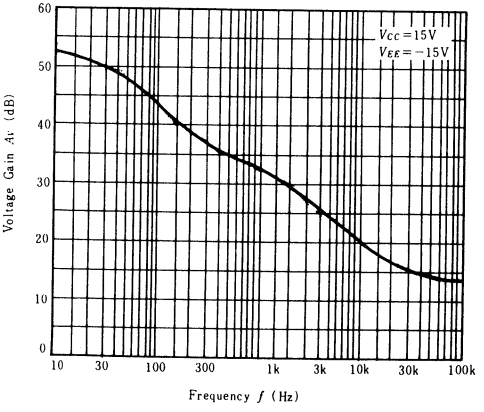
RIAA PRE-AMPLIFIER



T.H.D. VS. OUTPUT VOLTAGE (RIAA PRE-AMP.)

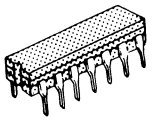


VOLTAGE GAIN VS. FREQUENCY (RIAA PRE-AMP.)



HA17715G ● High Slew Rate Operational Amplifier

HA17715 is an operational amplifier of high speed and high gain, and it's application is possible in A/D, D/A converter, active filter, wide band width amplifier, comparator, sample hold circuit, and general feedback circuit required wide band width from DC.

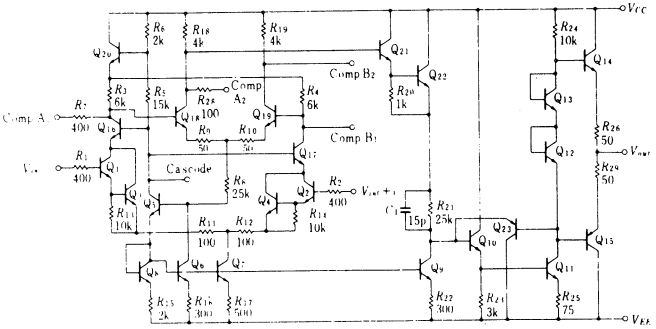


(DG-14)

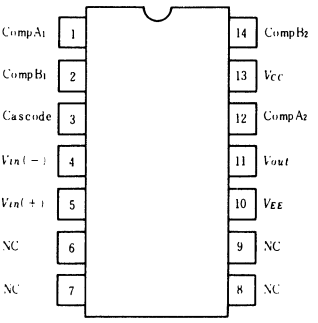
■ FEATURES

- Slew Rate 100V/μs (typ)
- Fast Settling Time 300 ns (typ)
- Wide Band Width 65MHz (typ)

■ CIRCUIT SCHEMAITIC



■ PIN ARRANGEMENT



(Top View)

■ ABSOLUTE MAXIMUM RATINGS ($Ta = 25°C$)

Item	Symbol	HA17715G	Unit
Supply Voltage	V_{CC}	+18	V
Supply Voltage	V_{EE}	−18	V
Power Dissipation	P_T**	625	mW
Common Mode Input Voltage	V_{CM}*	±15	V
Differential Input Voltage	$V_{in\ diff}$	±15	V
Operating Temperature	T_{opr}	−20 to +75	°C
Storage Temperature	T_{stg}	−65 to +150	°C

*If supply voltage is less than ±15V, input voltage is to supply voltage.
**It's a permissible value to $Ta = 70°C$, and beyond that, derate with 7.6mW/°C

■ ELECTRICAL CHARACTERISTICS-1 ($V_{CC} = -V_{EE} = 15V$, $Ta = 25°C$)

Item	Symbol	Measuring Condition	min	typ	max	Unit
Input Offset Voltage	V_{IO}	$R_S \leqq 10k\Omega$	–	2.0	7.5	mV
Input Offset Current	I_{IO}		–	70	250	nA
Input Bias Current	I_I		–	0.4	1.5	μA
Line Reguration	$\triangle V_{IO}/\triangle V_{CC}$ $\triangle V_{IO}/\triangle V_{EE}$	$R_S \leqq 10k\Omega$	–	45	400	μV/V
Voltage Gain	A_{VD}	$R_L \leqq 2k\Omega$, $V_{out} = \pm 10V$	10000	30000	–	V/V
Common Mode Rejection Ratio	CMR	$R_S \leqq 10k\Omega$	74	92	–	V
Common Mode Input Voltage Range	V_{CM}		±10	±12	–	V
Supply Current	I_{CC}		–	5.5	10	mA

HITACHI

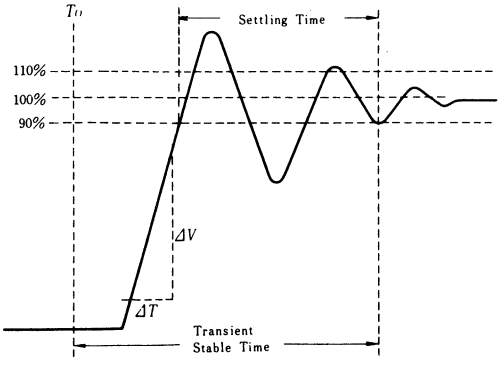
■ ELECTRICAL CHARACTERISTICS-1 (Continued)

Item	Symbol	Measuring Condition	min	typ	max	Uuit
Power Dissipation	P_T		—	165	300	mW
Band Width	BW	$A_{VD}=1$	—	65	—	MHz
Slew Rate	SR	$A_{CL}=100$	—	70	—	V/μs
		$A_{CL}=10$	—	38	—	V/μs
		$A_{CL}=1$(positive phase)	10	18	—	V/μs
		$A_{CL}=1$(negeative phase)	—	100	—	V/μs
Transient Stable Time	t_{ACO}	$V_{out}=5V$, $A_{CL}=1$	—	800	—	ns
Settling Time	t_{STL}	$A_{CL}=1$	—	300	—	ns
Rise Time	t_r	$V_{in}=400mV$, $A_{CL}=1$	—	30	75	ns
Overshoot	V_{over}	$V_{in}=400mV$, $A_{CL}=1$	—	25	50	%
Input Resistance	R_{in}		—	1.0	—	MΩ
Output Resistance	R_{out}		—	75	—	Ω
Temperature Drift	$\triangle V_{IO}/\triangle T$		—	6	—	μV/℃

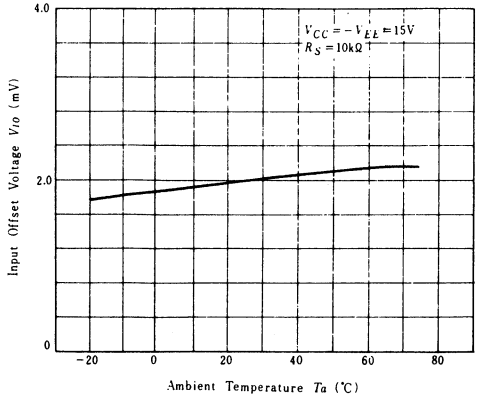
■ ELECTRICAL CHARACTERISTICS-2 ($V_{CC}=-V_{EE}=15V$, $Ta=-20$ to $+75℃$)

Item	Symbol	Measuring Condition	min	typ	max	Unit
Input Offset Voltage	V_{IO}	$R_S\leqq 10k\Omega$	—	—	10	mV
Input Offset Current	I_{IO}	$Ta=75℃$	—	—	250	nA
		$Ta=-20℃$	—	—	750	nA
Input Bias Current	I_I	$Ta=75℃$	—	—	1.5	μA
		$Ta=0℃$	—	—	7.5	μA
		$Ta=-20℃$	—	—	10	μA
Voltage Gain	A_{VD}	$R_L\geqq 2k\Omega$, $V_{out}=\pm 10V$	7000	—	—	V/V
Peak To Peak Output Voltage Amplitude	$V_{OP\ P}$	$R_L\geqq 2k\Omega$	±10	±13	—	V

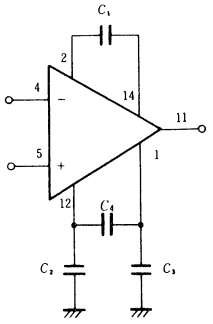
DEFINITION OF TRANSIENT RESPONSE WAVEFORM



INPUT OFFSET VOLTAGE VS. AMBIENT TEMPERTURE



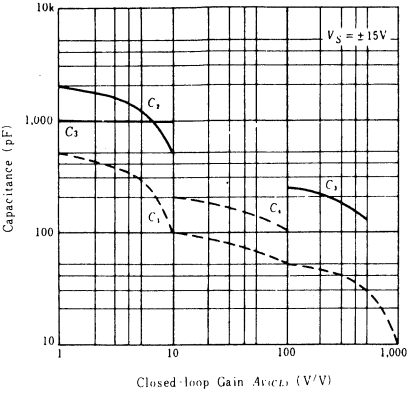
PHASE COMPENSATED CIRCUIT



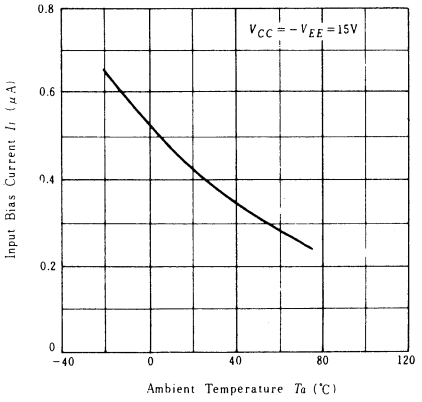
CAPACITANCE VALUE FOR PHASE COMPENSATION

Closed Loop Gain	C_1	C_2	C_3
1000	10pF	—	—
100	50pF	—	250pF
10	100pF	500pF	1000pF
1	500pF	2000pF	1000pF

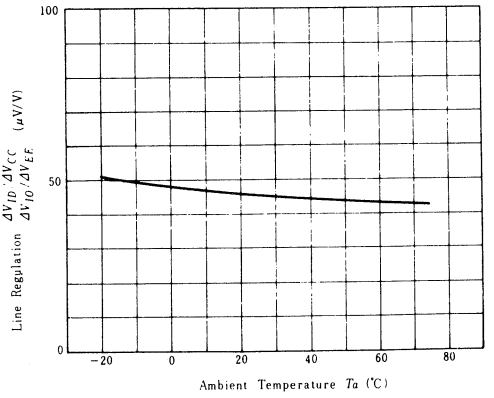
CLOSED LOOP GAIN VS. COMPENSATED CAPACITANCE



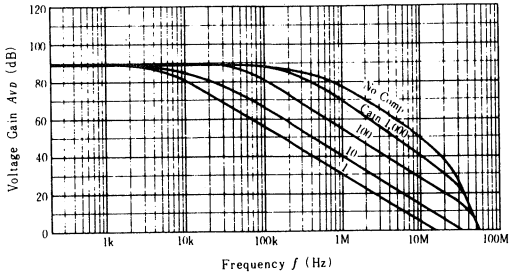
INPUT BIAS CURRENT VS. AMBIENT TEMPERATURE



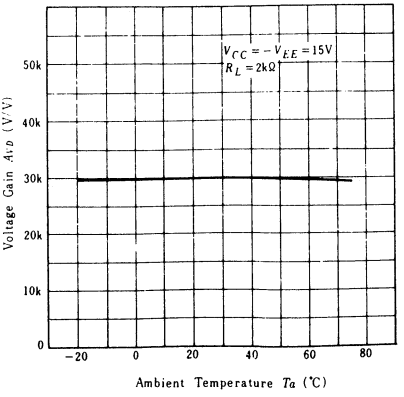
LINE REGULATION VS. AMBIENT TEMPERATURE



VOLTAGE GAIN VS. FREQUENCY



VOLTAGE GAIN VS. AMBIENT TEMPERATURE



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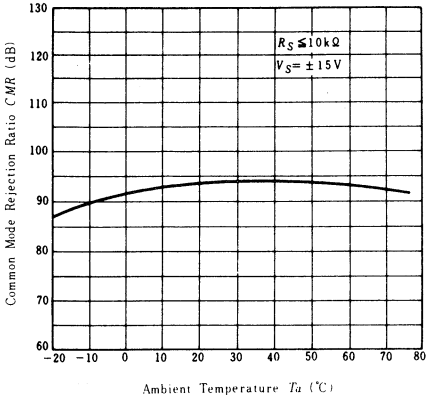
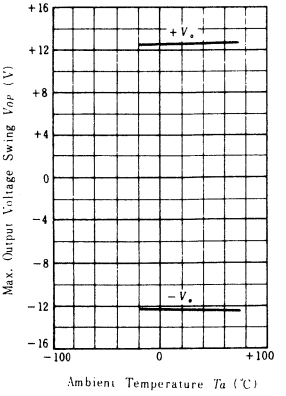
COMMON MODE REJECTION RATIO VS. AMBIENT TEMPERATURE



PEAK TO PEAK OUTPUT VOLTAGE VS. AMBIENT TEMPERATURE



■ AN APPLICATION OF HA17715

HA17715 is an operational amplifier of high slew rate, and is optimum for the application in the field requiring high speed signal processing and wide band width. The following describes an application of HA17715.

1. Fundamental articles for using HA17715

1.1 Method of using phase compensated capacitance

Because HA17715 is high speed and high gain, it is especially necessary to notice the prevention of oscillation at the time of using it. On account of this, capacitance value for phase compensation is being recommended as shown in Fig. 1, satisfying the largeness of closed loop gain for use.

(1) In case voltage gain is 1,

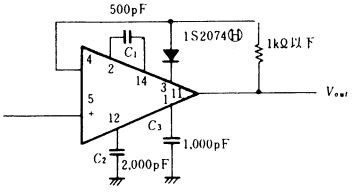


Fig.1 Phase Compensation in case voltage gain is 1

In case of voltage follower, in order not to have latch up occur at input stage even if output is increased, it is necessary to insert diode to cascode terminal as shown in the figure.

(2) In case voltage gain is 10

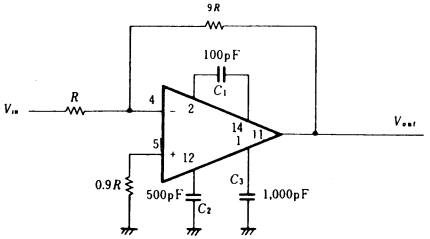


Fig.2 Phase Compensation in case voltage gain is 10

In case voltage gain is 10, it is allowable to insert capacitan of C_4 to between terminal 1 and 12, replacing C_2 and from the above figure. In that case, the value of C_4 is 200p

(3) In case voltage gain is 100

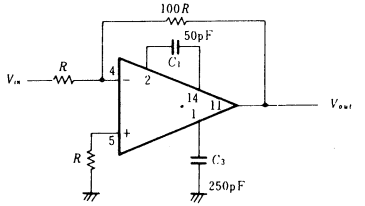


Fig.3 Phase Compensation in case voltage gain is 100

(4) In case voltage gain is 1000

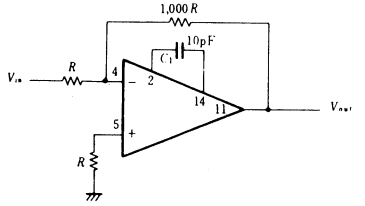


Fig.4 Phase Compensation in case voltage gain is 1000

1.2 Offset Adjustment

The adjustment of voltage offset can be performed by applying volume etc. for offset adjustment use to input terminal. In case of HA17715, it can be performed effectively by using terminals 1 and 2 for phase compensation use to input terminal. In case of HA17715, it can be performed effectively by using terminals 1 and 2 for phase compensation use as shown in Fig. 5

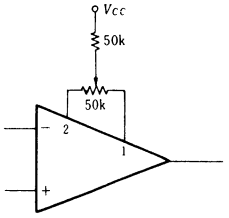


Fig.5 Offset Adjustment of HA17715

2. An application of HA17715

2.1 High Cycle Amplifier

Fig. 6 shows high cycle amplifier with progressed drive ability of output by applying PNP and NPN transistor to HA17715. Voltage Gain A_V of this amplifier can be.

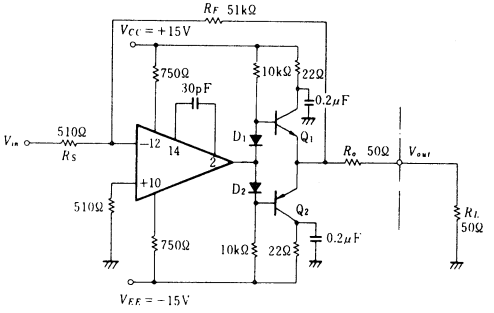


Fig.6 High Frequency Amplifier

expressed by $A_V = 20 \log \frac{R_F}{R_S} - 20 \log \left(1 + \frac{R_O}{R_L}\right)$

Fig. 7 shows frequency characteristic of voltage gain in the circuit of Fig. 6.

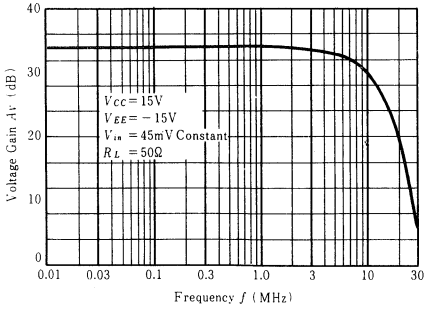


Fig.7 High Frequency Amplifier A_V-f Characteristic

2.2 Wide Band Width Oscillator

Fig. 8 shows oscillation circuit of wien bridge type theoretical equation

$$A_V = 1 + \frac{VR_1}{VR_2} + \frac{C_2}{C_1} = 6$$

$$f = \frac{1}{2\pi} \sqrt{1/(VR_1 \cdot VR_2 \cdot C_1 \cdot C_2)}$$

Table 1. CAPACITIVE VALUE FOR FREQUENCY RANGE

Frequency Range	C_1	C_2
10 to 100Hz	3μF	7.5μF
100 to 1000Hz	0.3μF	0.75μF
1k to 10kHz	0.03μF	0.075μF
10k to 100kHz	0.003μF	0.0075μF
100k to 1000 kHz	300pF + 150Ω	750pF

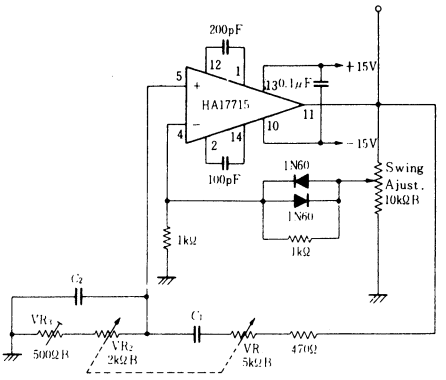


Fig.8 Wide Band Width Oscillator

Note 1. By switching C_1 and C_2, it is capable of oscillating the range of from 10 Hz to 1 MHz by 5 range.

2. As for output amplitude, about 3 Vpp is optimum.

3. The amplitude of each range is stabilized by the fine turning of C_2.

4. By the adjustment of VR_3, uniformalize amplitude change during VR_1, VR_2 changes.

2.3 Waveform Shaping Circuit

Fig. 1 shows Waveform Shaping Circuit of Schmitt Trigger method. At no signal, this circuit becomes Astable Multi, since bias is put to it with the negative feedback type in order to make high cycle waveform shaping good. Fig. 11 shows the relation between minimum identification level and resistance.

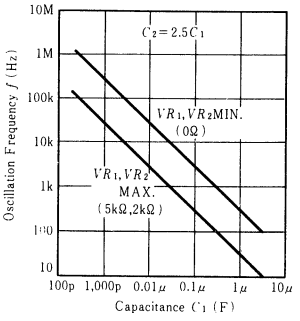


Fig.9 Oscillation Frequency vs Capacitance

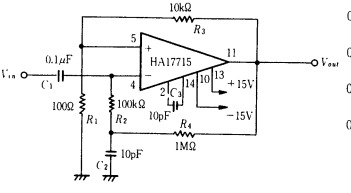


Fig.10 Waveform Shaping(Slice) Circuit Of Schmitt Trigger Method

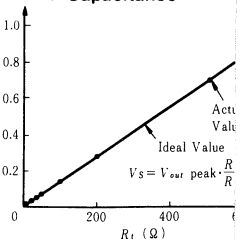


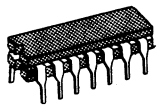
Fig.11 Minimum Identificating Level vs Resistance

HA17741 Series

● General Purpose Operational Amplifier (Frequency Compensated)

HA17741 is internal phase compensated type, high performance operational amplifier. Its application is possible widely in the fields of instrumentation operation use and of general use.

HA17741G



(DG-14)

HA17741GS

(DG-8)

HA17741PS, HA17741

(DP-8)

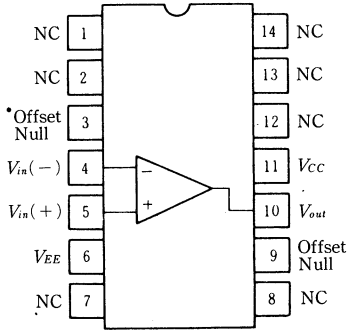
■FEATURES

Industrial use; HA17741G, HA17741GS, HA17741PS
Commercial use; HA17741

- High Voltage Gain 106dB (typ)
- Wide Output Amplitude ±13V (typ) [at $R_L \geqq 2k\Omega$]
- Protected to Output Short
- Capable of adjusting Offset Voltage
- Internal phase compensated type

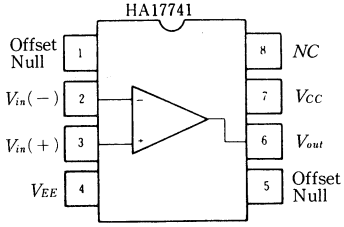
■PIN ARRANGEMENT

HA17741G



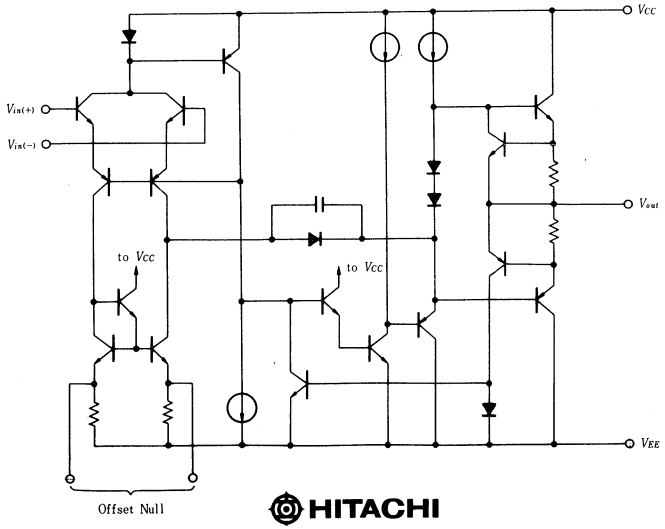
(Top View)

HA17741GS
HA17741PS
HA17741



(Top View)

■CIRCUIT SCHEMATIC



■ ABSOLUTE MAXIMUM RATINGS (Ta=25°C)

Item	Symbol	HA17741G, HA17741GS	HA17741PS	HA17741	Unit
Supply Voltage	V_{CC}	+18	+18	+18	V
	V_{EE}	−18	−18	−18	V
Power Dissipation	P_T	670*	670**	670**	mW
Input Voltage	V_{in}	±15	±15	±15	V
Differential Input Voltage	$V_{in(diff)}$	±30	±30	±30	V
Operating Temperature	T_{opr}	−20 to +75	−20 to +75	0 to +70	°C
Storage Temperature	T_{stg}	−65 to +150	−55 to +125	−55 to +125	°C

* is the permissible value to Ta=65°C, and beyond that, derate with 7.6mW/°C.
** is the permissible value to Ta=45°C, and beyond that, derate with 8.3mW/°C.

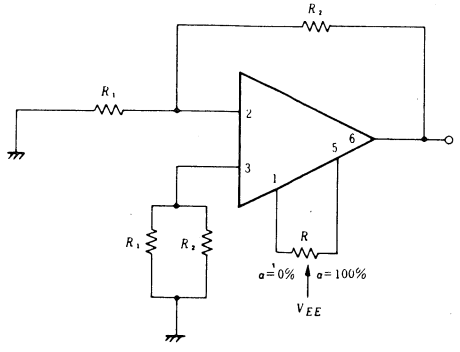
■ ELECTRICAL CHARACTERISTICS−1 (V_{CC}=−V_{EE}=15V, Ta=25°C)

Item	Symbol	Test Condition	min	typ	max	Unit
Input Offset Voltage	V_{IO}	R_S≦10kΩ	—	1.0	6.0	mV
Input Offset Current	I_{IO}		—	18	200	nA
Input Bias Current	I_I		—	75	500	nA
Line Regulation	$\Delta V_{IO}/\Delta V_{CC}$	R_S≦10kΩ	—	30	150	μV/V
	$\Delta V_{IO}/\Delta V_{EE}$	R_S≦10kΩ	—	30	150	μV/V
Voltage Gain	A_{VD}	R_L≧2kΩ, V_{out}=±10V	86	106	—	dB
Common Mode Rejection Ratio	CMR	R_S≦10kΩ	70	90	—	dB
Common Mode Input Voltage Range	V_{CM}	R_S≦10kΩ	±12	±13	—	V
Peak To Peak Output Voltage	V_{OP-P}	R_L≧10kΩ	±12	±14	—	V
	V_{OP-P}	R_L≧2kΩ	±10	±13	—	V
Power Dissipation	P_T	at the time of no load	—	65	100	mW
Slew Rate	SR	R_L≧2kΩ	—	1.0	—	V/μs
Rise Time	t_r	V_{in}=20mV, R_L=2kΩ	—	0.3	—	μs
Overshoot	V_{over}	C_L=100pF	—	5.0	—	%
Input Resistance	R_{in}		0.3	1.0	—	MΩ

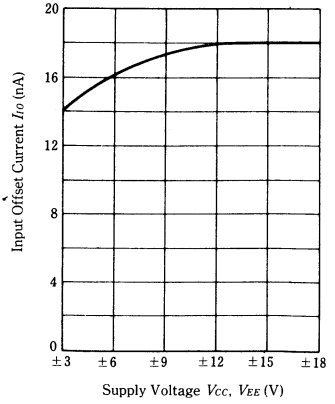
■ ELECTRICAL CHARACTERISTICS−2 (V_{CC}=−V_{EE}=15V, Ta=−20 to +75°C, however as for HA17741, Ta=0 to +70°C)

Item	Symbol	Test Condition	min	typ	max	Unit
Input Offset Voltage	V_{IO}	R_S≦10kΩ	—	—	9.0	mV
Input Offset Current	I_{IO}		—	—	400	nA
Input Bias Current	I_I		—	—	1100	nA
Voltage Gain	A_{VD}	R_L≧2kΩ, V_{out}=±10V	80	—	—	dB
Peak To Peak Output Voltage	V_{OP-P}	R_L≧2kΩ	±10	—	—	V

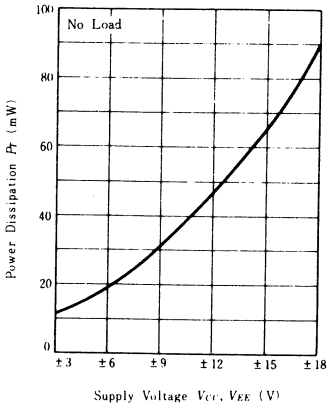
● VOLTAGE OFFSET ADJUSTING CIRCUIT



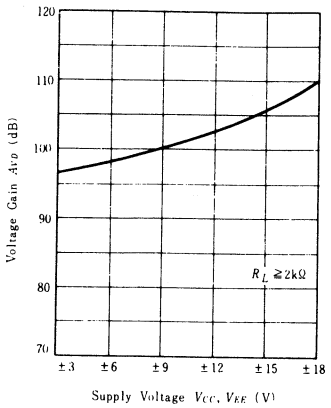
INPUT OFFSET CURRENT VS. SUPPLY VOLTAGE CHARACTERISTIC



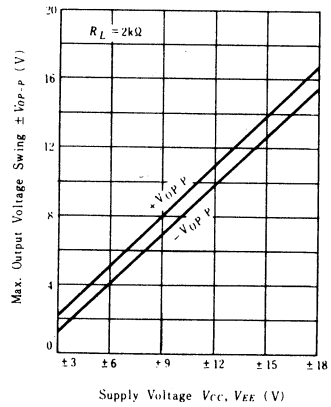
POWER DISSIPATION VS SUPPLY VOLTAGE



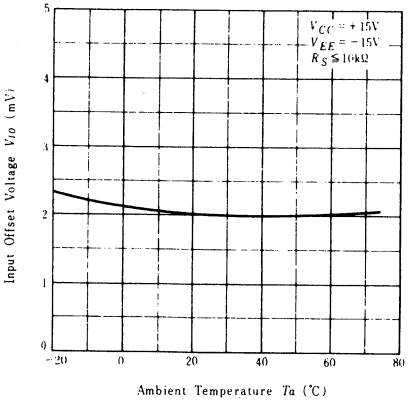
VOLTAGE GAIN VS SUPPLY VOLTAGE



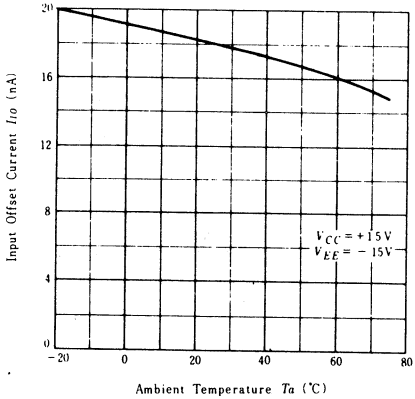
PEAK TO PEAK OUTPUT VOLTAGE VS SUPPLY VOLTAGE



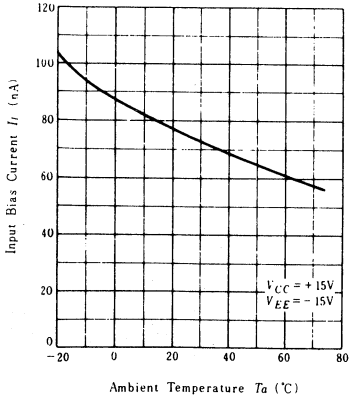
INPUT OFFSET VOLTAGE VS AMBIENT TEMPERATURE



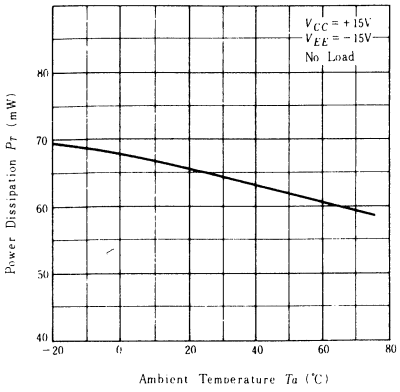
INPUT OFFSET CURRENT VS AMBIENT TEMPERATURE



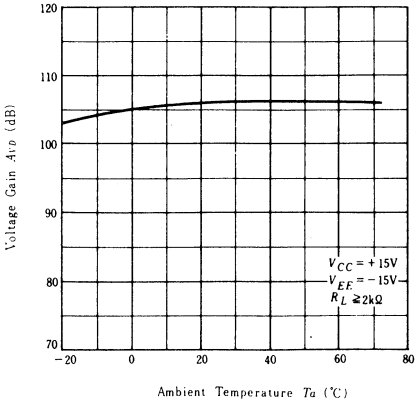
INPUT BIAS CURRENT VS AMBIENT TEMPERATURE



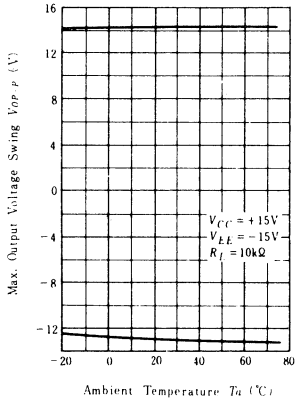
POWER DISSIPATION VS AMBIENT TEMPERATURE



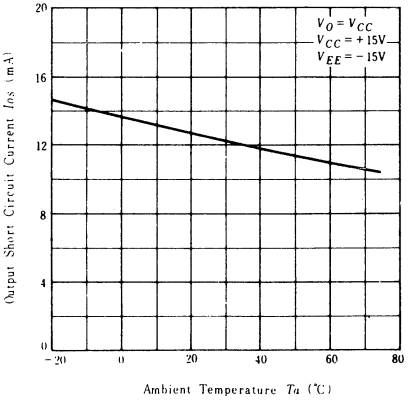
VOLTAGE GAIN VS AMBIENT TEMPERATURE



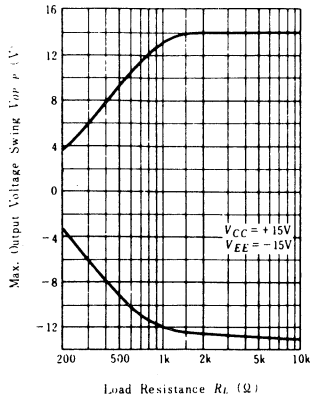
PEAK TO PEAK OUTPUT VOLTAGE VS AMBIENT TEMPERATURE



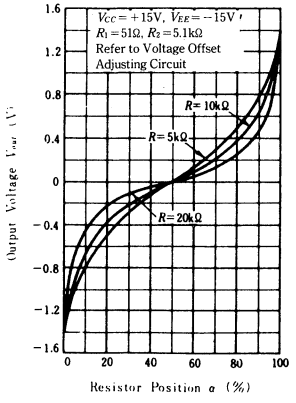
OUTPUT SHORT-CIRCUIT CURRENT VS AMBIENT TEMPERATURE



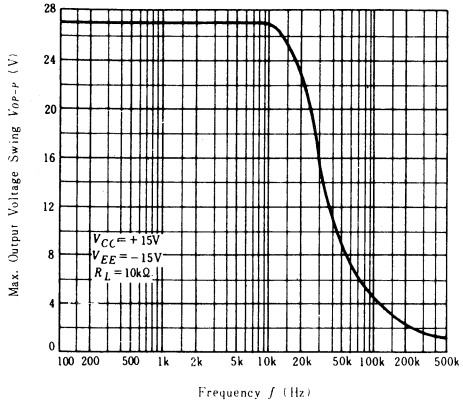
PEAK TO PEAK OUTPUT VOLTAGE VS LOAD RESISTANCE



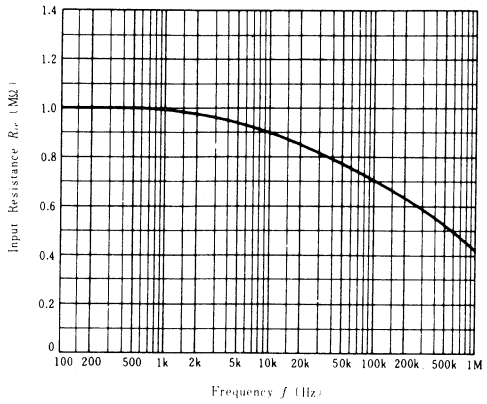
OFFSET ADJUSTING CHARACTERISTIC



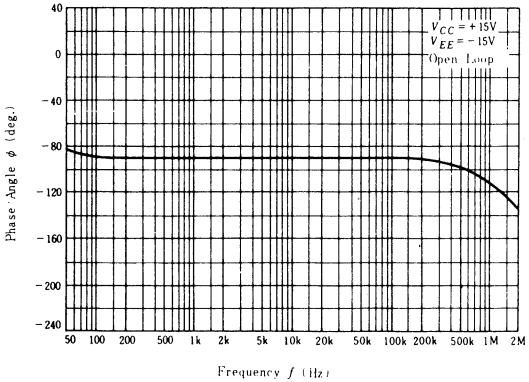
PEAK TO PEAK OUTPUT VOLTAGE VS FREQUENCY



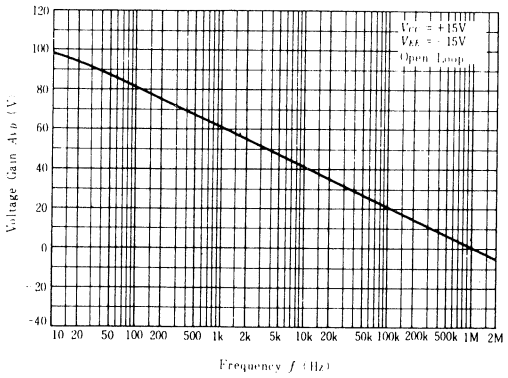
INPUT RESISTANCE VS FREQUENCY



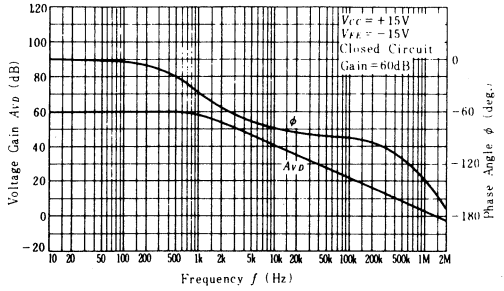
PHASE VS FREQUENCY



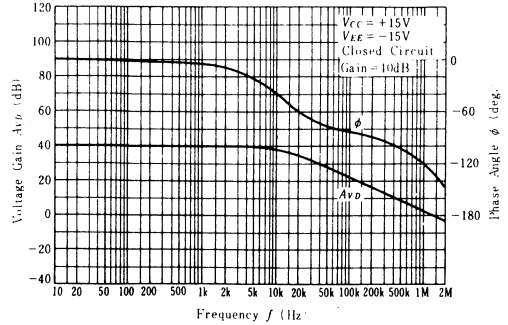
VOLTAGE GAIN VS FREQUENCY



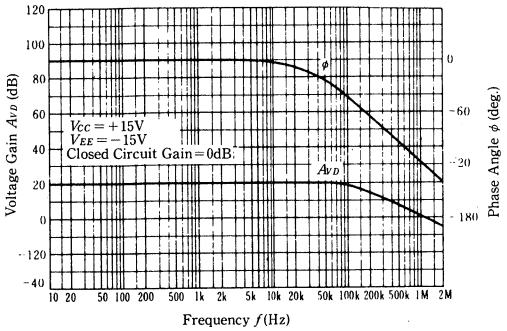
VOLTAGE GAIN, PHASE ANGLE VS FREQUENCY (1)



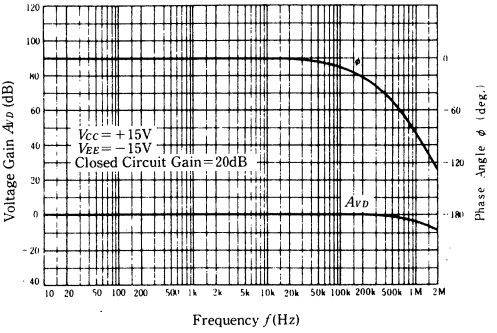
VOLTAGE GAIN, PHASE ANGLE VS FREQUENCY (2)



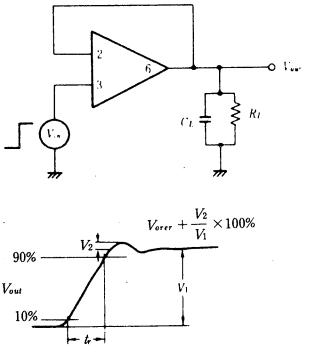
VOLTAGE GAIN, PHASE ANGLE VS FREQUENCY (3)



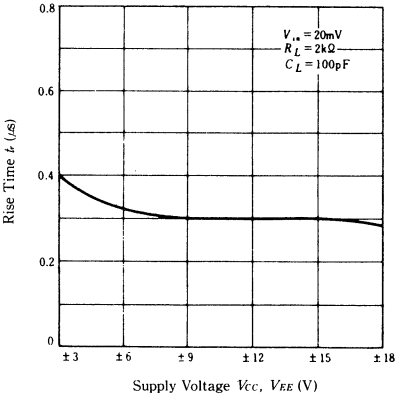
VOLTAGE GAIN, PHASE ANGLE VS FREQUENCY (4)



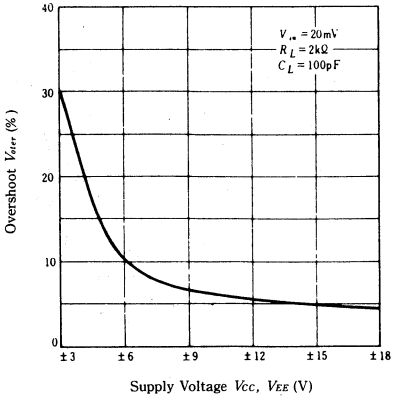
TRANSIENT RESPONSE CHARACTERISTIC MEASURING CIRCUIT



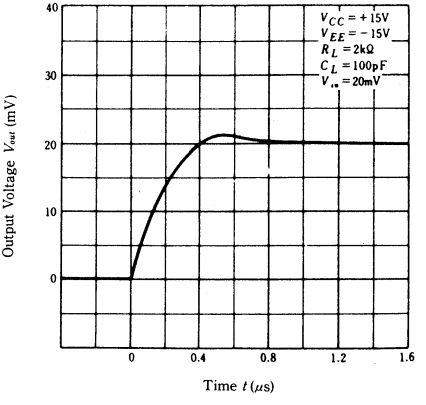
RISE TIME VS SUPPLY VOLTAGE



OVERSHOOT VS SUPPLY VOLTAGE



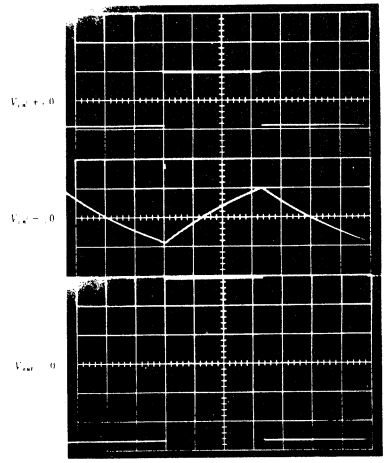
TRANSIENT RESPONSE CHARACTERISTIC



■ AN APPLICATION OF IC OPERATIONAL AMPLIFIER

1. Multivibrator

Multivibrator is the square wave generator utilizing the charge and discharge phenomenon of CR, and is widely used in power source of square wave, electromagnetic switch, etc.
Multivibrator is classified by Astable Multivibrator without stable state, Monostable Multivibrator with one stable state, Bistable Multivibrator with two stable states.



axis of ordinates 5V/DIV
quadrature axis 2ms/DIV
conditions $R_1 = 8k\Omega$, $R_2 = 4k\Omega$, $R_3 = 100k\Omega$, $C_1 = 0.1\mu F$, $R_L = \infty$, $V_{CC} = 15V$, $V_{EE} = -15V$

Fig.2 HA17741 Astable Multivibrator Operating Waveform

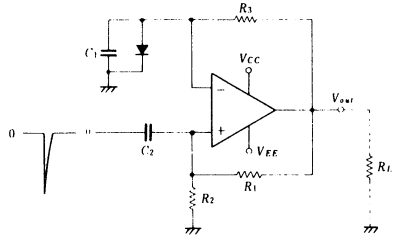


Fig.3 Monostable Multivibrator Operating Circuit

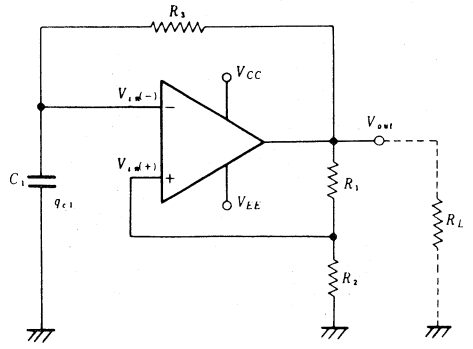
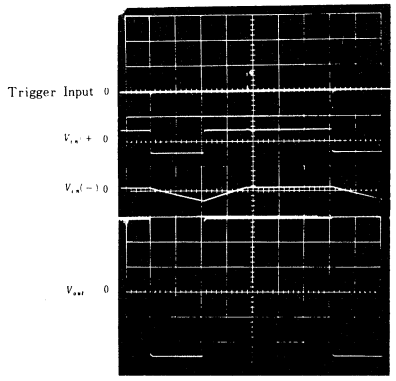


Fig.1 Astable Multivibrator Operating Circuit



axis of ordinates 5V/DIV
quadrature axis 2ms/DIV
conditions $R_1 = 10k\Omega$, $R_2 = 2k\Omega$, $R_3 = 40k\Omega$, $C_1 = 0.47\mu F$, $C_2 = 0.0068\mu F$, $R_L = \infty$, $V_{CC} = 15V$, $V_{EE} = -15V$

Fig.4 HA17741 Monostable Multivibrator Operating Waveform

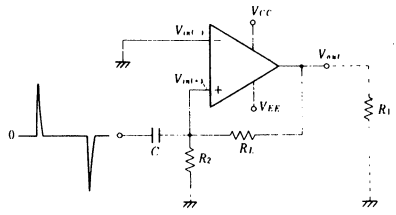
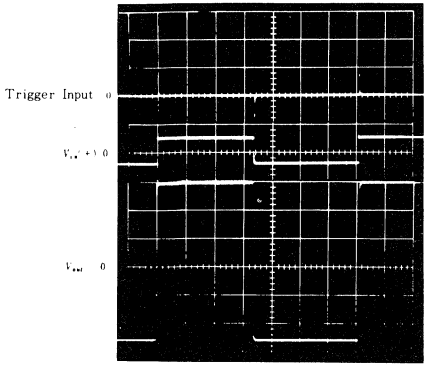


Fig.5 Bistable Multivibrator Operating Circuit



axis of ordinates 5V/DIV
quadrature axis 2ms/DIV
conditions $\begin{cases} R_1 = 10k\Omega, \ R_2 = 2k\Omega \\ C = 0.0068\mu F \\ R = \infty \\ V_{CC} = 15V, \ V_{EE} = -15V \end{cases}$

Fig.6 HA17741 Bistable Multivibrator Operating Waveform

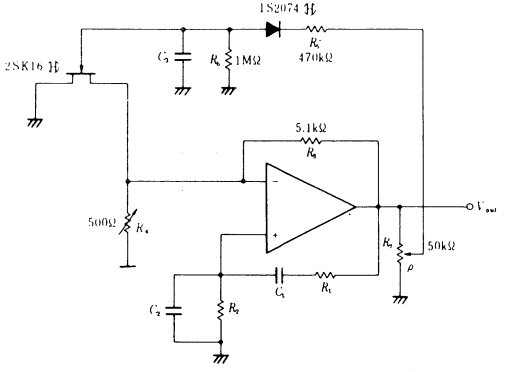


Fig.7 Wien bridge sine wave oscillator

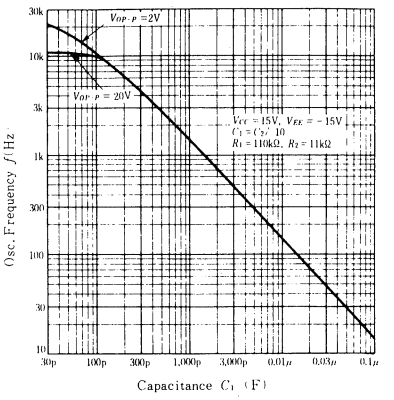
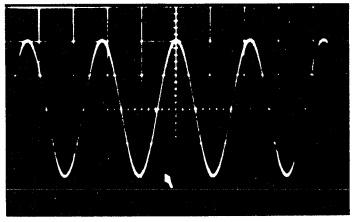


Fig.8 HA17741 Wien bridge sine wave oscillator f-c characteristic



axis of ordinates 5V/DIV
quadrature axis 0.5ms/DIV
conditions $\begin{cases} V_{CC} = 15V, \ V_{EE} = -15V \\ R_1 = 110k\Omega, \ R_2 = 11k\Omega \\ C_1 = 0.0015\mu F, \ C_2 = 0.015\mu F \\ \text{measurement result} \\ f = 929.7Hz, \ T.H.D = 0.06\% \end{cases}$

Fig.9 Operating Waveform of HA17741 Wien bridge sine wave oscillator

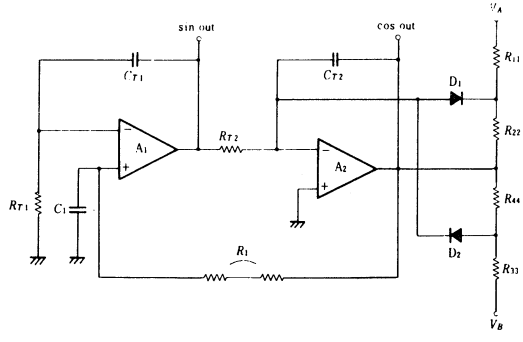


Fig.10 Quadrature Sine Wave Oscillator

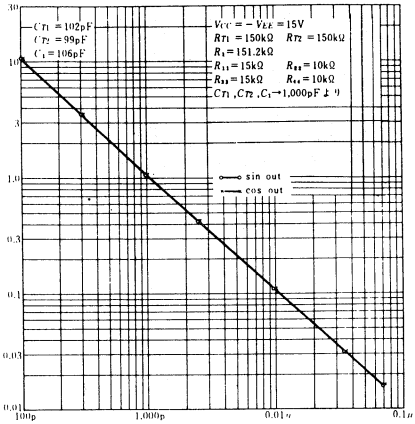
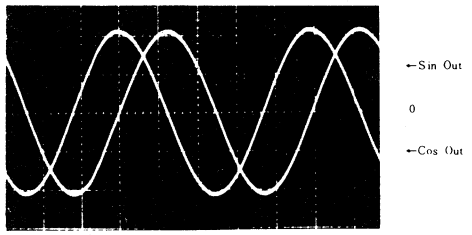


Fig.11 HA17747 Quadrature Sine Wave Oscillator f-C_{T1}, C_{T2}, C_1 characteristic



axis of ordinates 5V/DIV
quadrature axis 0.2ms/DIV
conditions

C_{T1} = 1000pF (990)	C_{T2} = 1000pF (990)
R_{T1} = 150kΩ	R_{T2} = 150kΩ
C_1 = 1000pF (990)	R_1 = 160kΩ
R_{11} = 15kΩ	R_{22} = 10kΩ
R_{33} = 16V	R_{44} = 10kΩ
V_{CC} = 15V	V_{EE} = − 15V

Fig.12 Output Waveform of Sine, Cos

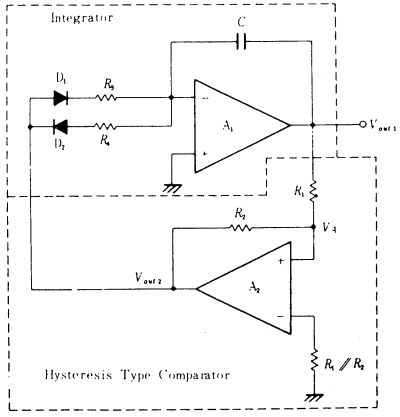
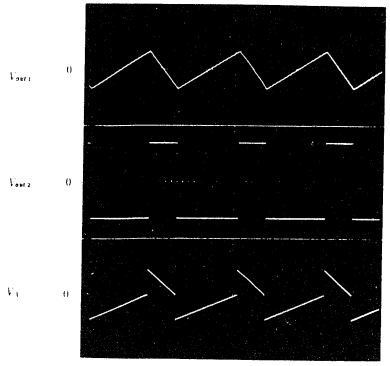


Fig.13 Triangular Wave Generator Operating Circuit



axis of ordinates 10V/DIV
quadrature axis 10ms/DIV
conditions $\begin{cases} V_{CC}=15\text{V},\ V_{EE}=-15\text{V} \\ R_1=10\text{k}\Omega,\ R_2=20\text{k}\Omega \\ R_3=100\text{k}\Omega,\ R_4=200\text{k}\Omega \\ C=0.1\mu\text{F} \end{cases}$

Fig.14 Operating Waveform of HA17741 Triangular Wave Generator

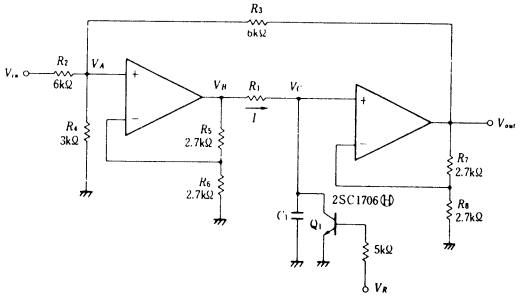
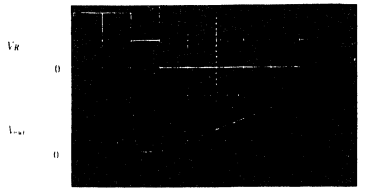


Fig.15 Saw Tooth Generator



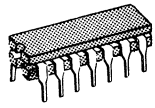
axis of ordinates 5V/DIV
quadrature axis 2ms/DIV
conditions $\begin{cases} V_{CC}=15\text{V},\ V_{EE}=-15\text{V} \\ R_1=100\text{k}\Omega,\ C_1=0.1\mu\text{F} \\ V_{in}=10\text{V} \end{cases}$

Fig.16 HA17741 Saw Tooth Generator Operating Waveform

HA17747 Series ● Dual Operational Amplifier

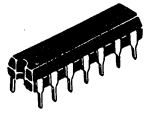
HA17747 is an internal phase compensated type, high performance, dual operational amplifier, and its wide scope of application is possible in the field of measuring and control use.

HA17747G



(PG-14)

HA17747P
HA17747

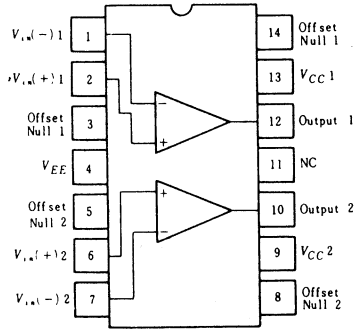


(DP-14)

■ FEATURES

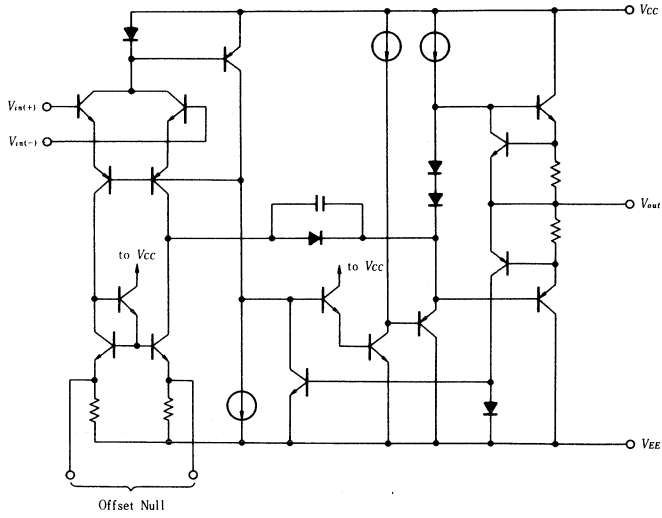
- Industrial use HA17747G, HA17747P
- Commercial use HA17747
- High Voltage Gain . . . . . 106dB (typ)
- Wide Output Amplitude . . . ±13V (typ) [at $R_L \geqq 2k\Omega$]
- Protected to Output Short
- Capable of adjusting Offset Voltage
- Internal Phase Compensated Type

■ PIN ARRANGEMENT



(Top View)

■ CIRCUIT SCHEMATIC(1/2)



■ ABSOLUTE MAXIMUM RATINGS (Ta=25°C)

Item	Symbol	HA17747G	HA17747P	HA17747	Unit
Supply Voltage	V_{CC}	+18	+18	+18	V
	V_{EE}	−18	−18	−18	V
Power Dissipation	P_T	670*	670**	670**	mW
Input Voltage	V_{in}***	±15	±15	±15	V
Differential Input Voltage	$V_{in(diff)}$	±30	±30	±30	V
Voltage between Offset Adjusting Terminal and V_{EE}	V_{OFF} V_{EE}	±0.5	±0.5	±0.5	V
Operating Temperature	T_{opr}	−20 to +75	−20 to +75	0 to +70	°C
Storage Temperature	T_{stg}	−65 to +150	−55 to +125	−55 to +125	°C

* Value under Ta≦65°C. In case of more than it, 7.6mW/°C derating shall be done.
** Value under Ta≦45°C. In case of more than it, 8.3mW/°C derating shall be done.
*** If supply voltage is less than ±15V, input voltage is to supply voltage.

■ ELECTRICAL CHARACTERISTICS-1 (V_{CC}=−V_{EE}=15V, Ta=25°C)

Item	Symbol	Measuring Condition	min	typ	max	Unit
Input Offset Voltage	V_{IO}	R_S≦10kΩ	−	1.0	6.0	mV
Input Offset Current	I_{IO}		−	20	200	nA
Input Bias Current	I_I		−	80	500	nA
Voltage Gain	A_{VD}	R_L≧2kΩ, V_{out}=±10V	88	106	−	dB
Supply Current	I_{CC}	at the time of no load It's the value per 1 channel.	−	1.7	2.8	mA
Power Dissipation	P_T		−	50	85	mW
Input Resistance	R_{in}		0.3	2.0	−	MΩ
Input Capacitance	C_{in}		−	1.4	−	pF
Output Resistance	R_{out}		−	75	−	Ω
Slew Rate	SR	R_L≧2kΩ	−	1.0	−	V/μs
Rise Time	t_r	V_{in}=20mV, R_L=2kΩ, C_L=100pF	−	0.3	−	μs
Overshoot	V_{over}		−	5.0	−	%
Input Offset Voltage Adjusting Range	$\triangle V_{IO\ adj}$		−	±15	−	mV
Output Short Current	I_{os}		−	25	−	mA
Channel Separation	CS		−	120	−	dB

■ ELECTRICAL CHARACTERISTICS-2 (V_{CC}=−V_{EE}=15V, Ta=−20 to +75°C, however, as for HA17747, Ta=0 to +70°C)

Item	Symbol	Measuring Condition	min	typ	max	Unit
Input Offset Voltage	V_{IO}	R_S≦10kΩ	−	1.0	9.0	mV
Input Offset Current	I_{IO}		−	20	400	nA
Input Bias Current	I_I		−	80	1100	nA
Line Reguration	$\triangle V_{IO}/\triangle V_{CC}$ $\triangle V_{IO}/\triangle V_{EE}$	R_S≦10kΩ	−	30	150	μV/V
Voltage Gain	A_{VD}	R_L≧2kΩ, V_{out}=±10V	80	−	−	dB
Common Mode Rejection Ratio	CMR	R_S≦10kΩ	70	90	−	dB
Common Mode Input Voltage Range	V_{CM}		±12	±13	−	V
Peak To Peak Output Voltage Amplitude	$V_{OP\text{-}P}$	R_L≧10kΩ	±12	±14	−	V
		R_L≧2kΩ	±10	±13	−	V
Supply Current	I_{CC}	at the time of no load It's the value per 1 channel.	−	2.1	3.7	mA
Power Dissipation	P_T		−	65	110	mW

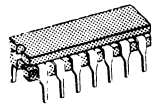
Note) As for characteristic curve, refer to HA17741

HA17902 Series ●Quad. Operational Amplifier

HA17902 is Quad. Operational Amplifier that provide high gain and internal phase compensation, and mono power source operation is possible. They can be widely used to control equipments.

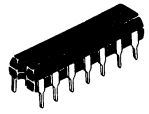
Industrial Use; HA17902G, HA17902P
Commercial Use; HA17902

HA17902G



(DG-14)

HA17902P
HA17902

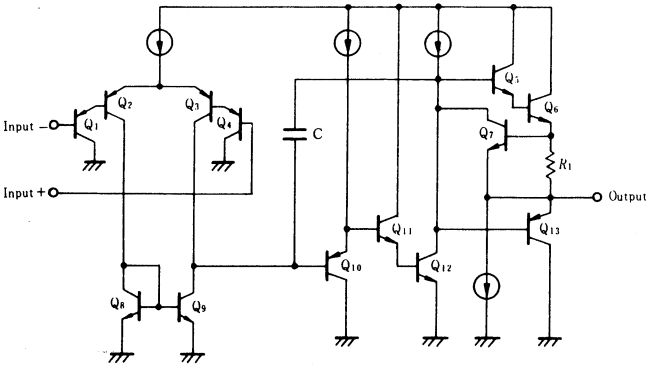


(DP-14)

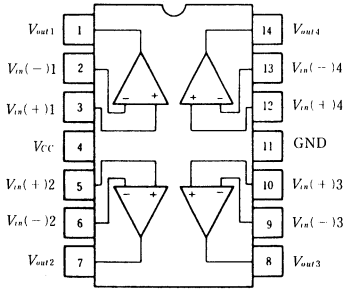
■FEATURES

- Wide range of supply voltage, and mono power source operation is possible.
- Internal Phase Compensation
- Wide range of common mode voltage, and possible to operate with an input about 0V.

■CIRCUIT SCHEMATIC(1/4)



■PIN ARRANGEMENT



(Top View)

■ABSOLUTE MAXIMUM RATINGS ($Ta = 25°C$)

Item	Symbol	HA17902G	HA17902P	HA17902	Unit
Supply Voltage	V_{CC}	28	28	28	V
Sink Current	I_{sink}	50	50	50	mA
Power Dissipation	P_T	625*	625**	625**	mW
Common Mode Input Voltage	V_{CM}	-0.3 to V_{CC}	-0.3 to V_{CC}	-0.3 to V_{CC}	V
Differential Input Voltage	$V_{in\cdot diff}$	± V_{CC}	± V_{CC}	± V_{CC}	V
Operating Temperature	T_{opr}	-40 to +85	-20 to +75	0 to +70	°C
Storage Temperature	T_{stg}	-60 to +150	-55 to +125	-55 to +125	°C

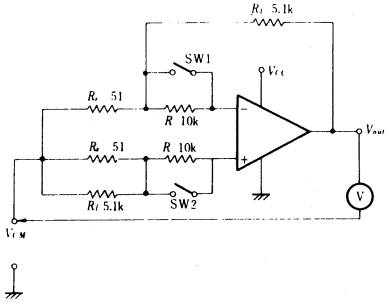
* Value under $Ta \leqq 70°C$. In case of more than it, 7.6mW/°C derating shall be done.
** Value under $Ta \leqq 50°C$. In case of more than it, 8.3mW/°C derating shall be done.

■ ELECTRICAL CHARACTERISTICS (V_{CC} = +15V, Ta = 25°C)

Item	Symbol	Test Conditions	min	typ	max	Unit
Input Offset Voltage	V_{IO}	V_{CM} = 7.5V, R_S = 50Ω, R_f = 5 kΩ	—	3	8	mV
Input Offset Current	I_{IO}	$I_{IO} = \lvert I_I^- - I_I^+ \rvert$, V_{CM} = 7.5V	—	5	50	nA
Input Bias Current	I_I	V_{CM} = 7.5V	—	30	500	nA
Power Source Rejection Ratio	$PSRR$	f = 100Hz, R_S = 1kΩ, R_f = 100kΩ	—	93	—	dB
Voltage Gain	A_{VD}	R_S = 1kΩ, R_f = 100kΩ, R_L = ∞	75	90	—	dB
Common Mode Rejection Ratio	CMR	R_S = 50Ω, R_f = 5kΩ	—	80	—	dB
Common Mode Input Voltage Range	V_{CM}	R_S = 1kΩ, R_f = 100kΩ, f = 100Hz	−0.3	—	13.5	V
Peak-to-peak Output Voltage	$V_{op\ p}$	f = 100Hz, R_S = 1kΩ, R_f = 100kΩ, R_L = 20kΩ	—	13.6	—	V
Output Voltage	V_{OH1}	I_{OH} = −1mA	13.2	13.6	—	V
	V_{OH2}	I_{OH} = −10mA	12	13.3	—	V
	V_{OL1}	I_{OL} = 1mA	—	0.8	1	V
	V_{OL2}	I_{OL} = 10mA	—	1.1	1.8	V
Output Source Current	I_{source}	V_{OH} = 10V	15	40	—	mA
Output Sink Current	I_{sink}	V_{OL} = 1V	3	9	—	mA
Supply Current	I_{CC}	V_{in} = GND, R_L = ∞	—	0.8	2	mA
Power Dissipation	P_T	R_L = ∞, V_{in} = GND	—	12	30	mW
Slew Rate	SR	f = 1.5kHz, V_{CM} = 7.5V, R_L = ∞	—	0.19	—	V/μs
Channel Separation	CS	f = 1kHz	—	120	—	dB

■ TEST CIRCUIT

1. Input Offset Voltage (V_{IO}), Input Offset Current (I_{IO}), Input Bias Current (I_I)



SW 1	SW 2	V_O
ON	ON	V_{O1}
OFF	OFF	V_{O2}
ON	OFF	V_{O3}
OFF	ON	V_{O4}

$$V_{CM} = \frac{1}{2} V_{CC}$$

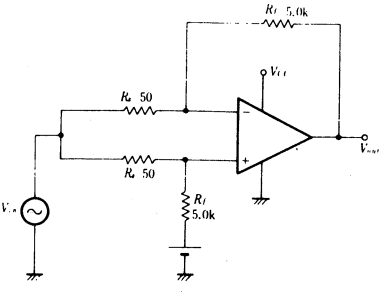
(1) $$V_{IO} = \frac{V_{O1}}{1 + R_f/R_S} \quad (V)$$

(2) $$I_{IO} = \frac{V_{O2} - V_{O1}}{R(1 + R_f/R_S)} \quad (A)$$

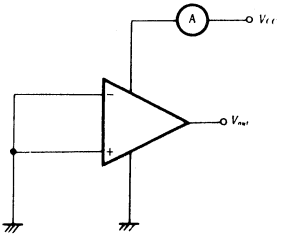
(3) $$I_I = \frac{\lvert V_{O4} - V_{O3} \rvert}{2 \cdot R(1 + R_f/R_S)} \quad (A)$$

2. Common Mode Input Rejection Ratio (CMR)

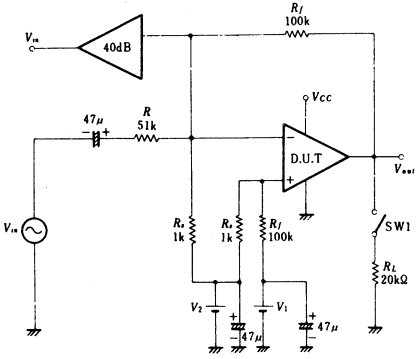
$$CMR = 20 \log \frac{V_{IN} \cdot R_f}{V_O \cdot R_S} \quad (dB)$$



3. Supply Current (I_{CC})



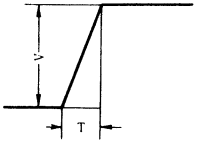
4. Voltage Gain (A_{VD}), Slew Rate (S.R), Common Mode Input Voltage Range (V_{CM}), Peak-to-peak Output Voltage Range (V_{op-p})



(1) A_{VD} : $R_S = 1\text{k}\Omega$, $R_f = 100\text{k}\Omega$, $R_L = \infty$,
$V_1 = V_2 = \frac{1}{2} V_{CC}$

$$A_{VD} = 20 \log \frac{V_O}{V_{IN}'} + 40 \ (\text{dB})$$

(2) SR : $f = 1.5\text{kHz}$, $R_L = \infty$,
$V_1 = V_2 = \frac{1}{2} V_{CC}$



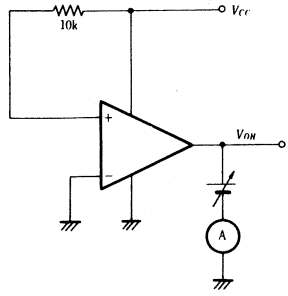
$$SR = \frac{V}{T} \ [V/\mu\text{s}]$$

(3) V_{CM} : $R_S = 1\text{k}\Omega$, $R_f = 100\text{k}\Omega$, $f = 100\text{Hz}$,
$V_1 = \frac{1}{2} V_{CC}$, $R_L = \infty$, value of V_2 just before the waveform changes. $V_{CM(+)}$, $V_{CM(-)}$

(4) V_{op-p} : $R_S = 1\text{k}\Omega$, $R_f = 100\text{k}\Omega$, $R_L = 20\text{k}\Omega$,
$f = 100\text{Hz}$, $V_{op-p} = V_{OH} \longleftrightarrow V_{OL}$ [V_{P-P}]

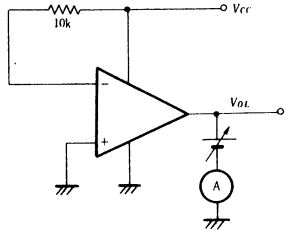
5. Output Source Current (I_{source})

I_{source} : $V_{OH} = 10\text{V}$

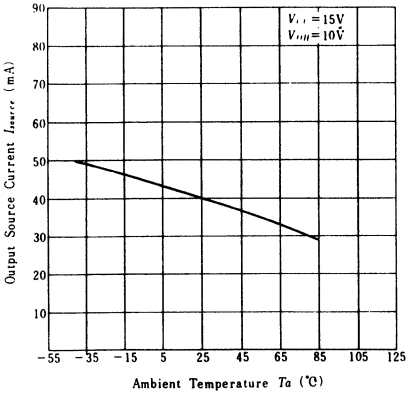


6. Output Sink Current (I_{sink})

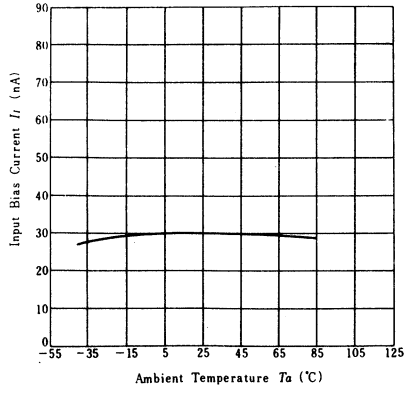
I_{sink} : $V_{OL} = 1\text{V}$



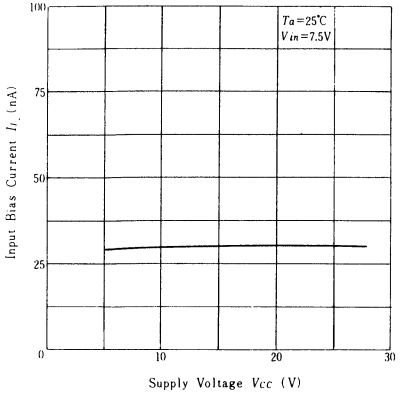
OUTPUT SOURCE CURRENT VS. AMBIENT TEMPERATURE



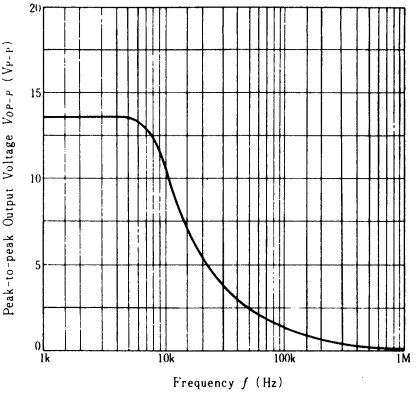
INPUT BIAS CURRENT VS. AMBIENT TEMPERATURE



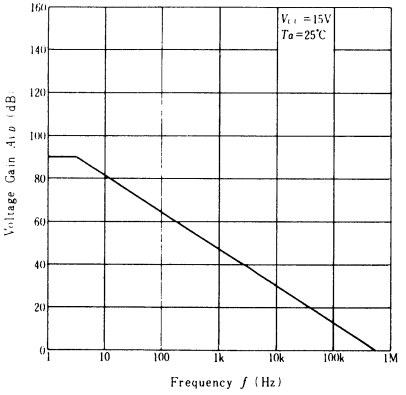
INPUT BIAS CURRENT VS. SUPPLY VOLTAGE



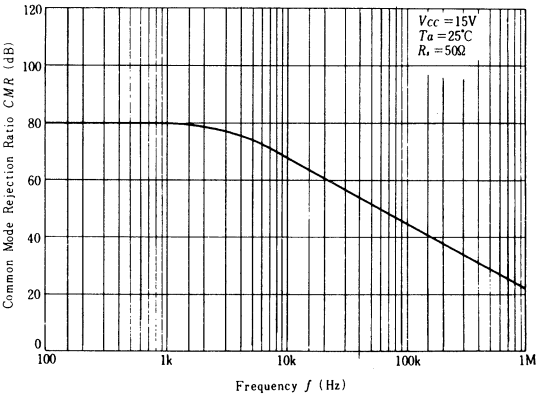
PEAK-TO-PEAK OUTPUT VOLTAGE VS. FREQUENCY



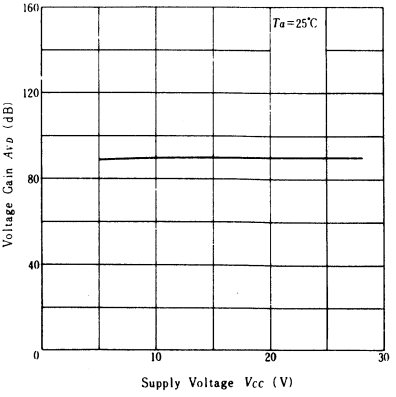
VOLTAGE GAIN VS. FREQUENCY



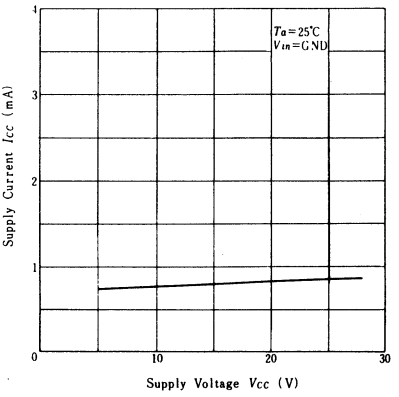
COMMON MODE REJECTION RATIO VS. FREQUENCY



VOLTAGE GAIN VS. SUPPLY VOLTAGE



SUPPLY CURRENT VS. SUPPLY VOLTAGE



■ HA17902 APPLICATION

HA17902 is a Quad. Operational Amplifier, and it's consisted of four operational amplifiers which operate independently, and a bias circuit. It can be widely used with the features such as wide range of operating temperature, mono power source operation, internal phase compensation, wide 0-cross band-width, small input bias current, large open loop voltage gain, etc. HA17902 applications will be explained below.

1. Non-inverted Amplifier

Fig.1 shows a non-inverted amplifier.

Voltage gain of the circuit is; $\frac{V_{out}}{V_{in}} = 1 + \frac{R_2}{R_1}$

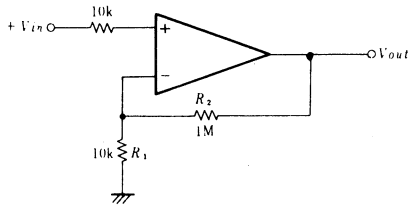


Fig.1 Non-inverted Amplifier

2. Adding & Subtracting Amplifier

In Fig.2, input +V1 and +V2 are applied to non-inversion circuit and input +V3 and +V4 are to inversion circuit.

The output is; $V_{out} = V_1 + V_2 - V_3 - V_4$

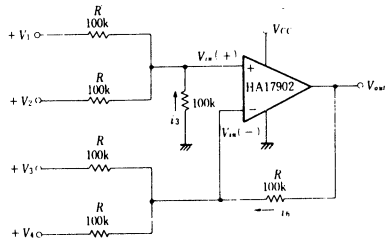


Fig.2 Adding & Subtracting Amplifier

3. High Input Impedance DC Differential Amplifier

Fig.3 shows a High Input Impedance DC Differential Amplifier which is consisted of two non-inverted amplifiers connected in cascade. The common mode rejection ratio (CMR) is depend on the matching of R_1/R_3 and R_4/R_3.

The output is;

$$V_{out} = \left(1 + \frac{R_4}{R_3}\right)(V_2 - V_1)$$

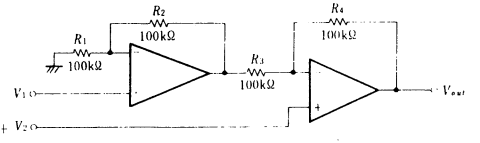


Fig.3 High Input Impedance DC Differential Amplifier

4. Voltage Control Generator

In Fig.4, Amp A_1, A_2 and TRS Q_1 operate as an integrator, a comparator and a switch for control of oscillation frequency, respectively.

When $Vout_1$ is in "LOW" level, TRS Q_1 is cut off. The potential of inverted input of A_1 becomes higher than that of non-inverted input, and the output of A_1 will be integrated to be the "LOW" level.

When the output of integrator A_1 becomes smaller than the non-inverted input of comparator A_2 ($V_{cc}/2$), output of the comparator will be "HIGH" level and TRS Q_1 will turn ON. Then the output of A_1 will be integrated to be "HIGH" level.

In this way, a square wave and a triangular wave are generated at $Vout_1$ and $Vout_2$ respectively.

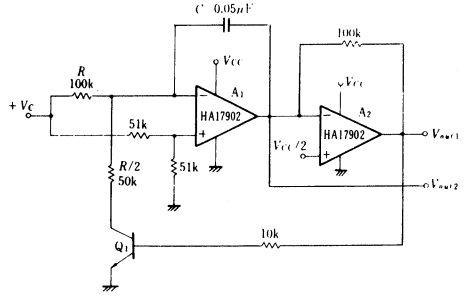


Fig.4 Voltage Control Oscillator

DATA SHEETS

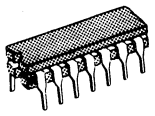
Voltage Comparators

HA17339, HA17901 Series ●Ouadruple Comparators

HA17901 and HA17339 are comparators designed for car use and control system use.
They provide wide operating voltage with single power source, and the supply current is small because it is independent of the supply voltage.
They can be widely applied, such as limit comparator, simple analog/digital converter, pulse/square wave/time delay generator, wide range VCO, MOS clock timer, multivibrator, high voltage logic gate, etc.

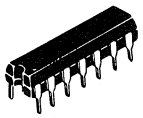
Industrial: HA17901G, HA17901P
Commercial: HA17339

HA17901G



(DG-14)

HA17901P
HA17339

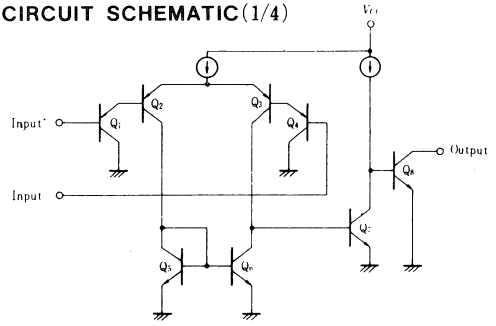


(DP-14)

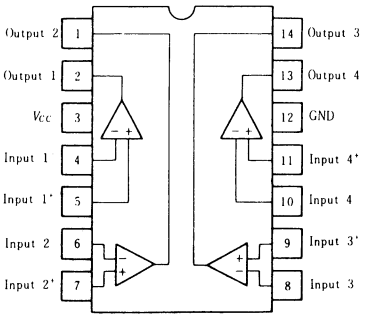
■ FEATURES

- Wide Range of Supply Voltage . . . . . 2 to 36V
- Very Small Supply Current 0.8mA
- Small Input Bias Current 25nA
- Small Input Offset Current 3nA
- Small Input Offset Voltage 2mV
- Common Mode Input Voltage Range Including Ground
- Differential Input Voltage Range Equal to Supply Voltage.
- Small Output Saturation Voltage . . . . . 1mV(5μA)
  70mV(1mA)
- The output voltage is compatible with that of CMOS Logic System

■ CIRCUIT SCHEMATIC (1/4)



■ PIN ARRANGEMENT



(Top View)

■ ABSOLUTE MAXIMUM RATINGS (Ta=25°C)

Item	Symbol	HA17901G	HA17901P	HA17339	Unit	Note
Supply Voltage	V_{CC}	36	36	36	V	
Differential Input Voltage	$V_{in(diff)}$	± V_{CC}	± V_{CC}	± V_{CC}	V	
Input Voltage	V_{in}	−0.3 to +36	−0.3 to +36	−0.3 to +36	V	
Power Dissipation	P_T	625*	625**	625**	mW	1
Output Current	I_{out}	20	20	20	mA	2
Operating Temperature	T_{opr}	−40 to +85	−20 to +75	0 to +70	°C	
Storage Temperature	T_{stg}	−65 to +150	−55 to +125	−55 to +125	°C	
Output Voltage	V_{out}	36	36	36	V	

Note (1. * Value at Ta=70°C. In case of more than it, 7.6mW/°C derating shall be performed.
** Value at Ta=50°C. In case of more than it, 8.3mW/°C derating shall be performed.
(2. Short-circuit between the output and V_{CC} will be a cause to destroy the circuit.
The maximum output current is the permissible value for continuous operation.

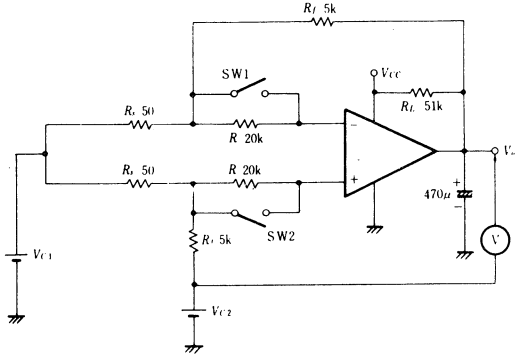
■ ELECTRICAL CHARACTERISTICS (V_{CC}=5V, Ta=25°C)

Item	Symbol	Test Condition	min	typ	max	Unit
Input Offset Voltage	V_{IO}	V_{REF}=1.4V & R_S=0Ω when V_O≅1.4V at the output switching point	—	2	7	mV
Input Bias Current	I_{IB}	$I_{IN(+)}$ or $I_{IN(-)}$	—	25	250	nA
Input Offset Current	I_{IO}	$I_{IN(+)} - I_{IN(-)}$	—	5	50	nA
Common Mode Input Voltage (Note 1)	V_{CM}		0	—	V_{CC}−1.5	V
Supply Current	I_{CC}	R_L=∞	—	0.8	2	mA
Voltage Gain	A_V	R_L=15kΩ	—	200	—	V/mV
Response Time (Note 2)	t_R	V_{RL}=5V, R_L=5.1kΩ	—	1.3	—	μs
Output Sink Current	I_{sink}	$V_{IN(-)}$=1V, $V_{IN(+)}$=0, V_O≧1.5V	6	16	—	mA
Output Saturation Voltage	V_{osat}	$V_{IN(-)}$=1V, $V_{IN(+)}$=0, I_{sink}=3mA	—	200	400	mV
Output Leak Current	I_{LO}	$V_{IN(+)}$=1V, $V_{IN(-)}$=0, V_O=5V	—	0.1	—	nA

Note) 1. Common mode input voltage or either of the input signal voltages should not be less than −0.3V.
2. This is a value to 100mV input step voltage with 5mV overdrive.

■ TEST CIRCUIT

1. Input Offset Voltage (V_{IO}), Input Offset Current (I_{IO}) Input Bias Current (I_{IB})



SW 1	SW 2	V_{out}
ON	ON	V_{O1}
OFF	OFF	V_{O2}
ON	OFF	V_{O3}
OFF	ON	V_{O4}

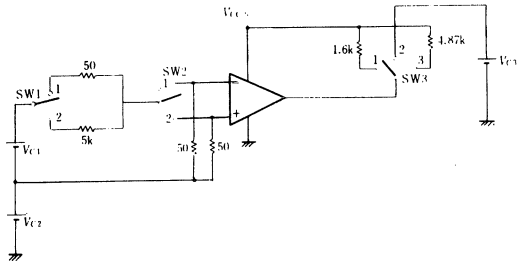
V_{C1}=1/2 V_{CC}
V_{C2}=1.4V

(1) $V_{IO} = \dfrac{|V_{O1}|}{1+\dfrac{R_f}{R_S}}$ 〔V〕

(2) $I_{IO} = \dfrac{|V_{O2}-V_{O1}|}{R\left(1+\dfrac{R_f}{R_S}\right)}$ 〔A〕

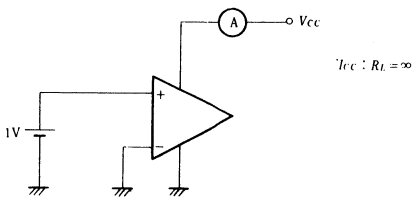
(3) $I_{IB} = \dfrac{|V_{O4}-V_{O3}|}{2\cdot R\left(1+\dfrac{R_f}{R_S}\right)}$ 〔A〕

2. Output Saturation Voltage (V_O sat), Output Sink Current (Isink), Common Mode Input Voltage (V_{CM})

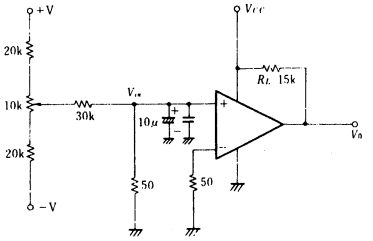


Item	V_{C1}	V_{C2}	V_{C3}	SW 1	SW 2	SW 3	Unit
V_O sat	2V	0V	—	1	1	1 at V_{CC}=5V 3 at V_{CC}=15V	V
I_{sink}	2V	0V	1.5V	1	1	2	mA
V_{CM}	2V	−1~V_{CC}	—	2	1, 2 switch	3	V

3. Supply Current (I_{CC})

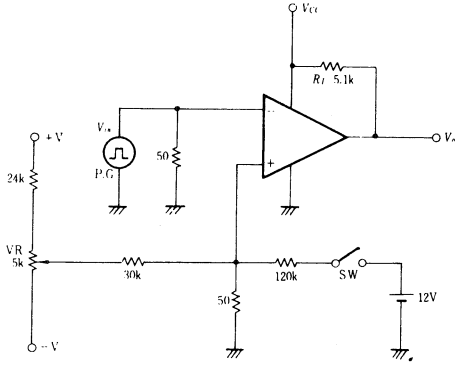


4. Voltage Gain (A_V) (R_L = 15kΩ)

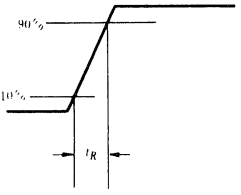


$$A_V = 20 \log \frac{V_{O1} - V_{O2}}{V_{IN1} - V_{IN2}} \quad [dB]$$

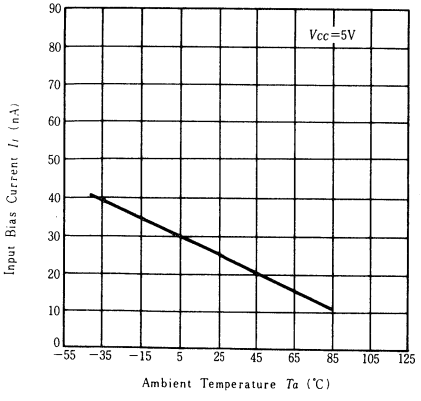
5. Response Time (t_R)



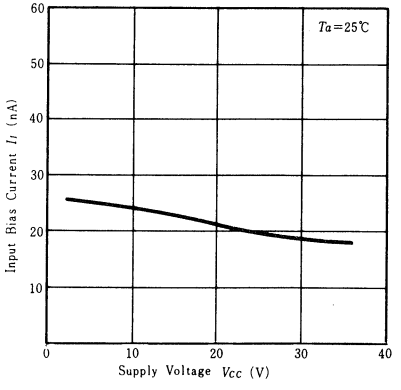
t_R: R_L = 5.1kΩ,
100mV input with 5mV overdrive
Turn the SW OFF without applying V_{IN}, and adjust the V_R to make V_O 1.4V approximately.
Apply V_{IN}, and turn the SW ON.



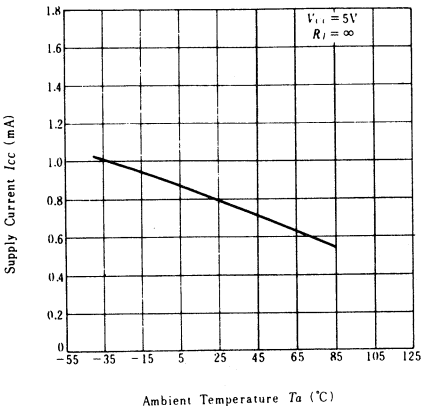
INPUT BIAS CURRENT VS: AMBIENT TEMPERATURE



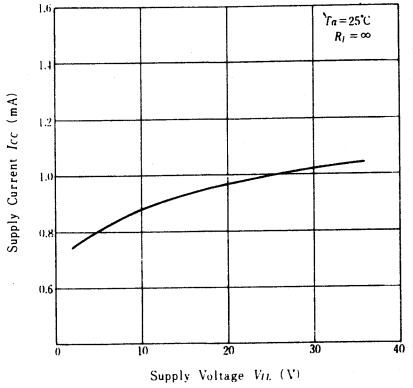
INPUT BIAS CURRENT VS. SUPPLY VOLTAGE



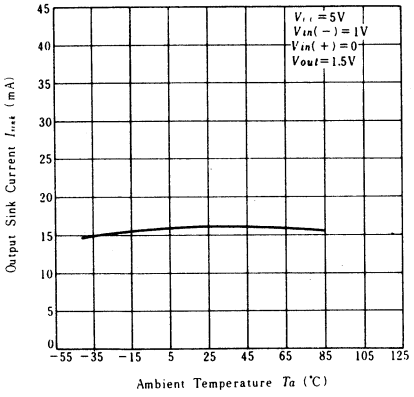
SUPPLY CURRENT VS. AMBIENT TEMPERATURE



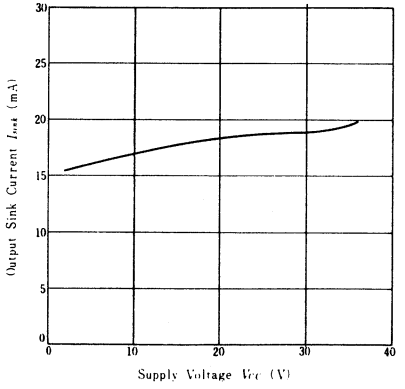
SUPPLY CURRENT VS. SUPPLY VOLTAGE



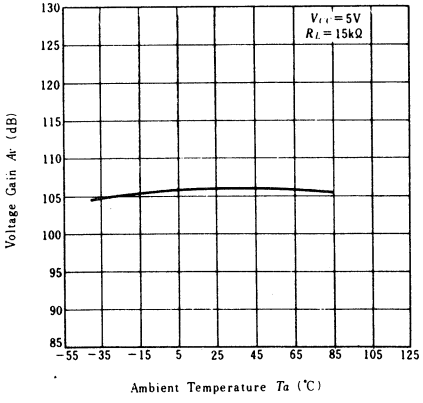
OUTPUT SINK CURRENT VS. SUPPLY VOLTAGE



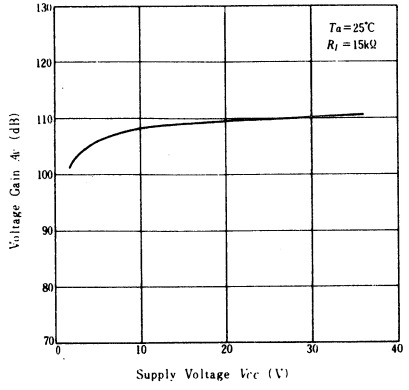
OUTPUT SINK CURRENT VS. SUPPLY VOLTAGE



VOLTAGE GAIN VS. AMBIENT TEMPERATURE



VOLTAGE GAIN VS. SUPPLY VOLTAGE



HA17393, HA17903 Series ●Dual Comparators

HA17903 and HA17393 are comparators designed for car use and control system use.
They provide wide voltage range with single power source, and the change of supply current is small, because it is independent of the supply voltage.
They can be widely applied, such as limit comparator, simple analog/digital converter, pulse/square wave/time delay genetor, wide range VCO, MOS clock timer, multivibrator, high voltage logic gate, etc.
Industrial: HA17903GS, HA17903PS
Commercial: HA17393

HA17903GS

(DG-8)

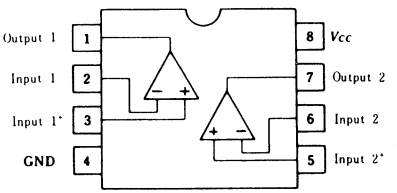
HA17903PS
HA17393

(DP-8)

■FEATURES

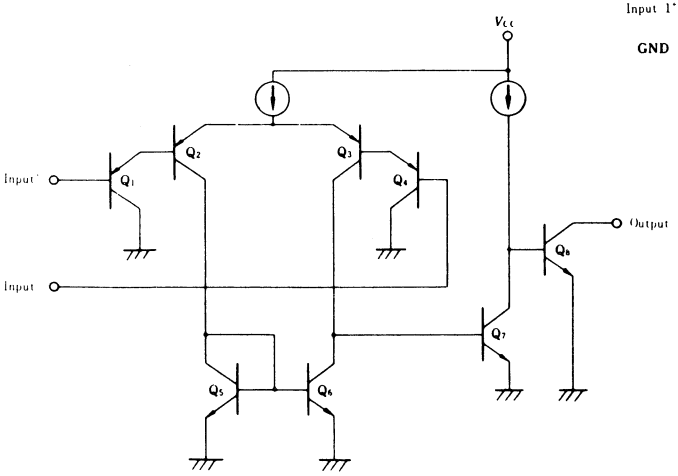
- Wide Supply Voltage . . . . . 2 to 36V
- Very Low Supply Current 0.8mA
- Small Input Bias 25nA
- Small Input Offset Current 3nA
- Small Input Offset Voltage 2mV
- Common Mode Input Voltage Range Including Ground.
- Small Output Saturation Voltage . . . . . 1mV(5μA)
  70mV(1mA)
- Output Voltage is Compatible with CMOS Logic System.

■PIN ARRANGEMENT



(Top View)

■CIRCUIT SCHEMATIC(1/2)



■ ABSOLUTE MAXIMUM RATINGS (Ta=25°C)

Item	Symbol	HA17903GS	HA17903PS	HA17393	Unit	Note
Supply Voltage	V_{CC}	36	36	36	V	
Differential Input Voltage	$V_{in(diff)}$	V_{CC}	V_{CC}	V_{CC}	V	
Input Voltage	V_{in}	−0.3 to +36	−0.3 to +36	−0.3 to +36	V	
Power Dissipation	P_T	570*	570**	570**	mW	1
Output Short-circuit Current	I_{OS}	Continuation possible	Continuation possible	Continuation possible		2
Operating Temperature	T_{opr}	−40 to +85	−20 to +75	0 to +70	°C	
Storage Temperature	T_{stg}	−65 to +150	−55 to +125	−55 to +125	°C	

Note) 1. * Value at Ta≦75°C. In case of more than it, 7.6mW/°C derating shall be performed.
** Value at Ta≦55°C. In case of more than it, 8.3mW/°C derating shall be performed.
2. Short-circuit between the output and V_{CC} will be a cause to destroy the circuit.
The maximum output current is about 20mA for any supply voltage.

■ ELECTRICAL CHARACTERISTICS-1 (V_{CC}=5V, Ta=25°C)

Item	Symbol	Test Condition	min	typ	max	Unit	Note
Input Offset Voltage	V_{IO}		—	2.0	5.0	mV	1
Input Bias Current	I_{IB}	$I_{IN(+)}$ or $I_{IN(-)}$	—	25	250	nA	2
Input Offset Current	I_{IO}	$\lvert I_{IN(+)} - I_{IN(-)} \rvert$	—	3	50	nA	
Common Mode Input Voltage	V_{CM}		3.5	—	—	V	3
	V_{CM}		—	—	0	V	
Supply Current	I_{CC}	All Comparators: R_L=∞, All Channels ON	—	0.8	2.0	mA	
Voltage Gain	A_{VD}	V_{CC}=15V, R_L≧15kΩ	—	200	—	V/mV	
Response Time	t_R	V_{RL}=5V, R_L=5.1kΩ	—	1.3	—	μs	4
Large Signal Response Time	t_{RI}	V_{IN}=TTL Threshold Width. V_{REF}=1.4V	—	300	—	ns	
Output Sink Current	I_{sink}	$V_{IN(-)}$≧1V, $V_{IN(+)}$=0, V_O≧1.5V	6	16	—	mA	
Output Saturation Voltage	$V_{O(sat)}$	$V_{IN(-)}$≧1V, $V_{IN(+)}$=0, I_{sink}=4mA	—	—	400	mV	
Output Leak Current	I_{LO}	$V_{IN(-)}$=0, $V_{IN(+)}$≧1V, V_O=5V	—	0.1	—	nA	

Note) 1. V_{REF}=1.4V and R_S=50Ω, when V_O=1.4V at output switching point.
2. Under Linear Operation.
3. Common mode input voltage or each one of the input signal should not be less than −0.3V.
4. This is a value to 100mV Input Step Voltage with 5mV over drive.

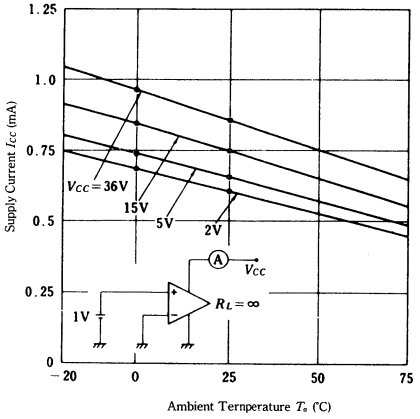
■ ELECTRICAL CHARACTERISTICS-2

(V_{CC}=5V, HA17903GS; Ta=−40 to +85°C, HA17903PS; Ta=−20 to +75°C, HA17393; Ta=0 to +70°C)

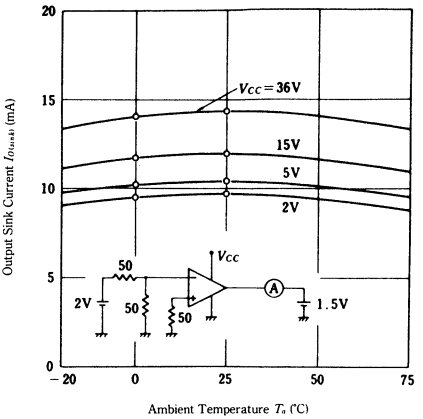
Item	Symbol	Test Condition	min	typ	max	Unit	Note
Input Offset Voltage	V_{IO}		—	9	15	mV	1
Input Offset Current	I_{IO}	$\lvert I_{IN(+)} - I_{IN(-)} \rvert$	—	50	200	nA	
Input Bias Current	I_{IB}	Output Linear Range	—	200	500	nA	
Common Mode Input Voltage	V_{CM}		V_{CC}−2.0	—	—	V	
	V_{CM}		—	—	0	V	
Output Saturation Voltage	$V_{O(sat)}$	$V_{IN(-)}$≧1V, $V_{IN(+)}$=0, I_{sink}≦4mA	—	400	700	mV	
Output Leak Current	I_{LO}	$V_{IN(-)}$=0, $V_{IN(+)}$≧1V, V_O=30V	—	—	1.0	μA	
Differential Input Voltage	$V_{in(diff)}$	All Inputs≧0V	—	—	V_{CC}	V	

Note) 1. V_{REF}=1.4V and R_S=50Ω, when V_O=1.4V at the output switching point.

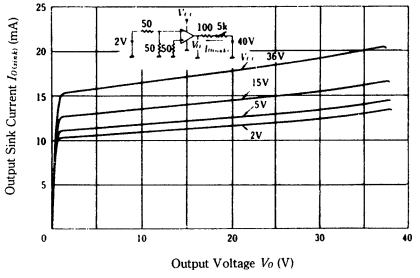
SUPPLY CURRENT VS. AMBIENT TEMPERATURE



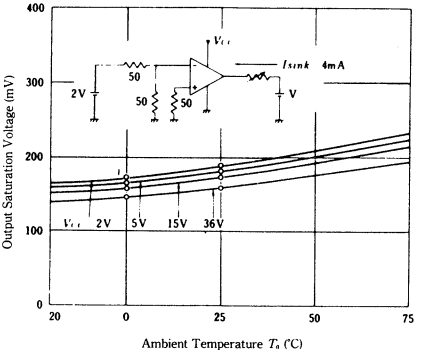
OUTPUT SINK CURRENT VS. AMBIENT TEMPERATURE



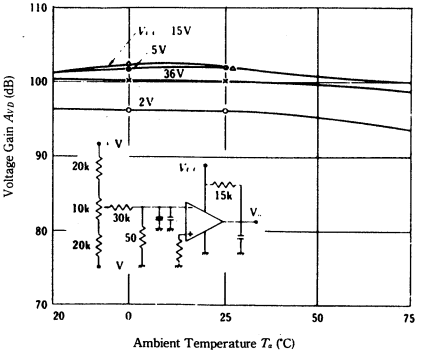
OUTPUT SINK CURRENT VS. OUTPUT VOLTAGE



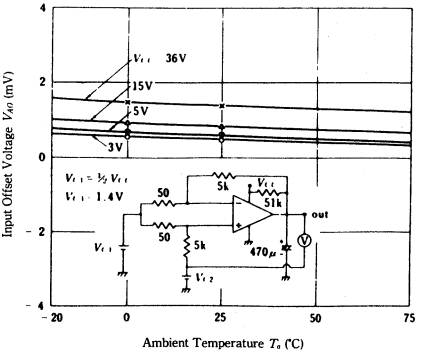
OUTPUT SATURATION VOLTAGE VS. AMBIENT TEMPERATURE



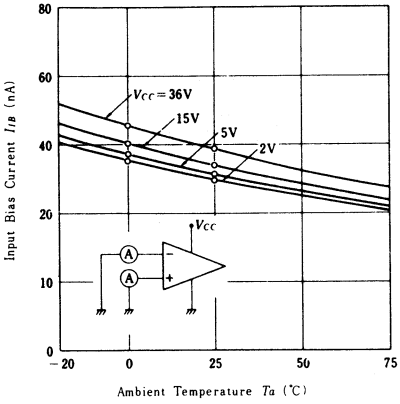
VOLTAGE GAIN VS. AMBIENT TEMPERATURE



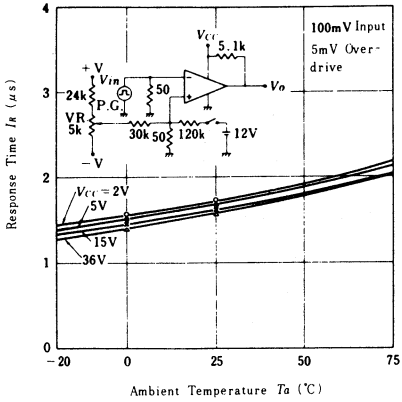
INPUT OFFSET VOLTAGE VS. AMBIENT TEMPERATURE



INPUT BIAS CURRENT VS. AMBIENT TEMPERATURE



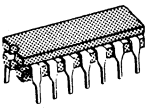
RESPONSE TIME VS. AMBIENT TEMPERATURE



HA1807, HA1813PS ● Voltage Comparator

HA1807, Dual Comparator, and HA1813PS, Single Comparator, can be widely applied to control equipments, since they operate with a single power source.

HA1807



(DG-14)

HA1813PS

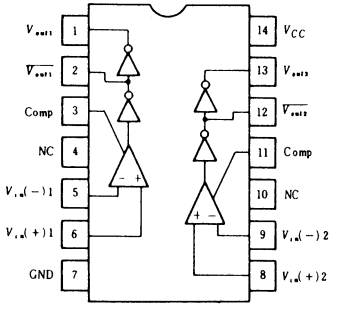
(DP-8)

■ FEATURES

- Operate with single power source.
- Provide complementary outputs (Vout and $\overline{Vout}$) (HA1807)
- Common mode input voltage range is wide.

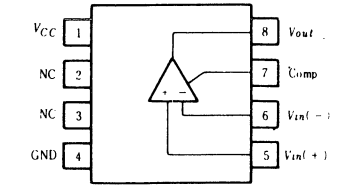
■ PIN ARRANGEMENT

HA1807



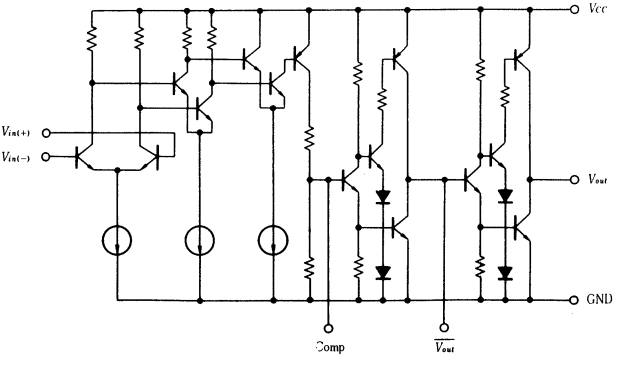
(Top View)

HA1813PS



(Top View)

■ CIRCUIT SCHEMATIC



■ ABSOLUTE MAXIMUM RATINGS ($Ta = 25°C$)

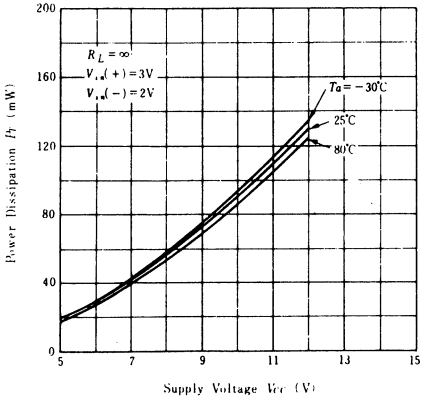
Item	Symbol	HA1807	HA1813PS	Unit
Supply Voltage	V_{CC}	18	18	V
Power Dissipation	P_T*	500	500	mW
Common Mode Input Voltage	V_{CM}	V_{CC}	V_{CC}	V
Differential Input Voltage	$V_{in\,(diff)}$**	±10	±10	V
Operating Temperature	T_{opr}	−30 to +80	−20 to +75	°C
Storage Temperature	T_{stg}	−65 to +150	−55 to +125	°C

Note: * HA1807 : Value at $Ta \leqq 70°C$. In case of more than it, 7.6mW/°C derating shall be performed.
HA1813PS : Value at $Ta \leqq 50°C$. In case of more than it, 8.3mW/°C derating shall be performed.
** Value at $V_{CC} > 10V$. In case of $V_{CC} < 10V$, $V_{in\,(diff)} < V_{CC}$.

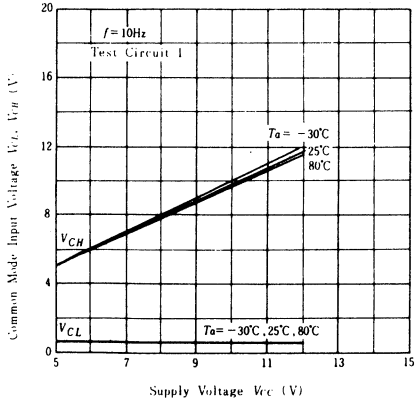
■ ELECTRICAL CHARACTERISTICS ($Ta = 25°C$)

Iten	Symbol	Test Condition		min	typ	max	Unit
Input Offset Voltage	V_{IO}	$V_{CC} = 6V$, $V_{CM} = 3V$, $R_S = 50\Omega$		—	1	5	mV
Input Offset Current	I_{IO}	$V_{CC} = 6V$, $V_{CM} = 1.5V$		—	–	150	nA
Voltage Gain	A_V	$V_{CC} = 5.5V$, $f = 10Hz$		75	100	–	dB
Input Bias Current	I_I	$V_{CC} = 6.5V$, $V_{I1} = 2V$, $V_{I2\ test} = 5.5V$		—	0.5	3	μA
Common Mode Input Voltage	V_{CH}	$V_{CC} = 6.5V$, $f = 10Hz$		5.5	6.4	–	V
	V_{CL}			—	0.6	1	V
Output Voltage	V_{OH}	$V_{CC} = 5.5V$	$I_{OH} = -2mA$	4	5.3	–	V
	V_{OL}		$I_{OL} = 10mA$	—	0.2	0.4	V
Power Dissipation	P_T	$V_{CC} = 6.5V$, $V_{I(+)} = 3V$, $V_{I(-)} = 2V$, $R_L = \infty$		—	36	48.8	mW

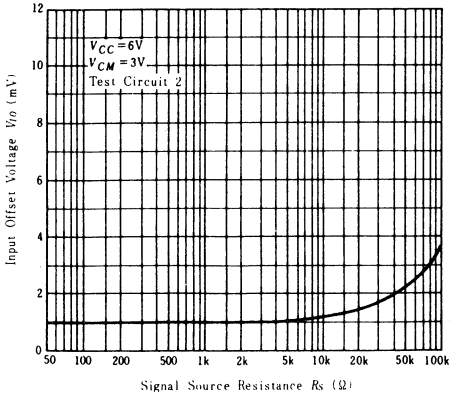
POWER DISSIPATION VS. SUPPLY VOLTAGE



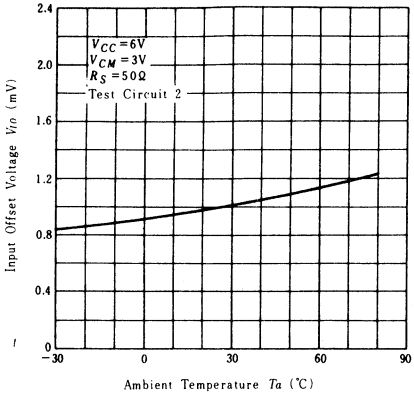
COMMON MODE INPUT VOLTAGE VS. SUPPLY VOLTAGE



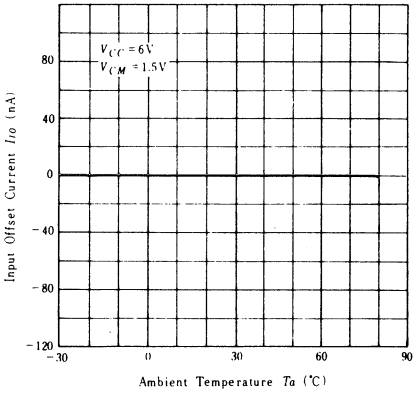
INPUT OFFSET VOLTAGE VS. SIGNAL SOURCE RESISTANCE



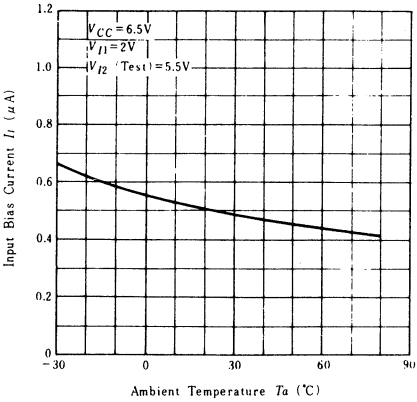
INPUT OFFSET VOLTAGE VS. AMBIENT TEMPERATURE



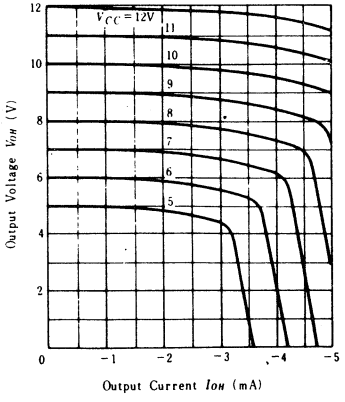
INPUT OFFSET CURRENT VS. AMBIENT TEMPERATURE



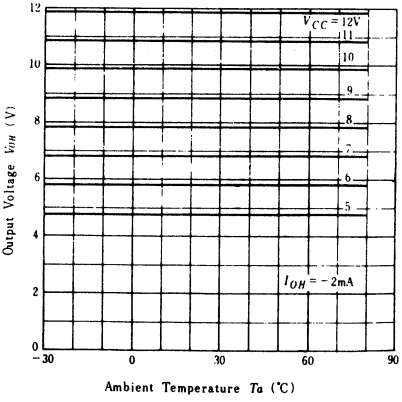
INPUT BIAS CURRENT VS. AMBIENT TEMPERATURE



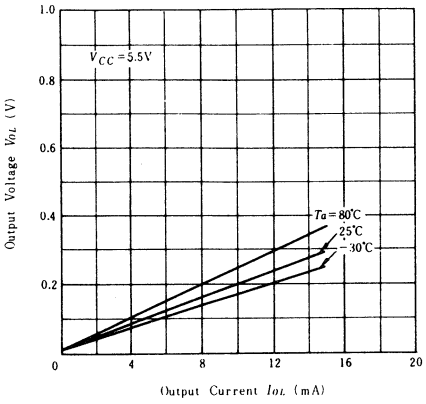
OUTPUT VOLTAGE VS. OUTPUT CURRENT



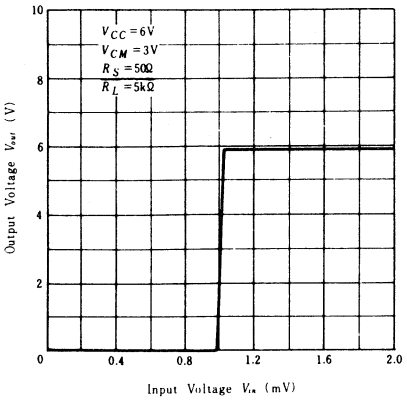
OUTPUT VOLTAGE VS. AMBIENT TEMPERATURE



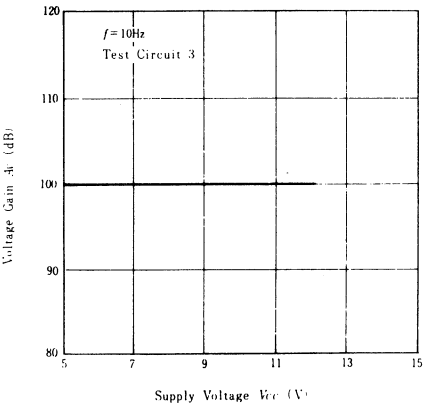
OUTPUT VOLTAGE VS. OUTPUT CURRENT



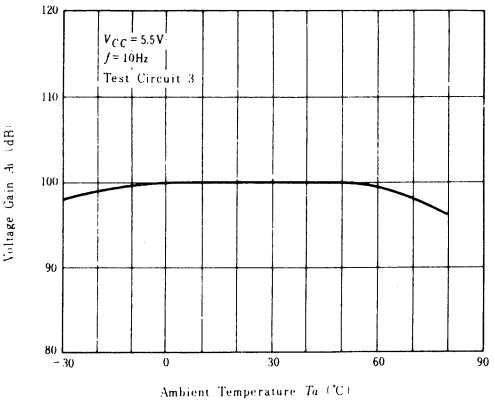
OUTPUT VOLTAGE VS. INPUT VOLTAGE



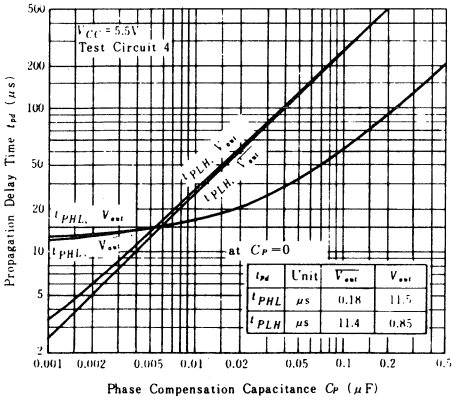
VOLTAGE GAIN VS. SUPPLY VOLTAGE



VOLTAGE GAIN VS. AMBIENT TEMPERATURE



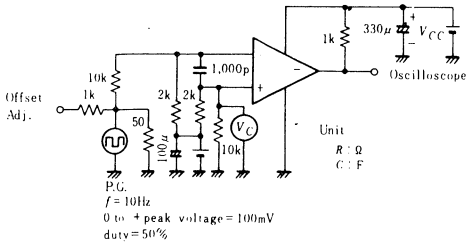
PROPAGATION DELAY TIME VS. PHASE COMPENSATION CAPACITANCE



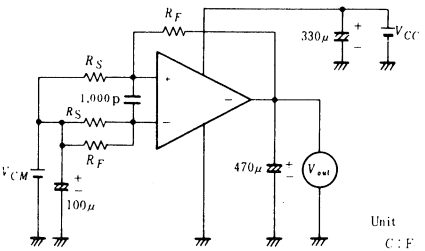
t_{pd}	Unit	$\overline{V_{out}}$	V_{out}
t_{PHL}	μs	0.18	11.5
t_{PLH}	μs	11.4	0.85

■ TEST CIRCUIT

1.



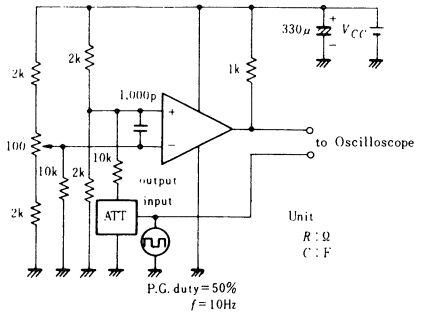
2.



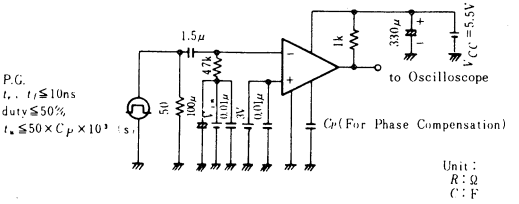
$R_S \leqq R_F / 100$ $\quad V_{CM} = V_{CC}/2$

$$V_{IO} = \frac{R_S (V_{out} - V_{CM})}{R_F + R_S} \text{ (V)}$$

3.

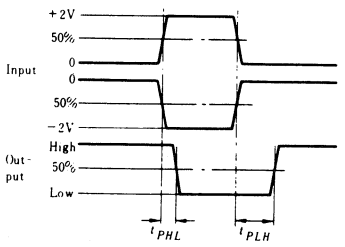


4



Output	V_{in} (V)	v_{in} (V)
V_{out}	4	− 2
V_{out}	2	+ 2

RESPONSE WAVEFORM

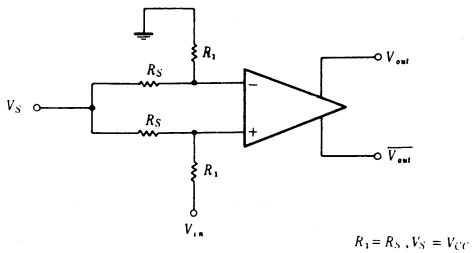


■ HA1807 APPLICATION

HA1807 operates with dual comparator and a power source. The operating supply voltage range is wide, 5 to 8V, and the output is a complementary output with two stages of gate connected in cascade.

1. Waveform Conversion Circuit

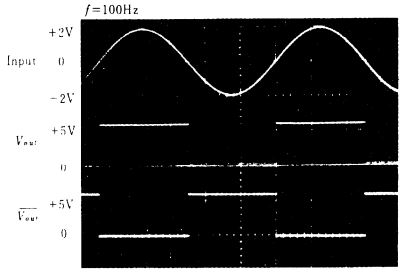
Fig. 1 shows a waveform conversion circuit. The input voltage range is maximum at Rs = R1 and Vs = Vcc, and the output is inverted at the time when the input is zero-crossed.



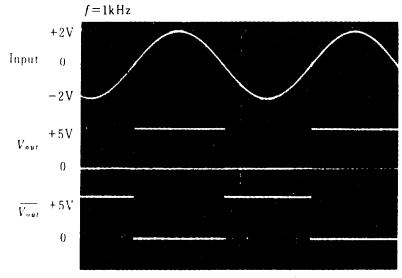
$R_1 = R_S$, $V_S = V_{CC}$

Fig.1 Wave form Converter

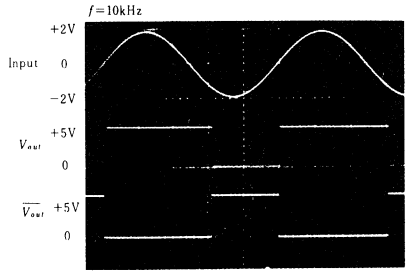
Fig. 2 shows Input and Output Waveforms at Vs = Vcc = 6.0V and R1 = Rs = 100kΩ.



2ms/DIV.



0.2ms/DIV.



20μs/DIV.

$V_s = V_{CC} = 6.0V$

$R_1 = R_s = 100k\Omega$

Fig.2 Operation Waveform of Waveform Converter

2. Schmitt Trigger Circuit

Schmitt Trigger Circuit is a circuit with hysteresis on the input and output characteristics by applying a positive feedback. Fig. 3 show a Schmitt Trigger Circuit.

Fig. 4 shows an example of the Schmitt Trigger Circuit Operation.

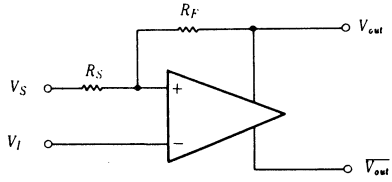


Fig.3 Schmitt Trigger Circuit

Fig.4 Shows an example of the Schmitt Trigger Circuit Operation

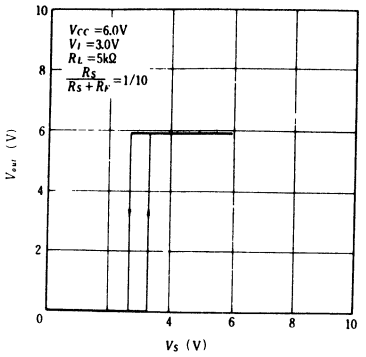


Fig.4(a) Operation Waveform of Schmitt Trigger Circuit (V_{out} – V_S)

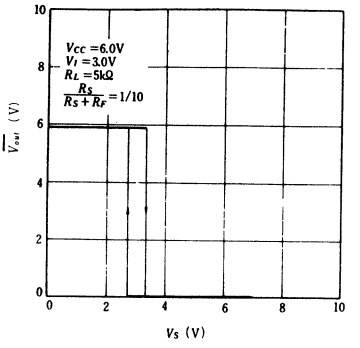


Fig.4(b) Operation Waveform of Schmitt Trigger Circuit ($\overline{V_{out}}$ – V_S)

3. Window Type Comparator

A window type comparator has two reference voltages. The output voltage level is determined according to that whether the voltage is smaller or larger than the two reference voltages.

Fig. 5 shows a circuit of window type comparator, and Fig. 6 shows an example of the operation.

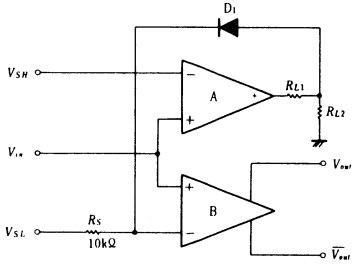


Fig.5 Window Type Comparator

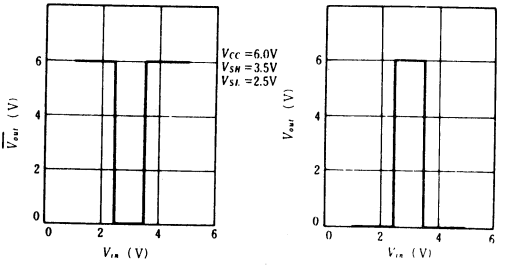
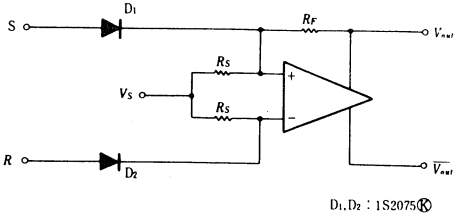


Fig.6 Operation Waveform of Window Type Comparator

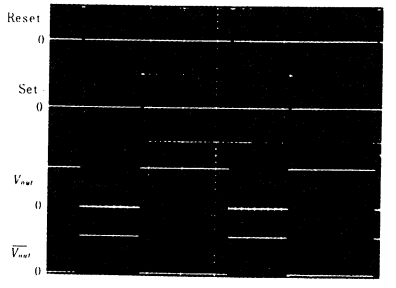
4. Bistable Circuit

Fig. 7 shows a Bistable Circuit (R-S Flip-Flop Circuit), and Fig. 8 shows an example of the operation.



D_1,D_2 : 1S2075Ⓚ

Fig.7 Bistable Circuit



Y-axis : 5V/div V_{CC} =6.0V, V_S =3.0V

X-axis : 2ms/div R_S =10kΩ, R_F =20kΩ

Fig.8 Operation Waveform of Bistable Circuit

5. Parallel Comparing A/D Converter

Fig. 9 and Fig. 10 show circuits of the parallel comparing A/D converters in which the comparator is applied. In this case, the output is converted to BCD (Binary Coded Decimal). This A/D converter can not be used suitably for a precise converter, but it has the features such as high speed conversion and a simple block diagram.

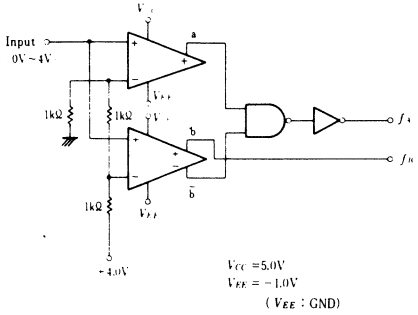


Fig.9 3 Split & 2 Bit A/D Converter

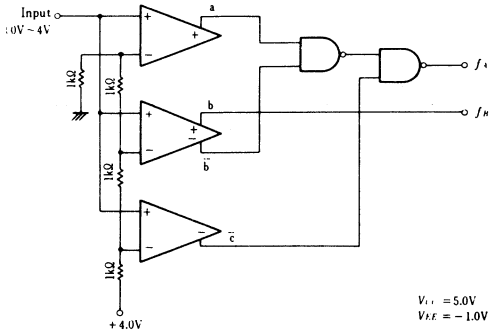


Fig.10 4 Split & 2 Bit A/D Converter

HA1812 Series ●Universal Comparator

HA1812 is general purpose IC, including comparator, buffer amplifier, reference voltage and is designed to be used widely as unit cell of circuit investigation and system designing.

HA1812GS

(DG-8)

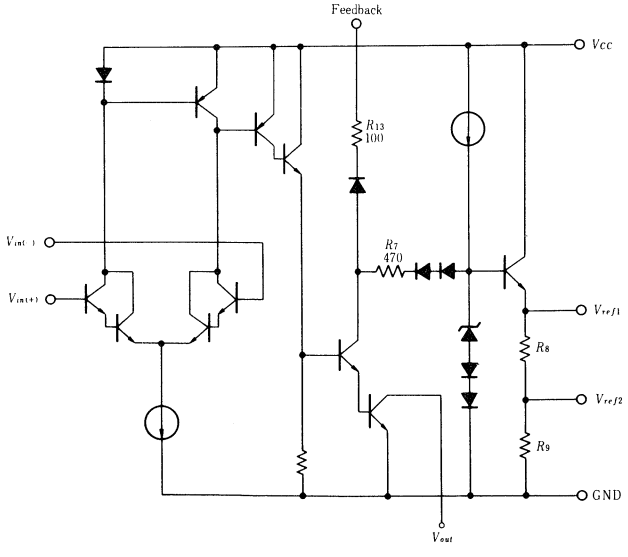
HA1812PS

(DP-8)

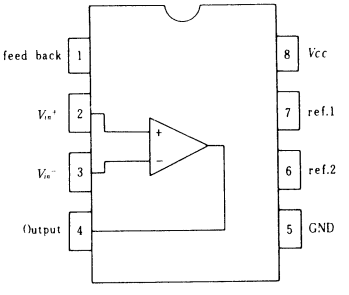
■FEATURES

- Large sink current of 200mA max.
- Capable of becoming Schmitt Trigger (Hysteresis characteristic) Circuit without external resistance.
- Includes reference voltage source.

■CIRCUIT SCHEMATIC



■PIN ARRANGEMENT



(Top View)

■ ABSOLUTE MAXIMUM RATINGS (Ta=25°C)

Item	Symbol	HA1812GS	HA1812PS	Unit
Supply Voltage	V_{CC}	20	20	V
Output Sink Current	I_{sink}	200	200	mA
Common Mode Input Voltage	V_{CM}	V_{CC}	V_{CC}	V
Differential Input Voltage	$V_{in\,(diff)}$	$\pm V_{CC}$*	$\pm V_{CC}$*	V
Reference 1 Source Current	$I_{source\,(ref.1)}$	2.0	2.0	mA
Output Transistor Voltage	V_{out}	40	40	V
Feedback Terminal Current	I_{FB}	±2.0	±2.0	mA
Power Dissipation	P_T**	800	800	mW
Operating Temperature	T_{opr}	−20 to +75	−20 to +75	°C
Storage Temperature	T_{stg}	−65 to +150	−55 to +125	°C

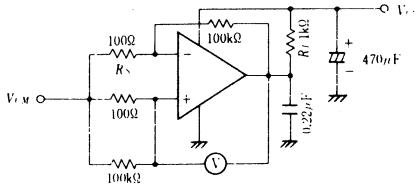
Note) * At V_{CC} >15V, $V_{in\,(diff)}$ max = ±15V.
** In HA1812GS, it is a value under the condition of Ta≦65°C. When Ta is more than 65°C, 7.6mW/°C derating shall be performed.
In HA1812PS, it is a value under the condition of Ta≦45°C. When Ta is more than 45°C, 8.3mW/°C derating shall be performed.

■ ELECTRICAL CHARACTERISTICS (Ta=25°C)

Item	Symbol	Measuring Circuit	Test Condition		min	typ	max	Unit
Supply Current	I_{CC}		V_{CC}=20V, V_{out}(+)=0, V_{in}(−)=3V, R_L=∞		—	18	27	mA
Output Leakage Current	I_{OL}		V_{CC}=V_{out}=20V		—	—	1	μA
"0" Level Output Voltage	V_{OL}		V_{CC}=8V, I_{sink}=100mA		—	0.3	0.5	V
Input Bias Current	I_{IB}		V_{CC}=13.5V, V_{CM}=6.75V		—	—	100	nA
Input Offset Current	I_{IO}		V_{CC}=13.5V, V_{CM}=6.75V		—	0.34	50	nA
Input Offset Voltage	V_{IO}		V_{CC}=13.5V, V_{CM}=6.75V		—	3	15	mV
Reference Voltage	V_{REF}		V_{CC}=13.5V	ref. 1 terminal	5.87	—	6.88	V
				ref. 2 terminal	2.935	—	3.44	V
	ΔV_{REF}	2	V_{CC}=13.5V, R_L=1kΩ	1A	—	15	—	mV
		3	V_{CC}=8→20V, $I_{source\,(ref.1)}$=0	1B	—	50	—	mV
Voltage Gain	A_V	4	V_{CC}=13.5V, R_L=1kΩ, f=10Hz		80	100	—	dB

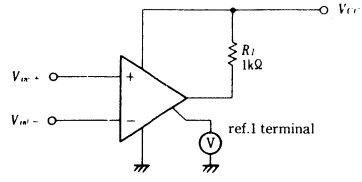
■ TEST CIRCUIT

1. Input Offset Voltage V_{IO}



Input Offset Voltage V_{IO} is 1/1000 of the indication of voltmeter V.

2. Reference Voltage V_{REF} 1A

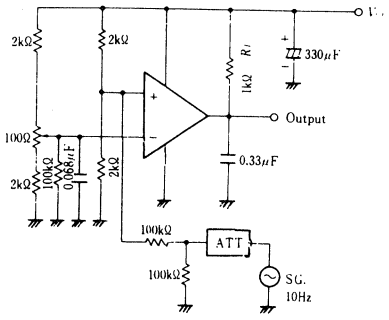


Measure difference voltage of ref. 1 terminal at the time of inverting output with Vin(+), Vin(−) at 3V or 0V.

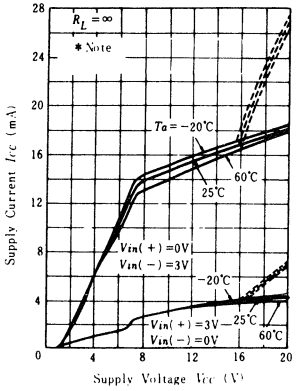
3. Reference Voltage V_{REF} 1B

In the same test circuit as V_{REF} 1A, with output established at 1 level, changing supply voltage Vcc from 8V to 20V, measure difference voltage of ref. 1 terminal.

4. Voltage Gain A_V

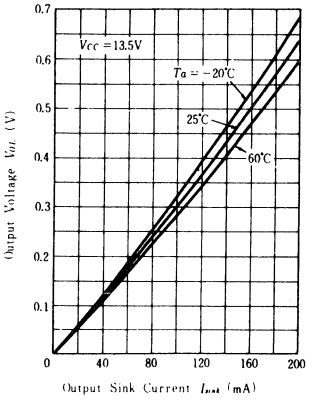


SUPPLY CURRENT VS. SUPPLY VOLTAGE

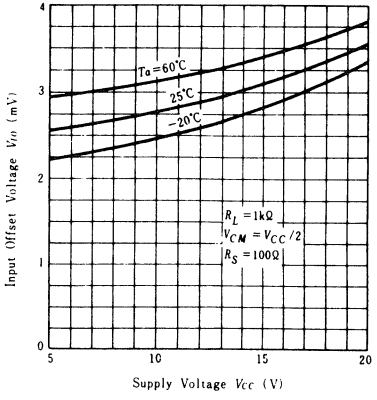


*Note: The broken line is the characteristic at the time of connecting each Input Terminal to V_{CC} and GND.

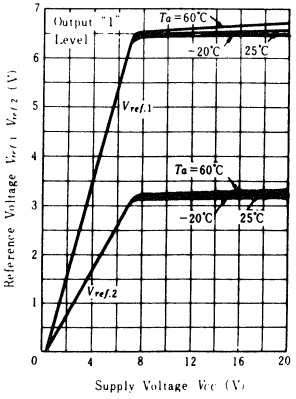
OUTPUT VOLTAGE VS. OUTPUT SINK CURRENT



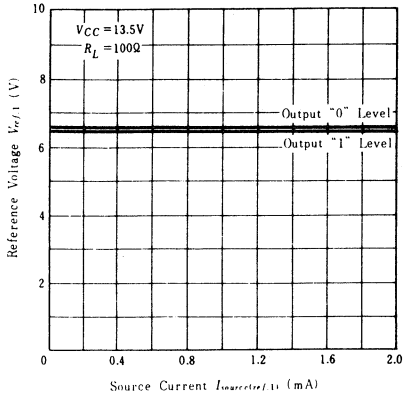
INPUT OFFSET VOLTAGE VS. SUPPLY VOLTAGE



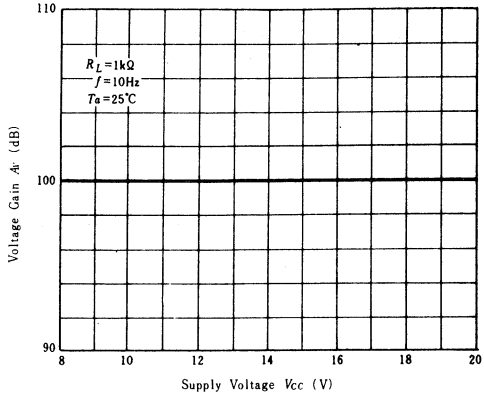
REFERENCE VOLTAGE VS. SUPPLY VOLTAGE



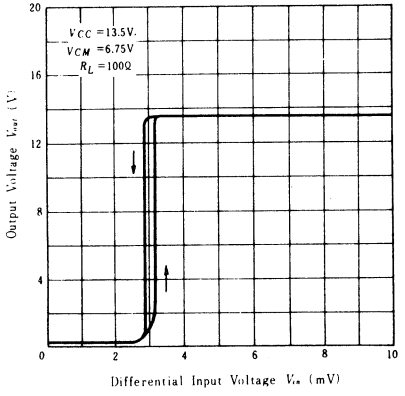
REFERENCE VOLTAGE VS. SOURCE CURRENT



VOLTAGE GAIN VS. SUPPLY VOLTAGE



OUTPUT VOLTAGE VS. DIFFERENTIAL INPUT VOLTAGE



■BASIC OPERATION DESCRIPTION

The following describes the circuit operation of HA1812.

1. Differential Amplifier and Output Terminal Vout

Q_3, Q_4 and Q_5, Q_6 are Differential Amplifier of Darlington Connection, and signals amplified at this stage are further applied to the base of Q_{16} through Q_8, Q_9, Q_{10}. Q_{16} is the open collector in order to be able to drive load directly, and its sink current is designed largely with the maximum at 200mA when Ambient Temperature is 25°C.

Q_1 and Q_2 are provides current mirror connection at the collector load of Q_3, Q_4 and Q_5, Q_6 and the progress of voltage gain are designed.

2. Feedback Terminal

Feedback terminal is connected to the collector of Q_{10} through R_{13} and R_{21}. The phase of this Feedback terminal is the same phase as the collector of Output Transistor Q_{16}, and used by feedback to positive input terminal at the time of Schmitt Trigger connection. Further, since values of R_{13}, R_7 affect hysteresis characteristic, its resistance value is shown in the following.

R_{13} = 100Ω ± 30%

R_7 = 470Ω ± 30%

3. Constant-Current-Circuit

The circuit formed through R_{10}, R_{11}, Q_{20}, Q_{19}, Q_7 is constant-current circuits, and attracts currents with a small dependance on supply voltage from each circuit.

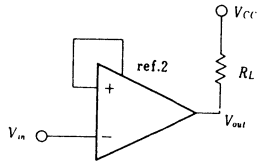
4. Reference Voltage

Q_{17}, ZD_1, Q_{14}, Q_{15} are the circuits which produce reference voltage, and have almost constant current flown with a small dependance on supply voltage to ZD_1, and so stabilize cathode voltage of Zener Diode ZD_1.

Q_{14} and Q_{15} are diodes for temperature compensation of Zener Diode. Q_{13} is the transistor for supplying stabilized voltage through ZD_1, to the two terminals of Reference 1 and Reference 2.

EXAMPLES OF APPLICATION CIRCUITS

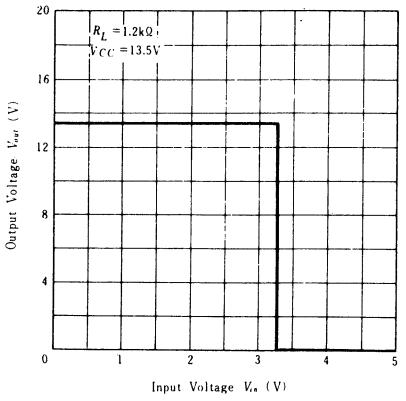
1. Negative Input Comparator (When fundamental voltage is set at Vref.2)



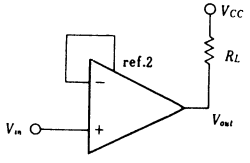
HA1812

Note) $V_{ref.2}$ is 3.27V.

OUTPUT VOLTAGE VS. INPUT VOLTAGE



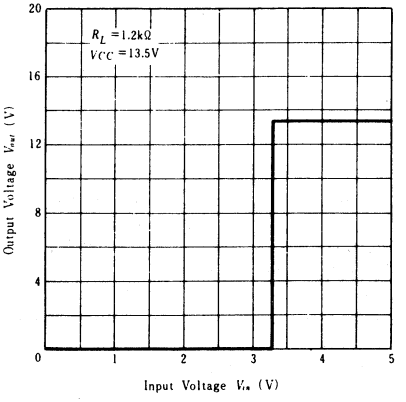
2. Positive Input Comparator (When reference voltage is set at Vref.2)



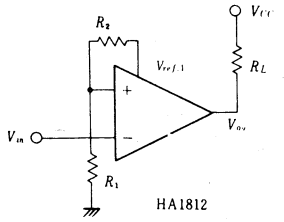
HA1812

Note) $V_{ref.2}$ is 3.27V.

OUTPUT VOLTAGE VS. INPUT VOLTAGE



3. Comparator when Vref.1 is divided by resistance at R_1, R_2 and set at Reference Voltage.

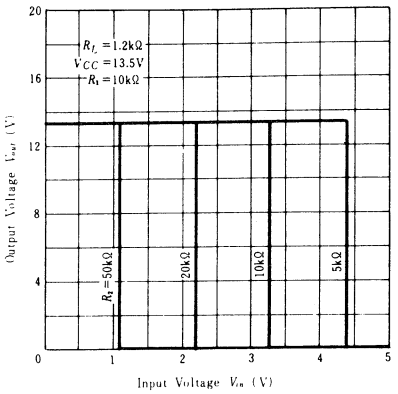


Note) V_{ref1} is 6.53V.

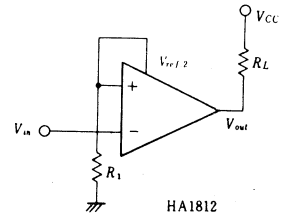
Threshold voltage V_{TH} is found by the following equation.

$$V_{TH} = \frac{6.53R_1}{R_1 + R_2} \text{ (V)}$$

OUTPUT VOLTAGE VS. INPUT VOLTAGE



4. Comparator established reference voltage by ref.2 and R_1.



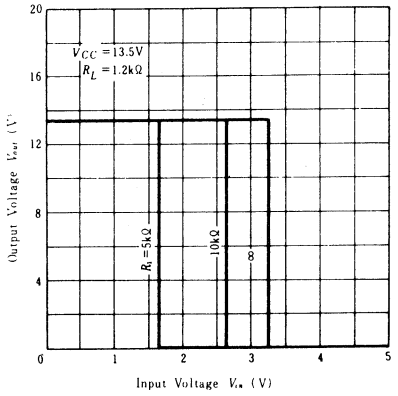
Note)

Threshold voltage V_{TH} is found by the following equation.

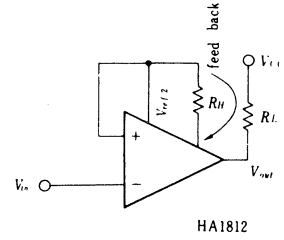
$$V_{TH} = \frac{6.53R_1}{10 + 2R_1} \text{ (V)}$$

Unit of R_1 : kΩ

OUTPUT VOLTAGE VS. INPUT VOLTAGE



5. Schmitt Trigger Circuit 1.



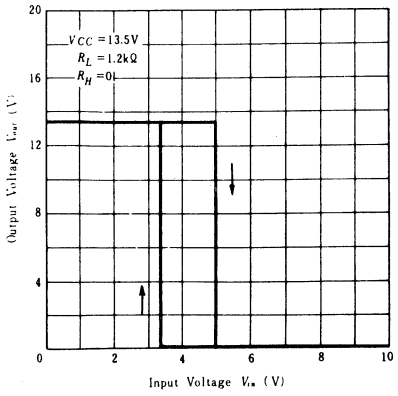
Note) Threshold voltage V_{TL}, V_{TH} are found by the following equations.

$V_{TL} = V_{ref2} = 3.2$ (V)

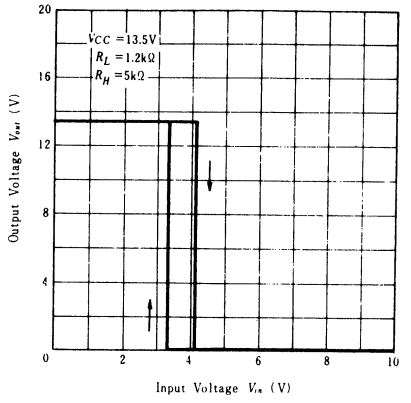
$$V_{TH} = V_{TL} + \frac{10}{R_H + 5.48} \text{ (V)}$$

Unit of R_H : kΩ

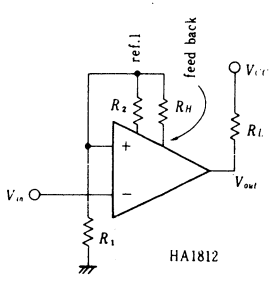
OUTPUT VOLTAGE VS. INPUT VOLTAGE (1)



OUTPUT VOLTAGE VS. INPUT VOLTAGE (2)



6. Schmitt Trigger Circuit.2.



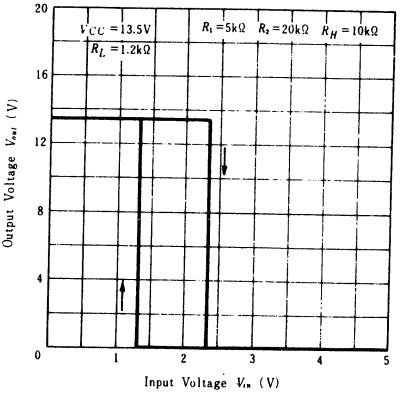
Note) Threshold voltage V_{TL}, V_{TH} are found by the following equation.

$$V_{TL} = \frac{6.53}{1+(R_2/R_1)} \text{ (V)}$$

$$V_{TH} = \frac{6.53}{1+(R_2/R_1)+a} \text{ (V)}$$

$$a = R_2/(570+R_H)$$

OUTPUT VOLTAGE VS. INPUT VOLTAGE



DATA SHEETS

Voltage Regulators

HA16654PS/FP ●500kHz Switching Regulator Controller for PWM Control

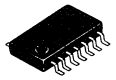
HA16664PS/FP ●200kHz Switching Regulator Controller for PWM Control

The HA16654PS/FP and HA16664PS/FP are ICs for PWM control switching regulator which drives a power MOSFET at high speed at high frequency. The standby current is limited to as small as 1.5mA (typ.). These devices incorporate totem pole circuits suited for high-speed pushpull operation at the Output stage, accomplishing high-speed switching of rising time t_r = 80ns (typ.) and falling time t_f = 40ns (typ.) at 20V swing.

HA16654PS
HA16664PS

(DP-8)

HA16654FP
HA16664FP



(FP-14D)

■ FUNCTIONS

- Reference voltage circuit.
- Triangular waveform oscillation circuit.
- PWM comparator circuit.
- Low-input malfunction protection circuit.
- Output driver circuit.
- Soft start & quick shut function.
- Adjustable dead band.

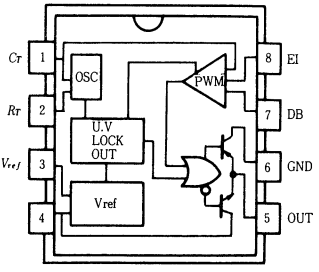
■ FEATURES

- High speed switching: t_r=80ns (typ.). t_f=40ns (typ.).
- High frequency operation: HA16654PS/FP (f=100k to 500kHz)
  HA16664PS/FP (f=100k to 200kHz)
- Low power dissipation 2mA max. in standby state. at V_{IN}=20V
- 5V reference voltage
- Low-input malfunction protection.
  (High threshold voltage: 10V, Low threthold voltage: 8V).
- Dead band width is adjustable.
- Output pulse width control range enlarged (0 to 80%).
- Soft start & quick shut functions provided.
- Signal Output. (totem pole)

Symbol	Pin name	Symbol	Pin name
C_T	Timing Capacitor	EI	Error Input
R_T	Timing Resistor	DB	Dead Band
V_{ref}	Reference Voltage	GND	Ground
V_{IN}	Input Voltage	OUT	Driver Output

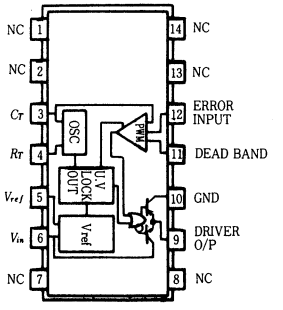
■ PIN ARRANGEMENT

- HA16654PS, HA16664PS



(Top View)

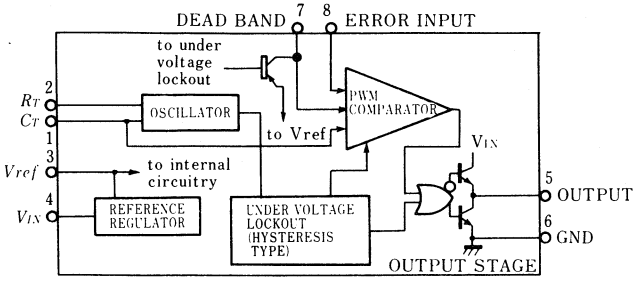
- HA16654FP, HA16664FP



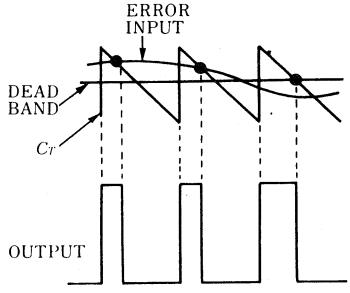
(Top View)

HITACHI

■ BLOCK DIAGRAM



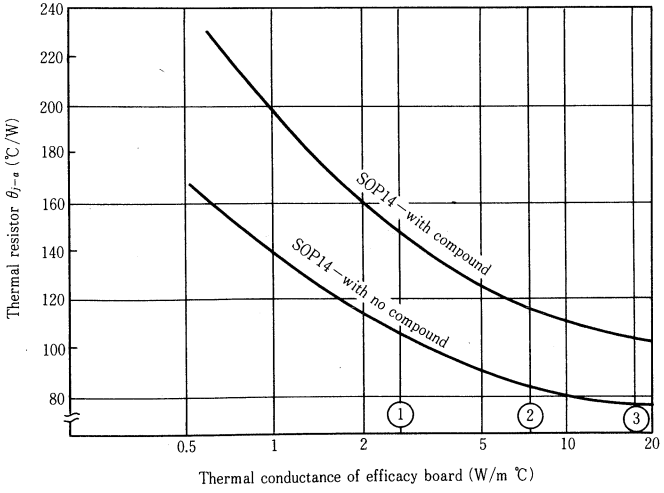
Waveform timing

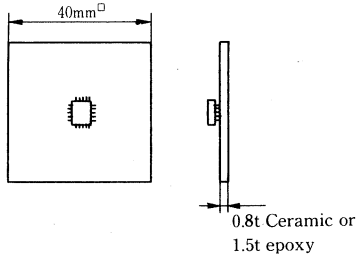


■ ABSOLUTE MAXIMUM RATINGS (T_a = 25°C)

Item	Symbol	HA16654PS	HA16654FP	HA16664PS*	HA1664FP**	Unit
Power Supply Voltage	V_{IN}	+40	+40	+40	+40	V
Collector Current (Push Pull)	I_O	20	20	20	20	mA
Comparator Input Voltage	V_{COM}	V_{ref}+0.3	V_{ref}+0.3	V_{ref}+0.3	V_{ref}+0.3	V
R_T Input Current	I_{RT}	1	1	1	1	mA
Power Dissipation	P_T	680*	680**	680*	680**	mW
Operation Temperature Range	T_{opr}	−20 to +85	−20 to +85	−20 to +85	−20 to +85	°C
Storage Temperature Range	T_{stg}	−55 to +125	−55 to +125	−55 to +125	−55 to +125	°C

**: Tjmax is shown as follows.
Tjmax = θj-a • $P_C$max + Ta (θja; Thermal resistor between junction and atmosphere at set board use).
The wiring density and the material of the set board must be chosen for thermal conductance of efficacy board.
And $P_C$max cannot be over the value of P_T.





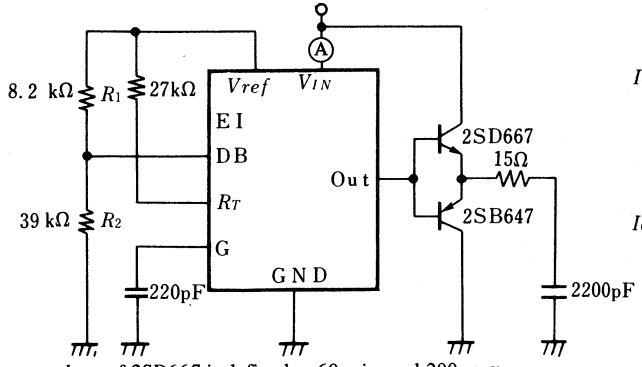
① Glass epoxy board of 10% wiring density
② Glass epoxy board of 30% wiring density
③ 96% aluminum cerdip board

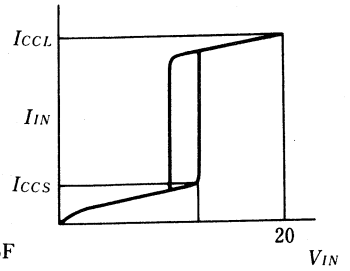
■ ELECTRICAL CHARACTERISTICS

● HA16654PS/FP (T_a=25°C, V_{IN}=20V, C_T=220pF, R_T=27kΩ at f≒500kHz)

Item	Symbol	Test Condition	min.	typ.	max.	Unit	Note
< Reference Section >							
Output Voltage			4.75	5.00	5.25	V	
Line Regulation	L_{ine}	V_{IN}=7.3~11V	–	–	100	mV	
		V_{IN}=11~40V	–	10	25	mV	
Load Regulation	L_{oad}	I_o=0 to 10mA	–	5	16	mV	
Temperature Stability	V_{RTC}		–	-26	–	ppm/°C	
Short Circuit Current	I_{OS}	V_{ref}=0V	10	35	–	mA	
< Oscillator Section >							
Maximum Frequency	F_{max}	C_T=220pF	500	–	–	kHz	
Minimum Frequency	F_{min}	C_T=560pF	–	–	100	kHz	
Initial Accuracy			–	–	±10	%	
Voltage Stability	f_{aT}	V_{IN}=11 to 40V	–	–0.02	±1.0	%	
< PWM Comparator Section >							
Minimum Duty Cycle	D_u		80	–	–	%	
Duty Accuracy	D_{dev}	R_1=8.2kΩ, R_2=39kΩ,	–	±1.0	±10	%	
Input Bias Current	I_B	V_{EI}=4V, V_{DB}=0V, or V_{EI}=0V, V_{DB}=4V	–	–	2.0	μA	
< Output Driver >							
Sink Current at *Vin* Low	I_{OS}(Low)	V_{IN}=6V, VCD=0.4V	0.6	1.5	–	mA	
Output Low Level	V_{OL}	I_O (sink)=10mA	–	0.86	1.4	V	
Output High Level	V_{OH}	I_O (source)=10mA	V_{in}-2.2	–	–	V	
Output Rising	t_r		–	80	150	ns	2
Output Falling Time	t_f		–	40	100	ns	2
High Level Threashold	V_{THH}		9	10	11	V	
Low Level Threshold	V_{THL}		7.3	8	9	V	
Hysteresis Width	V_{HRS}		1.5	2.0	2.5	V	
< Total Current Section >							
Standby Current	I_{CCS}		–	1.5	2.0	mA	1
Operation Current	I_{CCL}	R_1=8.2kΩ, R_2=39kΩ, V_{in}=20V	5.0	9.0	13.0	mA	1

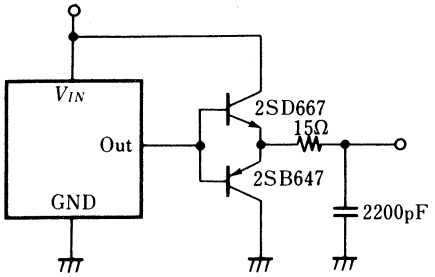
Note 1 $I_{CCS} \cdot I_{CCL}$ measurement circuit.

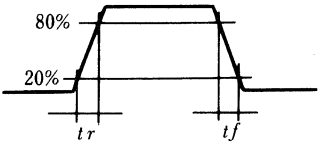




h_{FE} of 2SD667 is defined as 60 min. and 200 max.

Note 2 t_r, t_f measurement circuit





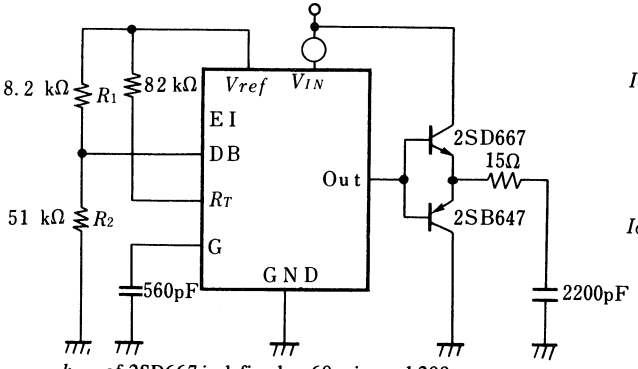
● **HA16664PS/FP** (T_a=25°C, V_{IN}=20V, C_T=560pF, R_T=82kΩ at f≒100kHz)

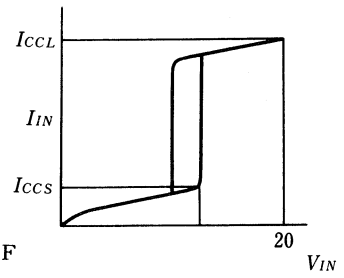
Item	Symbol	Test Condition	min.	typ.	max.	Unit	Note
< Reference Section >							
Output Voltage			4.75	5.00	5.25	V	
Line Regulation	L_{ine}	V_{IN}=7.3~11V	–	–	100	mV	
		V_{IN}=11~40V	–	10	25	mV	
Load Regulation	L_{oad}	I_o=0 to 10mA	–	5	16	mV	
Temperature Stability	V_{RTC}		–	-26	–	ppm/°C	
Short Circuit Current	I_{OS}	V_{ref}=0V	10	35	–	mA	
< Oscillator Section >							
Maximum Frequency	F_{max}	C_T=220pF	200	–	–	kHz	
Minimum Frequency	F_{min}	C_T=560pF	–	–	100	kHz	
Initial Accuracy			–	–	±10	%	
Voltage Stability	f_{aT}	V_{IN}=11 to 40V	–	–0.02	±1.0	%	

< PWM Comparator Section >

Item	Symbol	Test Condition	min.	typ.	max.	Unit	Note
Minimum Duty Cycle	D_u		80	–	–	%	
Duty Accuracy	D_{dev}	R_1=8.2kΩ, R_2=51kΩ	–	±1.0	±10	%	
Input Bias Current	I_B	V_{EI}=4V, V_{DB}=0V, or V_{EI}=0V, V_{DB}=4V	–	–	2.0	μA	
< Output Driver >							
Sink Current at *Vin* Low	I_{OS}(Low)	V_{IN}=6V, V_{CE}=0.4V	0.6	1.5	–	mA	
Output Low Level	V_{OL}	I_O (sink)=10mA	–	0.86	1.4	V	
Output High Level	V_{OH}	I_O (source)=10mA	V_{in}-2.2		–	V	
Output Rising Time	t_r		–	80	300	ns	2
Output Falling Time	t_f		–	40	200	ns	2
High Level Threshold	V_{THH}		9	10	11	V	
Low Level Threshold	V_{THL}		7.3	8	9	V	
Hysteresis Width	V_{HRS}		1.5	2.0	2.5	V	
< Total Current Section >							
Standby Current	I_{CCS}		–	1.5	2.0	mA	1
Operation Current	I_{CCL}	R_1=8.2kΩ, R_2=51kΩ, V_{in}=20V	3.0	5.0	7.0	mA	1

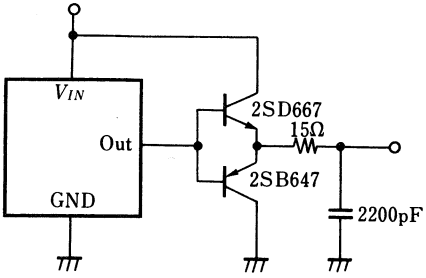
Note 1 I_{CCS} · I_{CCL} measurement circuit.

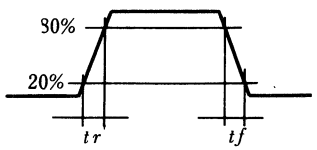




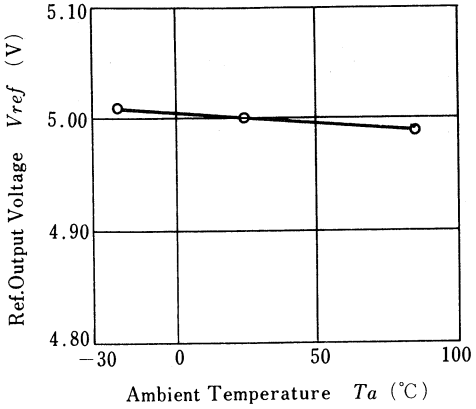
h_{FE} of 2SD667 is defined as 60 min. and 200 max.

Note 2 t_r, t_f measurement circuit

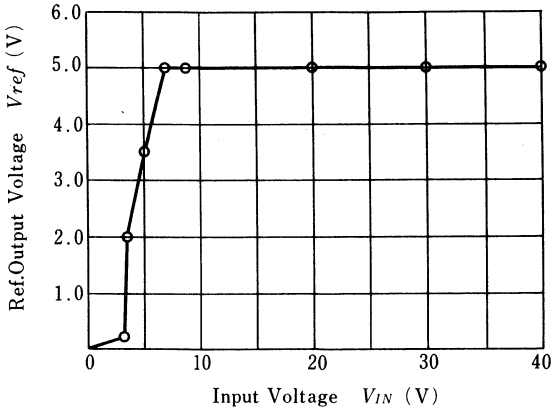




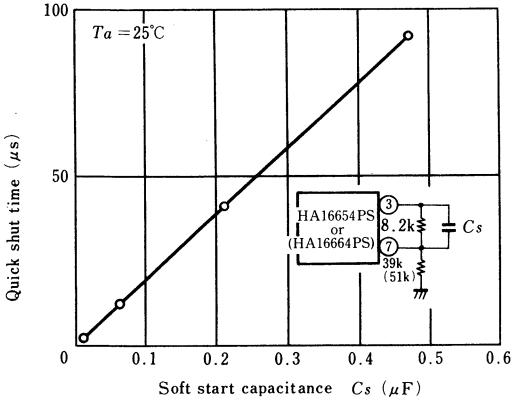
Vref output voltage vs. temperature characteristics



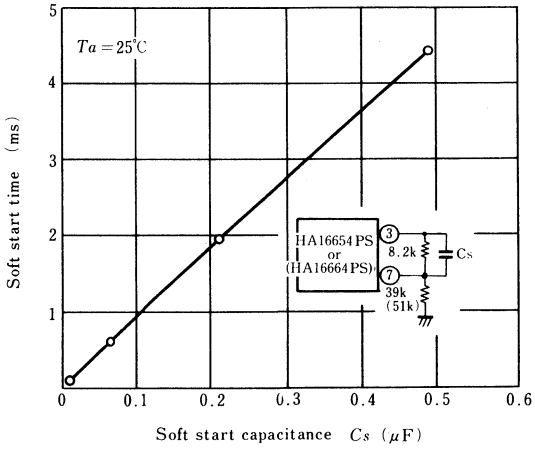
Vref rising characteristics



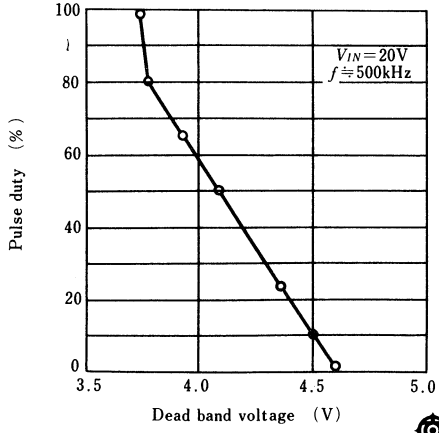
Quick shut time vs. soft start capacitance characteristics



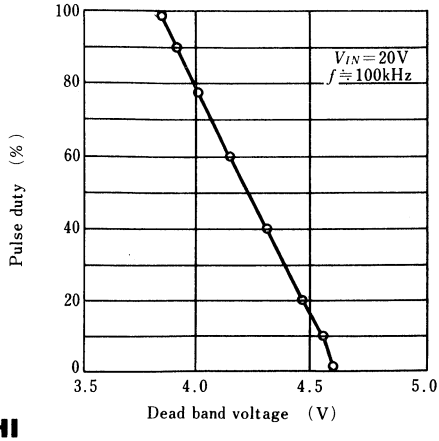
Soft start time vs. soft start capacitance characteristics



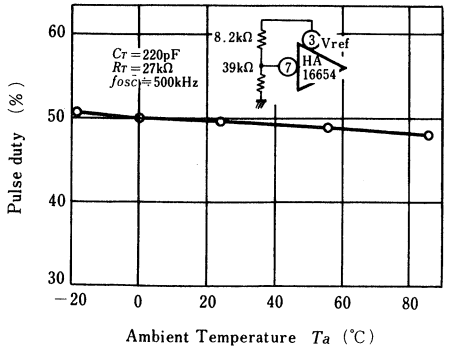
Pulse duty vs. dead band voltage in PWM comp. characteristics (HA16654PS/FP)



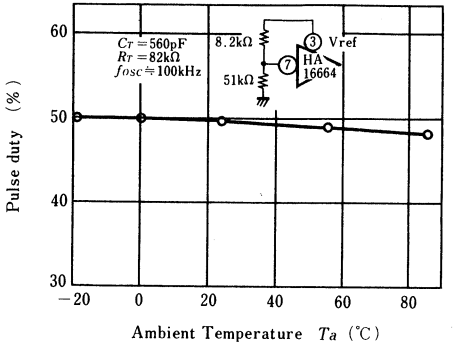
Pulse duty vs. dead band voltage in PWM comp. characteristics (HA16664PS/FP)



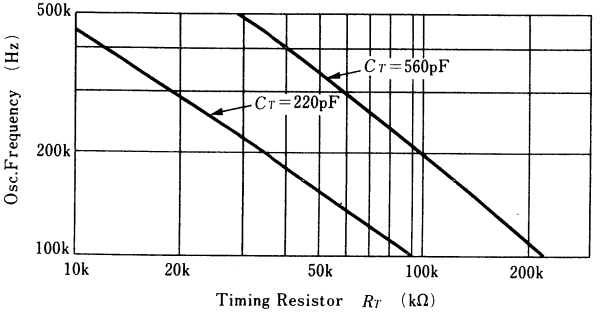
Pulse duty vs. ambient temperature characteristics (HA16654PS/FP)



Pulse duty vs. dead band voltage in PWM comp. characteristics (HA16664PS/FP)

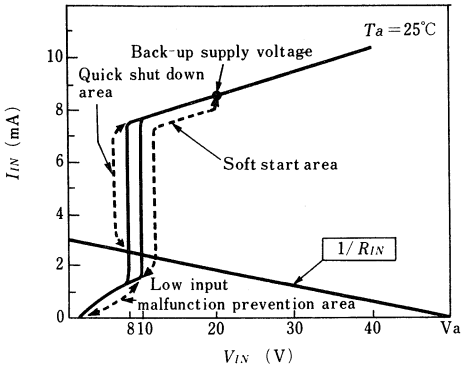


OSC frequency vs. timing resistor characteristics

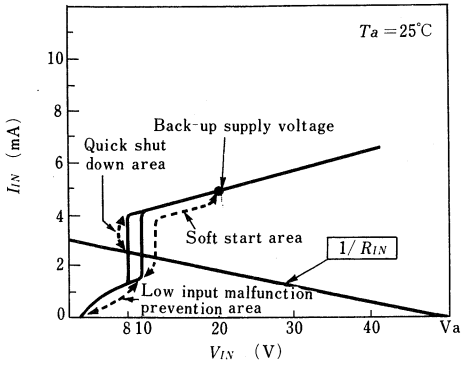


■ V_{IN} BIAS POINT

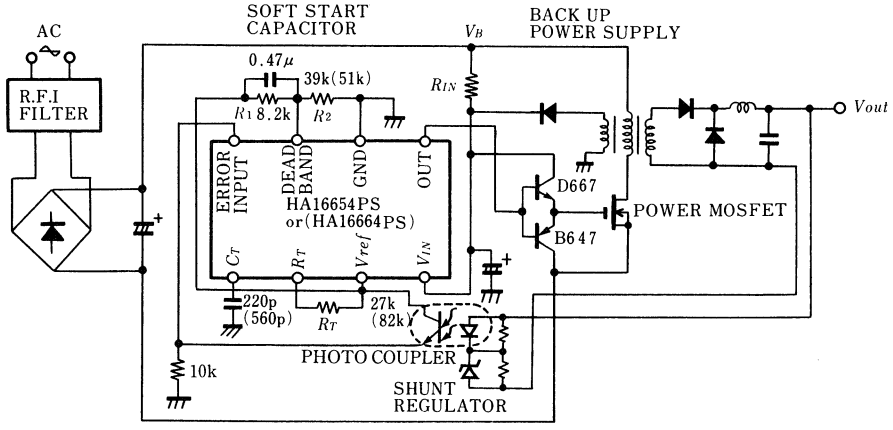
• **HA16654PS**/FP



• **HA16664PS**/FP



■ PRIMARY CONTROL FORWARD CONVERTER SYSTEM

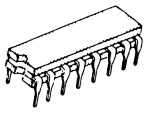


HA17524 Series ● Switching Regulator Controller

FEATURES

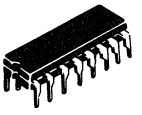
- Pulse Width Modulation (PWM)
- Wide Oscillation Frequency Range . . . . . 450kHz (typ)
- Low Quiecent Current . . . . . 5mA typ
- Good Line Regulation (0.2% typ) and Load Regulation (0.4% typ)
- Provides independent output stage of 2 channels. Wide external circuit application including single end method and push-pull method.
- Reference Power Source Output Stage and Switching Output Stage include current limitting protection circuit.
- Compatible with SG3524

HA17524G



(DG-16)

HA17524P



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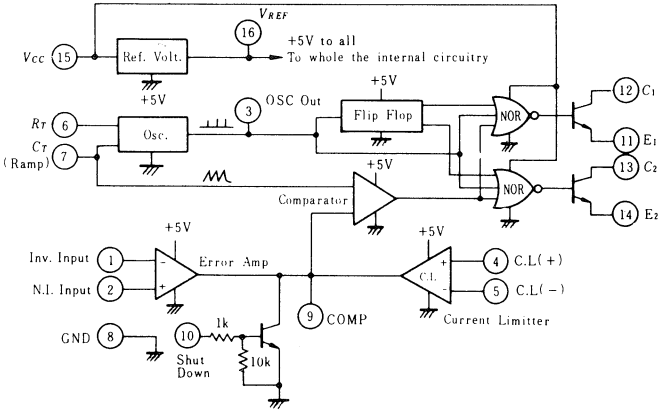
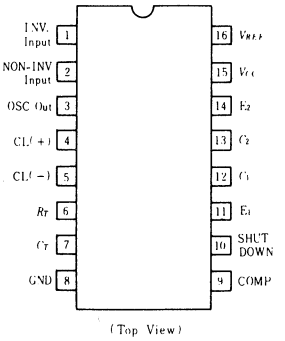
BLOCK DIAGRAM



PIN ARRANGEMENT



(Top View)

ABSOLUTE MAXIMUM RATINGS:

(Unless otherwise specifieb, $Ta = +25°C$)

Item		Symbol	Rating	Unit	Note No
Supply Voltage		V_{CC}	40	V	1.2
Collector Output Current		I_C	100	mA	
Reference Output Current		I_{REF}	50	mA	
Current througn C_T Terminal		I_{CT}	5	mA	
Continnous Total Power Dissipation		P_T	600	mW	3
Operating Free-Air Temperature Range		T_{opr}	−20 to +75	°C	
Strorage Temeperature Range	Cerdip	T_{stg}	−65 to +150	°C	
	Plastic		−55 to +125		

Note: 1. With respect to network ground terminal
2. The reference voltage can be given by connecting the Vcc and 5V reference output pins both to the Supply Voltage. In this configuration, Vcc ~ 6Vmax.
3. HA17524P : Value at $T_a \leqq 52.7°C$. In case of more than it, 8.3mW/°C derating shall be performed.
HA17524G : Value at $T_a \leqq 71°C$. In case of more than it, 7.6mW °C derating shall be performed.

Dissipation Derating Table

Package	Power Rating	Derating Factor	Above Ta
P	600mW	8.3mW/°C	52.7°C
G	600mW	7.6mW/°C	71°C

HITACHI

■ELECTRICAL CHARACTERISTICS (V_{CC}=20V, f=20kHz, Ta=25°C)

Item		Symbol	Test Conditions	min	typ	max	Unit
Regulator	Output Voltage	V_{REF}		4.6	5.0	5.4	V
	Input Regulation	$\delta V_{O\,Line}$	V_{CC}=8 to 40V	—	10	30	mV
	Ripple Rejection	R_{REJ}	f=120Hz	—	66	—	dB
	Output Regulation	$\delta V_{O\,Load}$	I_{out}=0 to 20mA	—	20	50	mV
	Output Voltage Change With Output Temperature	$\delta V_O/\delta Ta$	Ta=0 to +70°C	—	0.3	1.0	%
			Ta=−20 to +75°C	—	0.4	1.36	%
	Short-Circuit* Output Current	I_{OS}	V_{REF}=0	—	100	—	mA
Error Amplifier	Input Offset Voltage	V_{IO}	V_{IC}=2.5V	—	2	10	mV
	Input Bias Current	I_I	V_{IC}=2.5V	—	2	10	μA
	Open-Loop Voltage Gain	A_{VD}		—	60	—	dB
	Common-Mode Iuput Voltage Range	V_{CM}	Ta=25°C	1.8to3.4	—	—	V
	Common-Mode Rejection Ratio	CMR		—	70	—	dB
	Unity-Gain Bandwidth	BW		—	3	—	MHz
	Output Swing	$V_{OP\,P}$		0.5	—	3.8	V
Oscillator	OSC. Frequency	f	C_T=0.001μF, R_T=2kΩ	—	450	—	kHz
	Standard Deviation of Frequency	Δf	V_{CC}=8 to 40V, R_T=1.8 to 100kΩ C=Const	—	5	—	%
	Frequency Change with Temperature	δf_{Line}	V_{CC}=8 to 40V	—	—	1.0	%
		$\delta f/\delta Ta$	Ta=0 to +70°C	—	5.0	10	%
			Ta=−20 to +75°C	—	5.0	13.6	%
	Output Amplitude	$V_{3\,(peak)}$	3Pin	—	3.5	—	V
	Ouput Pulse Width	T_P	C_T=0.01μF, 3Pin	—	0.5	—	μs
Comparator	Maximum Duty Cycle	D_{max}		45	—	—	%
	Input Threshold Voltage	V_{th} 0	duty=0	—	1.0	—	V
		V_{thmax}	duty=max	—	3.5	—	V
	Input Bias Current	I_I		—	−1	—	μA
Current Limiter	Input Voltage Range	V_{IS}		−0.7 to +1.0	—	—	V
	Sense Voltage	V_S	V(Pin9)=2V, Ta=25°C V(Pin2)−V(Pin1)≧50mV	180	200	220	mV
	Sense Voltage Change with Temperature	$\delta V_S/\delta Ta$	Ta=−20 to +75°C	—	0.2	—	mV/°C
Output	Collector-Emitter Breakdown Voltage	V_{CE}		40	—	—	V
	Collector Off-State Current	I_{Leak}	V_{CE}=40V	—	0.01	50	μA
	Collector-Emitter Saturation Voltage	$V_{CE(sat)}$	I_C=20mA	—	1	2	V
	Emitter Output Voltage	V_E	V_{CC}=20V, I_E=−250μA	17	18	—	V
	Turn-off Voltage Rise Time	t_r	R_C=2kΩ	—	0.2	—	μs
	Turn-on Voltage Fall Time	t_f		—	0.1	—	μs
Total Device	Standby Current	I_{ST}	V_{CC}=40V, V_2=2V, Pins 1,4,7,8,9,11,14, grounded All other pins open.	—	5.0	10	mA

Note) *Duration of the short-circuit should not exceed one second.

APPLICATION NOTE

- Principal in HA17524 Operation

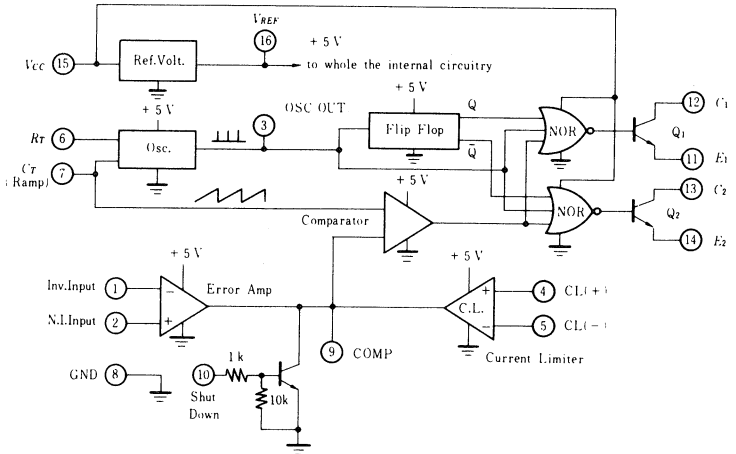
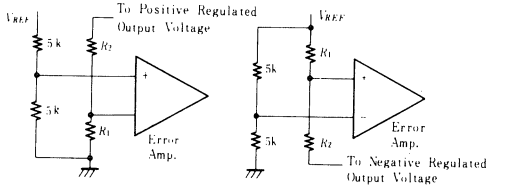


Fig. 1 HA17524 Block Diagram

HA17524 is a switching regulator circuit using Pulsewidth Modulating Method (P.W.M) constructed by the block shown in Fig. 1.

Timing resistance, R_T and timing capacitance, C_T control the oscillating frequency and the C_T is charged by a constant current generated by the R_T. Lump signals (saw-teeth wave) at C_T terminal generated in this oscillator is available for reference input signal to comparators which control the pulse-wideth.



(a) Forward Output stabilizing Source

$$V_o = 2.5V\frac{R_1 + R_2}{R_1}$$

(b) Reverse Output Stabilizing Source

$$Vo = -2.5\left(\frac{R_2 - R_1}{R_1}\right)$$

Fig. 2 Biasing in Error-Amplifier

As shown in Fig. 2 the reference voltage connects to non-inverted on inverted input terminal of error-amplifier via resistance divider.

The output voltage from the error-amplifier is compared with the lump signal of the Timing Capacitance C_T, as shown in Fig. 1 and comparator can provide a signal with modulated pulse width.

This signal, then, control output transistors Q_1 and Q_2, making an open loop to stabilize output voltage.

Commonly connected outputs from the error-amplifier, the current limiter and the shut-down circuit is provided to the comparator, which enable to break output stage by input signal in any one of those circuits.

- Blocks Description

Oscillator; The oscillating frequency f is calculated from the following equations. Fig. 3 shows one example.

$$f \fallingdotseq 1.15/(R_T \cdot C_T)$$

$R_T = 1.8\text{k}\Omega$ to $100\text{k}\Omega$

$C_T = 0.001$ to $0.1\mu\text{F}$

$f = 140\text{Hz}$ to 500kHz

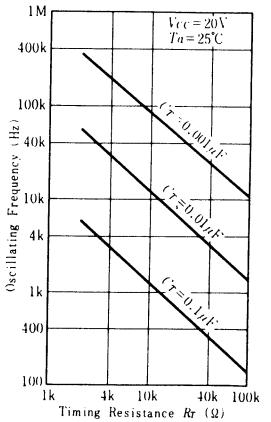


Fig. 3 Oscillating Frequency vs Timing Resistance

Then the lump wave shown in Fig. 4 is available at pin 7, C_T Terminal since the C_T is charged by the constant current I generated by the R_T.

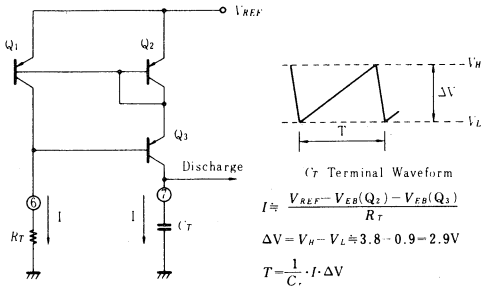


Fig. 4 Oscillating Circuit and C_T Terminal Waveform

The output pulse signal at oscillator is used as elements in Flip-flop circuit and (a synchronous signal of clock-pulse) switching. The pulse-width which can be controlled by the timing capacitor C_T as shown in Fig. 5 provides function to gain a dead time of output.

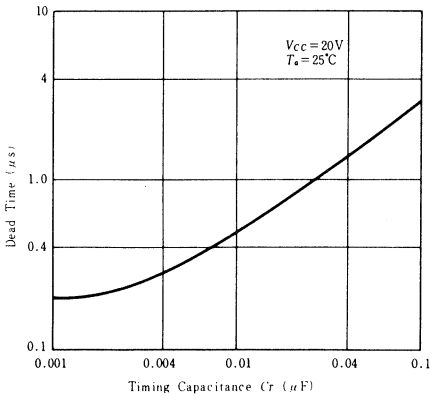


Fig. 5 Dead Time vs Timing Capacitance

Reference Voltage: The regulator (reference voltage: V_{REF} = 5 ± 0.4V) is built in Integrated Circuit. It can be used as reference power supply of error amplifier which determines Output Voltage Output (V_{out}). And also, it is connected as bias source of another circuit in IC.

Error Amplifier: Biasing in error amplifier is shown in the Fig. 2. Input Applied Voltage is required to be set within the range of common-mode Input Voltage (1.8V to 3.4V). If resistor and capacitor are inserted between phase compensation terminal (Pin 9) and GND in series, phase compensation is available.

Current Limiter: Threshold Voltage (V_S) of sense amplifier for current limiter is calculated as follows;

$$V_S = V_{BE}(Q_1) + I_1 R_2 - V_{BE}(Q_2)$$
$$= I_1 R_2$$
$$= 200\text{mV typ.}$$

At Current limiter Sense Amp shown in the Fig. 6, when V + − V − ≧ 200mV, Q_1 turns "ON", Phase compensation terminal becomes low level and Output Switching element is cut off.

Fig. 7 shows an example of detecting current limit. As the range of Input Voltage is −0.7V to +1.0V; detection output of current limit is provided from GND Line.

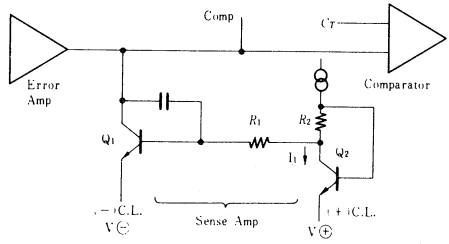
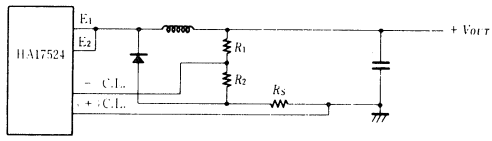


Fig. 7 An Example of detecting current limit



$$I_{O(max)} = \frac{1}{R_S}\left(V_{sense} + \frac{V_O \; R_2}{R_1 + R_2}\right)$$

$$I_{OS} = \frac{V_{sense}}{R_S}$$

$$V_{sense} = 200\text{mV}$$

● Operating waveform at every part

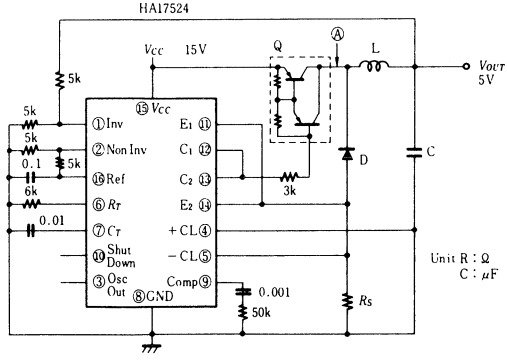


Fig. 8 Breakdown Voltage types Chopper Switching Regulator

Fig. 6 Sense Amplifier for Current Limiter

Fig. 9 shows operating waveform at every part, when the circuit configuration of breakdown voltage type chopper switching regulator (shown in the Fig. 8) is used. Operating Conditions are as follows, f = 20kHz, V_{OUT} = 5V. At output section, two channels are connected in parallel. Operating waveform inside IC is shown at the same time.

■ CAUTIONS

Compared with the conventional series regulator, switching regulator generates high frequency noise by switching current quickly. To reduce noise, the following shall be followed.

1) As a general rule, insert line filter in order to reduce noise at the side of Input.
2) To reduce noise at the side of output,
   (a) Output wiring should be twisted.
   (b) Power Source and output wiring should not be bundled.
   (c) Capacitor should be inserted at the side of load.
   (d) Power frame should be grounded.
3) When grounding frame, output (0V) and Shielding wire, Only one of them should be grounded. Impedance must be as low as possible. And also, Power frame should be grounded. In case of choosing external parts-external switching transistor, diode, coil and etc. –, it is necessary to consider their capacitance and characteristics.

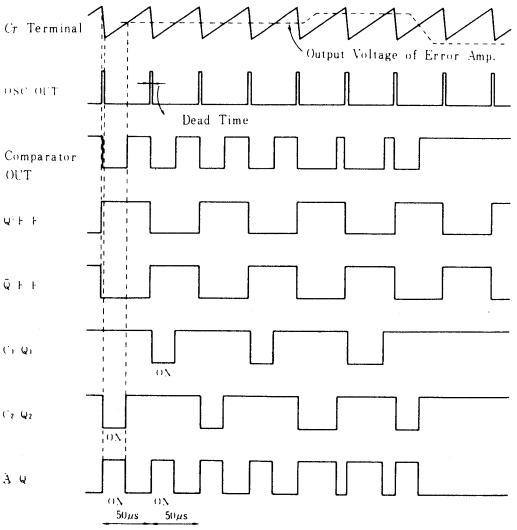


Fig. 9 Operating Timing Chart of each part

● Circuit Applications

Simple polarity switching regulator: Fig. 10 shows the circuit configuration of HA17524 polarity switching regulator which has small current capacitance (V_{OUT} = –5V).

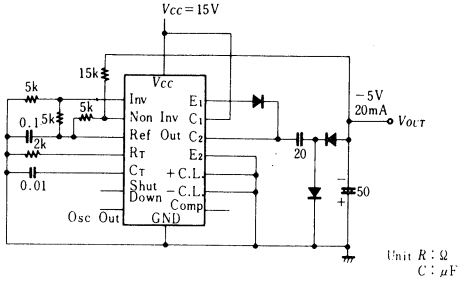


Fig. 10 Simple Type Polarity Conversion

Tracking switching regulator: The circuit configuration of tracking regulator which uses transformer is shown in the Fig. Fig. 11 (V_{OUT} = ±5V).

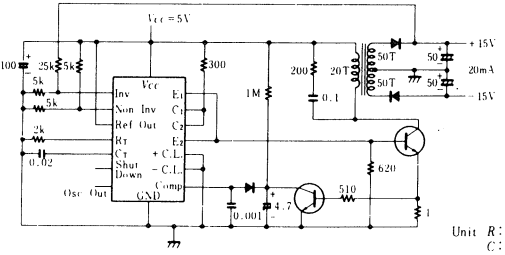


Fig. 11 Tracking Switching Regulator

Push-pull switching regulator: Fig. 12 shows the circuit configuration of Push-pull switching regulator which uses transformer. This system is suited for large power. Output transistors inside HA17524 can drive external switching transistors respectively.

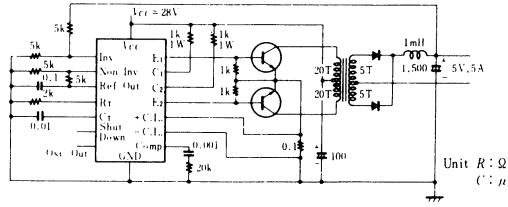
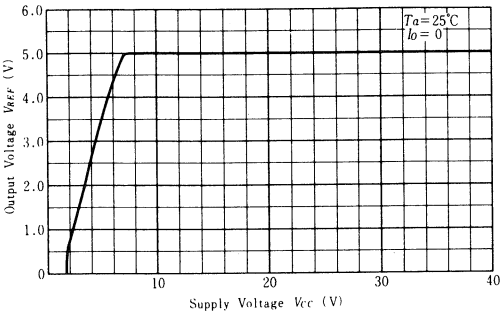
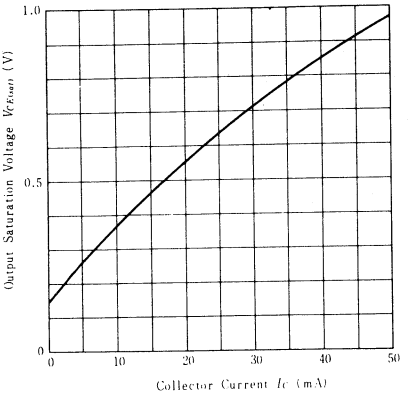


Fig. 12 Push-pull Switching Regulator

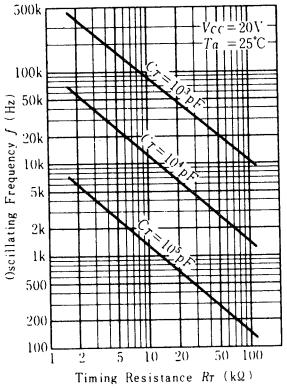
OUTPUT VOLTAGE VS. SUPPLY VOLTAGE



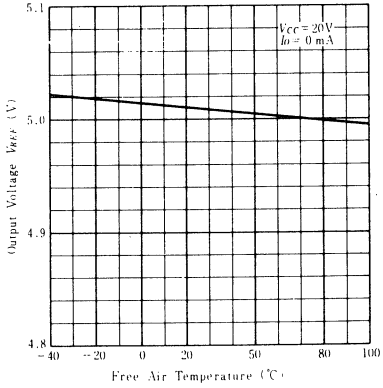
OUTPUT SATURATION VOLTAGE VS. COLLECTOR CURRENT



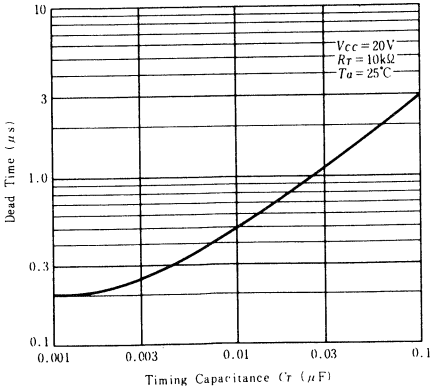
OSCILLATING FREQUENCY VS. TIMING RESISTANCE



OUTPUT VOLTAGE VS. FREE AIR TEMPERATURE



DEAD TIME VS. TIMING CAPACITANCE

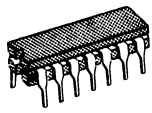


HA17723G,HA17723 ●Voltage Regulator

HA17723, high accuracy voltage regulator for general purposes, features low stand-by current — quiescent current, low temperature drift and high ripple rejection ratio.
Output current above 150mA is also available by adding PNP or NPN transistors externally. This voltage regulator finds wide application, using in series, parallel and as switches.

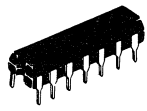
Industrial Use HA17723G
Commercial Use HA17723

HA17723G



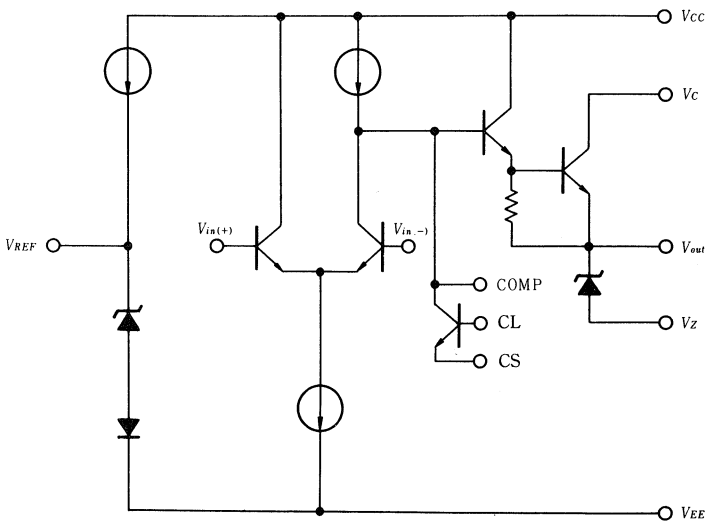
(DG-14)

HA17723

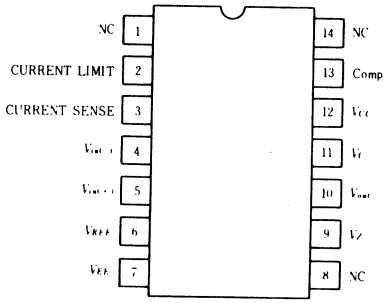


(DP-14)

CIRCUIT SCHEMATIC



PIN ARRANGEMENT



(Top View)

■ ABSOLUTE MAXIMUM RATINGS ($Ta = 25°C$)

Item	Symbol	HA17723G	HA17723	Unit
Supply Voltage	V_{CC}	40	40	V
Input/Output Voltage Differential	$V_{diff.(IN-O)}$	40	40	V
Differential Input Voltage	$V_{in(diff.)}$	±5	±5	V
Maximum Output Current	I_{out}	150	150	mA
Current from V_{REF}	I_{REF}	15	15	mA
Power Dissipation*	P_T	950*	830**	mW
Operating Temperature	T_{Opr}	−20 to +75	0 to +70	°C
Storage Temperature	T_{stg}	−65 to +150	−55 to +125	°C

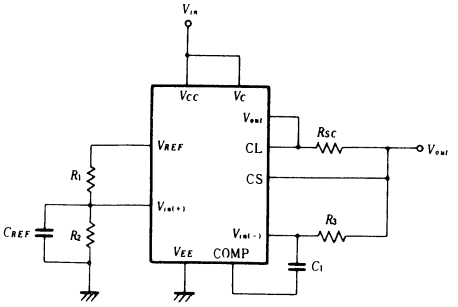
* Derating above 25°C will be 7.6mW/°C
** Derating above 25°C will be 8.3mW/°C

■ ELECTRICAL CHARACTERISTICS ($Ta = 25°C$)

Item	Symbol	Test Conditions		min	typ	max	Unit
Line Regulation	$\delta V_{O\ Line}$	V_{in} = 12 to 15V		—	0.01	0.1	%
		V_{in} = 12 to 40V		—	0.1	0.5	%
		V_{in} = 12 to 15V, Ta = −20 to +75°C *		—	—	0.4	%
		V_{in} = 12 to 15V, Ta = 0 to +70°C		—	—	0.3	%
Load Regulation	$\delta V_{O\ Load}$	I_{out} = 1 to 50mA		—	0.03	0.2	%
		I_{out} = 1 to 50mA Ta = −20 to +75°C *		—	—	0.7	%
		I_{out} = 1 to 50mA Ta = 0 to +70°C		—	—	0.6	%
Ripple Rejection	R_{REJ}	f = 50Hz to 1kHz	C_{REF} = 0	—	74	—	dB
			C_{REF} = 5μF	—	86	—	dB
Average Temperature Coefficient of Output Voltage	$\delta V_O/\delta_T$	Ta = −20 to +75°C *		—	0.003	0.018	%/°C
		Ta = 0 to +70°C		—	0.003	0.015	%/°C
Reference Voltage	V_{REF}	$V_{in} = V_{CC} = V_C$ = 12V, V_{EE} = 0		6.80	7.15	7.50	V
Standby Current	I_{ST}	V_{in} = 30V, I_L = 0		—	—	4.0	mA
Short Circuit Current Limit	I_{SC}	R_{SC} = 10Ω, V_{out} = 0		—	65	—	mA

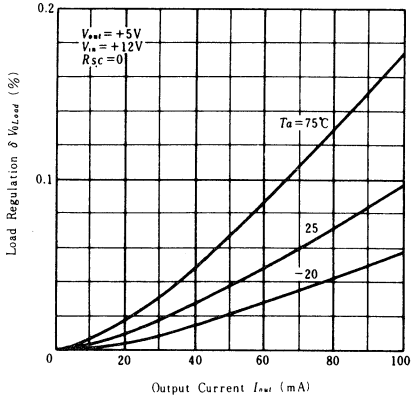
* HA17723G Only

ELECTRICAL CHARACTERISTICS MEASURING CIRCUIT

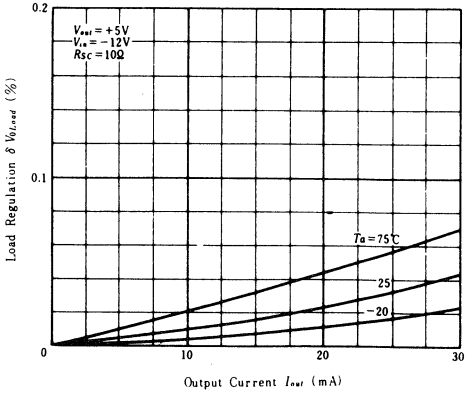


$V_{in} = V_{CC} = V_C = 12V$, $V_{EE} = 0$
$V_{out} = 5.0V$, $I_L = 1mA$
$R_{SC} = 0$, $C_1 = 100pF$, $C_{REF} = 0$
$R_2 \fallingdotseq 5k\Omega$, $R_3 = R_1R_2/(R_1 + R_2)$

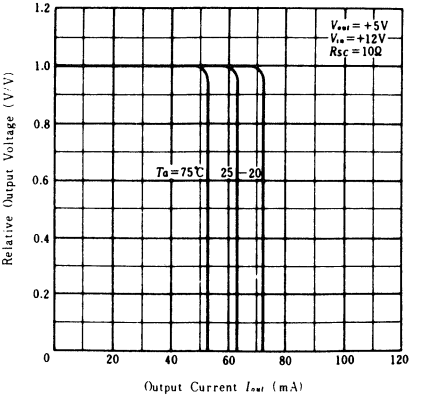
LOAD REGULATION VS. OUTPUT CURRENT-1



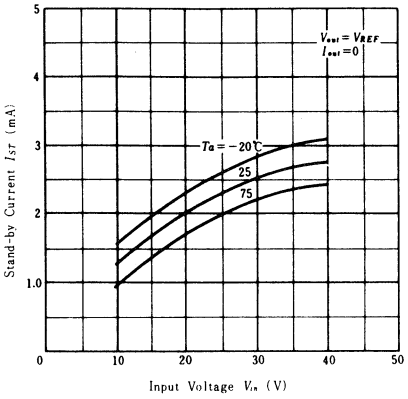
LOAD REGULATION VS. OUTPUT CURRENT-2



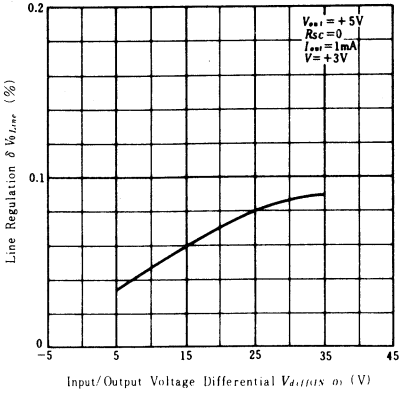
RELATIVE OUTPUT VS. OUTPUT CURRENT VOLTAGE



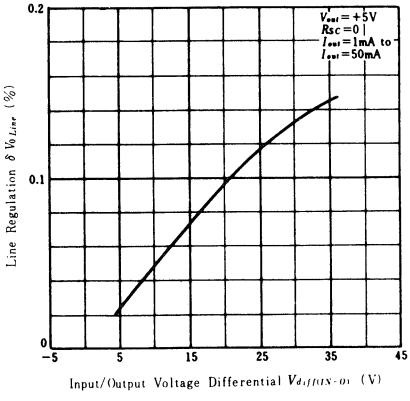
STAND-BY CURRENT VS. INPUT VOLTAGE



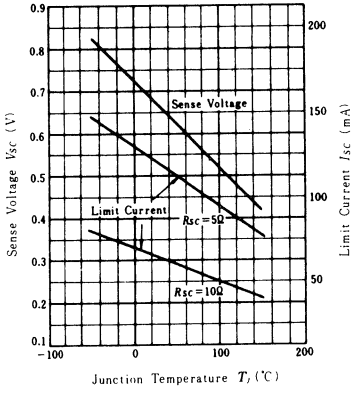
LINE REGULATION VS. INPUT/OUTPUT VOLTAGE DIFFERENTIAL



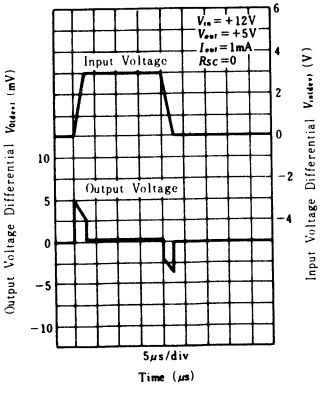
LINE REGULATION VS. INPUT/OUTPUT VOLTAGE DIFFERENTIAL



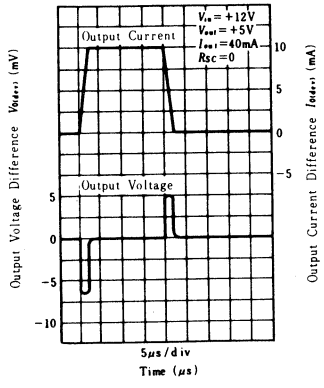
CURRENT LIMITING CHARACTERISTICS



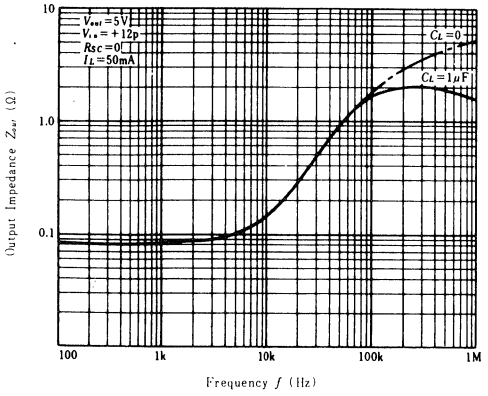
LINE TRANSIENT RESPONSE



LOAD TRANSIENT RESPONSE



OUTPUT IMPEDANCE VS. FREQUENCY



Thus output voltage Vout is:

$$V_{out} = \frac{V_{REF}}{n} \qquad n = \frac{R_2}{R_1 + R_2} \quad \cdots\cdots (2)$$

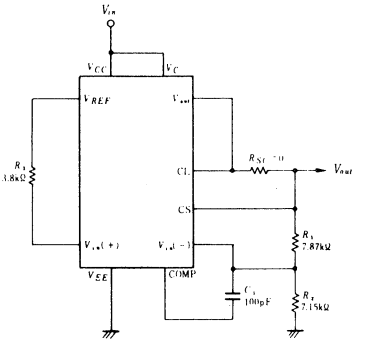


Fig.2 High Voltage (7 to 37V) Regulator

HA17723, APPLICATIONS

HA17723 is high accuracy voltage regulator for general purposes and may be used as voltage sources in various types.

1. Fixed Voltage Source in Series

1.1 Low Voltage, 2 to 7 volts, Regulator

Fig. 1 shows the construction of a basic low voltage regulator. The divider by resistors R_1 and R_2 from V_{REF} is to make the reference voltage which will be provided to non-inverted input of the error amplifier, be less than output voltage. In the fixed voltage source where the output voltage will be fed back to the error amplifier directly as shown in Fig. 1. Output voltage will be divided V_{REF} since the output voltage is equal to the reference voltage.

Thus, the output voltage Vout is;

$$V_{out} = nV_{REF}, \quad n = \frac{R_2}{R_1 + R_2} \quad \cdots\cdots (1)$$

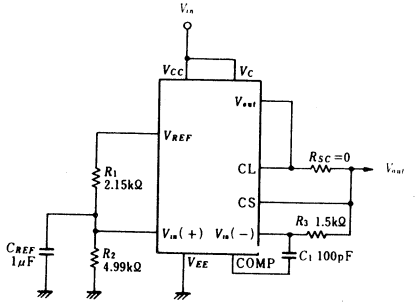


Fig.1 Low Voltage (2 to 7V) Regulator

1.2 High Voltage, 7 to 37V, Regulator

Fig. 2 shows the construction of a regulator when output voltage is higher than the reference voltage, V_{REF}. The V_{REF} shall be added to the non-inverted input of the error amplifier via a resistor, R_3. The feedback voltage is available by dividing the output voltage with resistors R_1 and R_2.

1.3 Negative Voltage Regulator

Fig. 3 shows the construction of a so-called negative voltage regulator which generates negative output voltage with regard to the GND. Assuming that the output voltage, $-V_{out}$ increased in the negative directions. As the voltage across the R_1 is larger than that across the R_3 which provides the reference voltage, output current of the error amplifier increases. In the control circuit, the impedance decreases with increasement of input current, which makes the base current of the external transistor Q approach to the potential at GND. As the results, the output voltage returns to the established value and stable output voltage is available.

The output voltage $-V_{out}$ in this circuit is;

$$-V_{out} = -\left(\frac{R_1 + R_2}{R_3 + R_4} \times \frac{R_3}{R_1}\right) V_{REF}$$

$$= -\frac{(R_1 + R_2)\cdot(R_3 + R_4)}{R_2\cdot(R_3 + R_4) - R_4\cdot(R_1 + R_2)} \times \frac{R_3}{R_3 + R_4} V_{REF} \cdots (2)$$

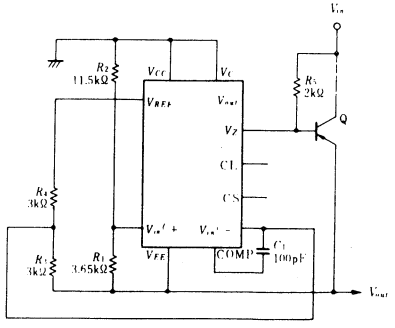


Fig.3 Negative Voltage Regulator

1.4 How to Increase the Output Current

It is necessary for increasement of output current to increase the current capacitance in the control circuit. Fig. 4 and Fig. 5 show examples, where transistors are externally added.

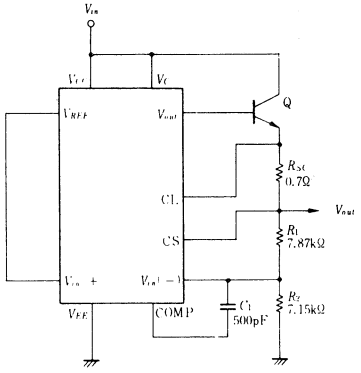


Fig.4 Method to Increase Output Current (1)

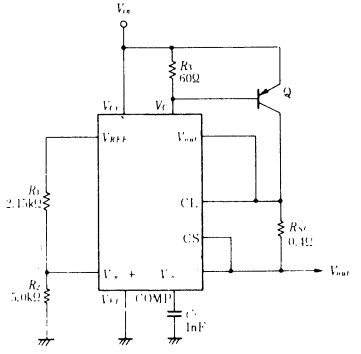


Fig.5 Method to Increase Output Current (2)

2. Fixed Voltage Source in Parallel Control

Fig. 6 shows the circuit of fixed voltage source in parallel control.

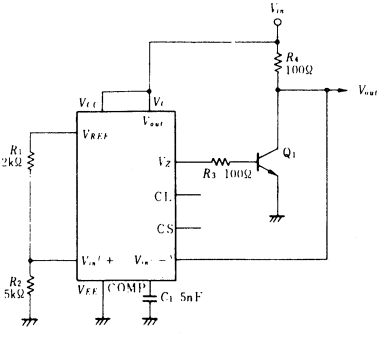


Fig.6 Fixed Voltage Source in Parallel Control

3. Switching Regulator

Fig. 7 shows the circuit of a switching regulator. The error amplifier, control circuit and forward feedback circuit R_4 and R_3 operate in together as a comparator, and make the external transistors Q_1 and Q_2 operate as switching elements to turn ON/OFF. In this circuit, the self-oscillation stabilizes the output voltage and the change in output is absorbed by the changes of conducted period of switches.

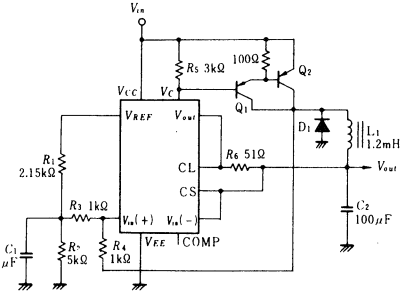


Fig.7 Positive Voltage Switching Regulator

Fig. 8 and Fig. 9 show the circuit of negative voltage switching regulator and its characteristics.

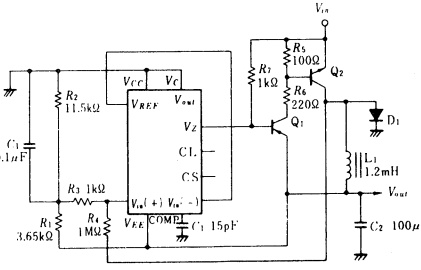
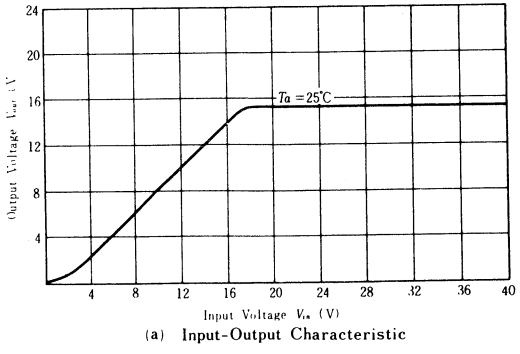
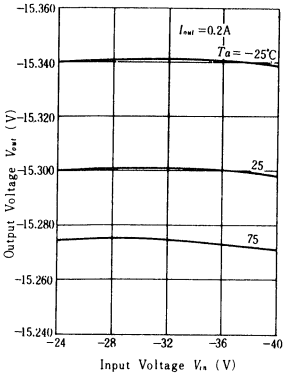


Fig.8 Negative Voltage Switching Regulator

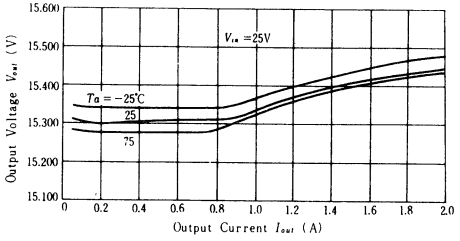


(a) Input-Output Characteristic

Fig.9 Operating Characteristics of Negative Voltage Switching Regulator



(b) Line Regulation



(c) Load Regulation

Fig.9 Operating Characteristics of Negative Voltage Switching Regulator

4. Fixed Voltage Source in Floating Type

Voltage sources in floating type or boost type are typically employed when high voltage output is required. Fig. 10 shows the circuit of a fixed voltage source in the floating type. For considering the stabilization in this circuit, assuming that the output voltage increased. At the input terminal of the error amplifier, non-inverted input will become low compared with inverted input, and the output current of the error amplifier decrease. Then, the current from the terminal V_Z in the control circuit decrease. As the results, the base current of the external resistor Q_1 will decrease and collector current will decrease, resulting to control increasement of the output voltage.

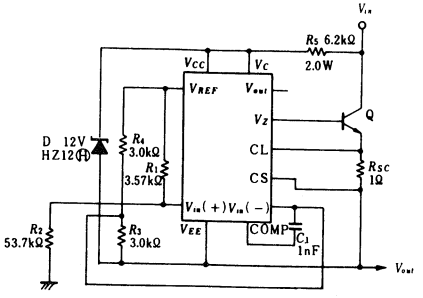


Fig.10 Positive Voltage Floating Regulator

The output voltage V_{out} in the circuit, Fig. 10 is;

$$V_{out} = \left(\frac{R_1+R_2}{R_3+R_4} \times \frac{R_4}{R_1} - 1\right) V_{REF} \quad \cdots\cdots\cdots\cdots (3)$$

Fig. 11 shows the circuit diagram of the negative fixed voltage source in floating type.

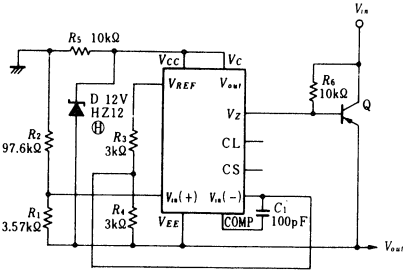


Fig.11 Negative Voltage Floating Regulator

5. Other Applications

Other applications are follows.

5.1 Fixed Voltage Source with Reduction Type Current Limiter

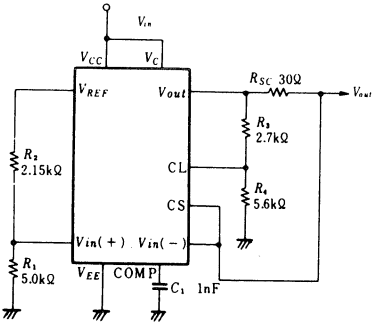
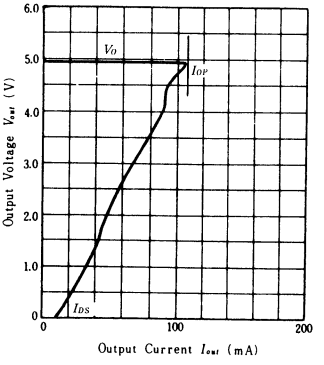


Fig.12 Fixed Voltage Source with Reduction Type Current Limiter



$$I_{OS} = \frac{R_3+R_4}{R_4+R_{SC}} \cdot V_{BE}$$

$$I_{OP} = I_{OS} + \frac{R_3}{R_4+R_{SC}} \cdot V_O$$

Fig.13 Current Control Characteristics of Fixed Voltage Source with Reduction Type Current Limiter

5.2 Fixed Voltage Source Turning ON/OFF External Control

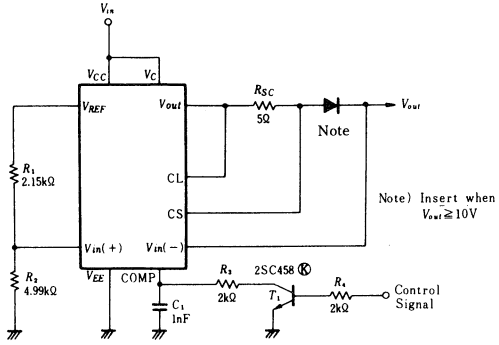


Fig.14 Fixed Voltage Source Turning ON/OFF External Control

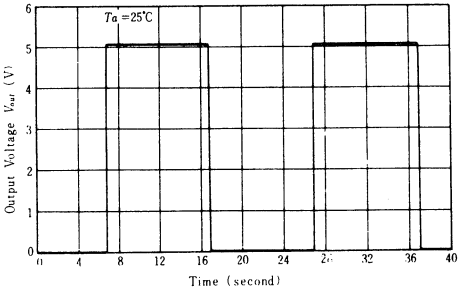


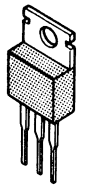
Fig.15 Operating Characteristics of Fixed Voltage Source Turning ON/OFF External Control

HA17800P, HA17800 Series ● 3-terminal Fixed Voltage Regulators

HA17800P and HA17800 series, 3-terminal fixed voltage regulators provides 8 kinds of output voltage; 5, 6, 7, 8, 12, 15, 18 and 24 volts. When a heat sink is used, output current above 1A is available, which enables wide applications are a power source of various equipments.

For all devices in this series, three protection circuit; one to limit current, another to limit temperature at chip junctions and the other to limit internal power dissipation, are built-in and elements are protected against the destructions.

Industrial Use . . . . . HA17800P Series
Commercial Use . . . . . HA17800 Series

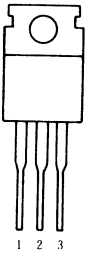


(T-220AB)

■ FEATURES

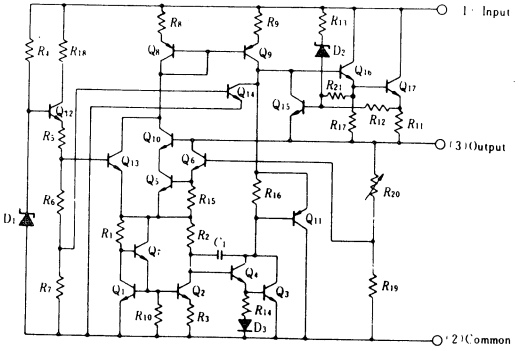
- Output Current 1A is available.
- 8 kinds of output voltages, 5, 6, 7, 8, 12, 15, 18 and 24V will be provided to offer wide applications as various sources.
- Eliminates external compensating circuit.
- T0-220AB package enables easy mounting and radiation design like transistors.
- Built-in Current Limiter prevents elements from destruction when load is short circuited.
- Built-in Chip Junctions Temperature Limiting Circuit protects elements against thermal destruction.
- Built-in Internal Power Dissipation Limiting Circuit protects transistors at output driver.

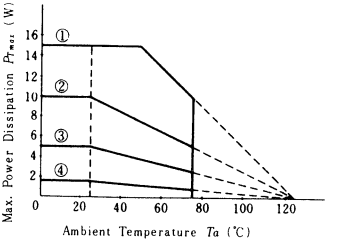
■ PIN ARRANGEMENT



1. Input
2. Common
3. Output

■ CIRCUIT SCHEMATIC





(1) With Infinitely Large Heat Sink
(2) 5°C/W Heat Sink } Including Additional
(3) 15°C/W Heat Sink } Thermal Resistance
(4) Without Heat Sink

$\theta_{j\text{-}c}$ = 3.0°C/W (typ.)
5.0°C/W (max.)
$\theta_{j\text{-}a}$ = 60°C/W (typ.)
65°C/W (max.)

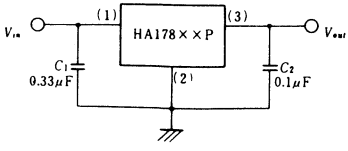
Thermal Resistance

■ ABSOLUTE MAXIMUM RATINGS (Ta=25°C)

Item	Symbol	HA17800P, HA17800 Series	Unit
Input Voltage	V_{in}*	35	V
Input Voltage	V_{in}**	40	V
Power Dissipation	P_T***	15	W
Operating Ambient Temperature	T_{opr}	−20 to +75	°C
Operating Junction Temperature	T_j	−20 to +125	°C
Storage Temperature	T_{stg}	−55 to +125	°C

Note) * HA17805P to HA17818P and HA17805 to HA17818
** HA17824P and HA17824
*** Follow the derating curve

■ TYPICAL CONNECTING CIRCUIT



HITACHI

■ HA17805P, HA17805 ELECTRICAL CHARACTERISTICS

(V_{in} = 10V, I_{out} = 500mA, 0°C ≦ T_j ≦ 125°C, C_{in} = 0.33μF, C_{out} = 0.1μF; unless otherwise specified.)

Item	Symbol	Test Conditions		min	typ	max	Unit
Output Voltage	V_{out}	T_j = 25°C		4.8	5.0	5.2	V
		7V ≦ V_{in} ≦ 20V, 5mA ≦ I_{out} ≦ 1.0A, P_T ≦ 15W		4.75	—	5.25	V
Line Regulation	$\delta V_{o\ line}$	T_j = 25°C	7V ≦ V_{in} ≦ 25V	—	3	100	mV
			8V ≦ V_{in} ≦ 12V	—	1	50	mV
Load Regulation	$\delta V_{o\ load}$	T_j = 25°C	5mA ≦ I_{out} ≦ 1.5A	—	15	100	mV
			250mA ≦ I_{out} ≦ 750mA	—	5	50	mV
Quiescent Current	I_Q	T_j = 25°C, I_{out} = 0		—	4.2	8.0	mA
Quiescent Current Change	δI_Q	7V ≦ V_{in} ≦ 25V		—	—	1.3	mA
		5mA ≦ I_{out} ≦ 1.0A		—	—	0.5	mA
Output Noise Voltage	V_n	Ta = 25°C, 10Hz ≦ f ≦ 100kHz		—	40	—	μV
Ripple Rejection Ratio	R_{REJ}	f = 120Hz		62	78	—	dB
Voltage Drop	V_{DROP}	I_{out} = 1.0A, T_j = 25°C		—	2.0	—	V
Output Resistance	R_{out}	f = 1kHz		—	17	—	mΩ
Output Short Circuit Current	I_{OS}	T_j = 25°C		—	750	—	mA
Peak Output Current	$I_{o\ peak}$	T_j = 25°C		—	2.2	—	A
Temperature Coefficient of Output Voltage	$\delta V_{out}/\delta T_j$	I_{out} = 5mA, 0°C ≦ T_j ≦ 125°C		—	−1.1	—	mV/°C

■ HA17806P, HA17806 ELECTRICAL CHARACTERISTICS

(V_{in} = 11V, I_{out} = 500mA, 0°C ≦ T_j ≦ 125°C, C_{in} = 0.33μF, C_{out} = 0.1μF, unless otherwise specified.)

Item	Symbol	Test Conditions		min	typ	max	Unit
Output Voltage	V_{out}	T_j = 25°C		5.75	6.0	6.25	V
		8V ≦ V_{in} ≦ 21V, 5mA ≦ I_{out} ≦ 1.0A, P_T ≦ 15W		5.7	—	6.3	V
Line Regulation	$\delta V_{o\ line}$	T_j = 25°C	8V ≦ V_{in} ≦ 25V	—	5	120	mV
			9V ≦ V_{in} ≦ 13V	—	1.5	60	mV
Load Regulation	$\delta V_{o\ load}$	T_j = 25°C	5mA ≦ I_{out} ≦ 1.5A	—	14	120	mV
			250mA ≦ I_{out} ≦ 750mA	—	4	60	mV
Quiescent Current	I_Q	T_j = 25°C, I_{out} = 0		—	4.3	8.0	mA
Quiescent Current Change	δI_Q	8V ≦ V_{in} ≦ 25V		—	—	1.3	mA
		5mA ≦ I_{out} ≦ 1.0A		—	—	0.5	mA
Output Noise Voltage	V_n	Ta = 25°C, 10Hz ≦ f ≦ 100kHz		—	45	—	μV
Ripple Rejection Ratio	R_{REJ}	f = 120Hz		59	75	—	dB
Voltage Drop	V_{DROP}	I_{out} = 1.0A, T_j = 25°C		—	2.0	—	V
Output Resistance	R_{out}	f = 1kHz		—	19	—	mΩ
Output Short Circuit Current	I_{OS}	T_j = 25°C		—	550	—	mA
Peak Output Current	$I_{o\ peak}$	T_j = 25°C		—	2.2	—	A
Temperature Coefficient of Output Voltage	$\delta V_{out}/\delta T_j$	I_{out} = 5mA, 0°C ≦ T_j ≦ 125°C		—	−0.8	—	mV/°C

HA17807P, HA17807 ELECTRICAL CHARACTERISTICS

(V_{in}=12.5V, I_{out}=500mA, 0°C ≦ T_j ≦ 125°C, C_{in}=0.33μF, C_{out}=0.1μF, unless otherwise specified.)

Item	Symbol	Test Conditions		max	typ	max	Unit
Output Voltage	V_{out}	T_j=25°C		6.72	7.0	7.28	V
		9V ≦ V_{in} ≦ 22V, 5mA ≦ I_{out} ≦ 1.0A, P_T ≦ 15W		6.65	—	7.35	V
Line Regulation	$\delta V_{o\ line}$	T_j=25°C	9V ≦ V_{in} ≦ 25V	—	5.5	140	mV
			10V ≦ V_{in} ≦ 15V	—	1.7	70	mV
Load Regulation	$\delta V_{o\ load}$	T_j=25°C	5mA ≦ I_{out} ≦ 1.5A	—	13	140	mV
			250mA ≦ I_{out} ≦ 750mA	—	4	70	mV
Quiescent Current	I_Q	T_j=25°C, I_{out}=0		—	4.3	8.0	mA
Quiescent Current Change	δI_Q	9V ≦ V_{in} ≦ 25V		—	—	1.3	mA
		5mA ≦ I_{out} ≦ 1.0A		—	—	0.5	mA
Output Noise Voltage	V_n	Ta=25°C, 10Hz ≦ f ≦ 100kHz		—	48.5	—	μV
Ripple Rejection Ratio	R_{REJ}	f=120Hz		57	73	—	dB
Voltage Drop	V_{DROP}	I_{out}=1.0A, T_j=25°C		—	2.0	—	V
Output Resistance	R_{out}	f=1kHz		—	17	—	mΩ
Output Short Circuit Current	I_{OS}	T_j=25°C		—	500	—	mA
Peak Output Current	$I_{o\ peak}$	T_j=25°C		—	2.2	—	A
Temperature Coefficient of Output Voltage	$\delta V_{out}/\delta T_j$	I_{out}=5mA, 0°C ≦ T_j ≦ 125°C		—	−0.8	—	mV/°C

HA17808P, HA17808 ELECTRICAL CHARACTERISTICS

(V_{in}=14V, I_{out}=500mA, 0°C ≦ T_j ≦ 125°C, C_{in}=0.33μF, C_{out}=0.1μF, unless otherwise specified.)

Item	Symbol	Test Conditions		min	typ	max	Unit
Output Voltage	V_{out}	T_j=25°C		7.7	8.0	8.3	V
		10.5V ≦ V_{in} ≦ 23V, 5mA ≦ I_{out} ≦ 1.0A, P_T ≦ 15W		7.6	—	8.4	V
Line Regulation	$\delta V_{o\ line}$	T_j=25°C	10.5V V_{in} ≦ 25V	—	6.0	160	mV
			11V ≦ V_{in} ≦ 17V	—	2.0	80	mV
Load Regulation	$\delta V_{o\ load}$	T_j=25°C	5mA ≦ I_{out} ≦ 1.5A	—	12	160	mV
			250mA ≦ I_{out} ≦ 750mA	—	4.0	80	mV
Quiescent Current	I_Q	T_j=25°C, I_{out}=0		—	4.3	8.0	mA
Quiescent Current Change	δI_Q	10.5V ≦ V_{in} ≦ 25V		—	—	1.0	mA
		5mA ≦ I_{out} < 1.0A		—	—	0.5	mA
Output Noise Voltage	V_n	Ta=25°C, 10Hz ≦ f ≦ 100kHz		—	52	—	μV
Ripple Rejection Ratio	R_{REJ}	f=120Hz		56	72	—	dB
Voltage Drop	V_{DROP}	I_{out}=1.0A, T_j=25°C		—	2.0	—	V
Output Resistance	R_{out}	f=1kHz		—	16	—	mΩ
Output Short Circuit Current	I_{OS}	T_j=25°C		—	450	—	mA
Peak Output Current	$I_{o\ peak}$	T_j=25°C		—	2.2	—	A
Temperature Coefficient of Output Voltage	$\delta V_{out}/\delta T_j$	I_{out}=5mA, 0°C ≦ T_j ≦ 125°C		—	−0.8	—	mV/°C

■HA17812P, HA17812 ELECTRICAL CHARACTERISTICS

(V_{in}=19V, I_{out}=500mA, 0°C≦T_j≦125°C, C_{in}=0.33μF, C_{out}=0.1μF; unless otherwise specified.)

Item	Symbol	Test Conditions		min	typ	max	Unit
Output Voltage	V_{out}	T_j=25°C		11.5	12.0	12.5	V
		14.5V≦V_{in}≦27V, 5mA≦I_{out}≦1.0A, P_T≦15W		11.5	—	12.6	V
Line Regulation	$\delta V_{o\ line}$	T_j=25°C	14.5V≦V_{in}≦30V	—	10	240	mV
			16V≦V_{in}≦22V	—	3.0	120	mV
Load Regulation	$\delta V_{o\ load}$	T_j=25°C	5mA≦I_{out}≦1.5A	—	12	240	mV
			250mA≦I_{out}≦750mA	—	4.0	120	mV
Quiescent Current	I_Q	T_j=25°C, I_{out}=0		—	4.3	8.0	mA
Quiescent Current Change	δI_Q	14.5V≦V_{in}≦30V		—	—	1.0	mA
		5mA≦I_{out}≦1.0A		—	—	0.5	mA
Output Noise Voltage	V_n	Ta=25°C, 10Hz≦f≦100kHz		—	75	—	μV
Ripple Rejection Ratio	R_{REJ}	f=120Hz		55	71	—	dB
Voltage Drop	V_{DROP}	I_{out}=1.0A, T_j=25°C		—	2.0	—	V
Output Resistance	R_{out}	f=1kHz		—	18	—	mΩ
Output Short Circuit Current	I_{OS}	T_j=25°C		—	350	—	mA
Peak Output Current	$I_{o\ peak}$	T_j=25°C		—	2.2	—	A
Temperature Coefficient of Output Voltage	$\delta V_{out}/\delta T_j$	I_{out}=5mA, 0°C≦T_j≦125°C		—	−1.0	—	mV/°C

■HA17815P, HA17815 ELECTRICAL CHARACTERISTICS

(V_{in}=23V, I_{out}=500mA, 0°C≦T_j≦125°C, C_{in}=0.33μF, C_{out}=0.1μF; unless otherwise specified.)

Item	Symbol	Test Conditions		min	typ	max	Unit
Output Voltage	V_{out}	T_j=25°C		14.4	15.0	15.6	V
		17.5V≦V_{in}≦30V, 5mA≦I_{out}≦1.0A, P_T≦15W		14.25	—	15.75	V
Line Regulation	$\delta V_{o\ line}$	T_j=25°C	17.5V≦V_{in}≦30V	—	11	300	mV
			20V≦V_{in}≦26V	—	3	150	mV
Load Regulation	$\delta V_{o\ load}$	T_j=25°C	5mA≦I_{out}≦1.5A	—	12	300	mV
			250mA≦I_{out}≦750mA	—	4	150	mV
Quiescent Current	I_Q	T_j=25°C, I_{out}=0		—	4.4	8.0	mA
Quiescent Current Change	δI_Q	17.5V≦V_{in}≦30V		—	—	1.0	mA
		5mA≦I_{out}≦1.0A		—	—	0.5	mA
Output Noise Voltage	V_n	Ta=25°C, 10Hz≦f≦100kHz		—	90	—	μV
Ripple Rejection Ratio	R_{REJ}	f=120Hz		54	70	—	dB
Voltage Drop	V_{DROP}	I_{out}=1.0A, T_j=25°C		—	2.0	—	V
Output Resistance	R_{out}	f=1kHz		—	19	—	mΩ
Output Short Circuit Current	I_{OS}	T_j=25°C		—	230	—	mA
Peak Output Current	$I_{o\ peak}$	T_j=25°C		—	2.1	—	A
Temperature Coefficient of Output Voltage	$\delta V_{out}/\delta T_j$	I_{out}=5mA, 0°C≦T_j≦125°C		—	−1.0	—	mV/°C

HA17818P, HA17818 ELECTRICAL CHARACTERISTICS

(V_{in}=27V, I_{out}=500mA, 0℃ ≦ T_j ≦ 125℃, C_{in}=0.33μF, C_{out}=0.1μF; unless otherwise specified.)

Item	Symbol	Test Conditions		min	typ	max	Unit
Output Voltage	V_{out}	T_j=25℃		17.3	18.0	18.7	V
		21V ≦ V_{in} ≦ 33V, 5mA ≦ I_{out} ≦ 1.0A, P_T ≦ 15W		17.1	—	18.9	V
Line Regulation	$\delta V_{o\ line}$	T_j=25℃	21V ≦ V_{in} ≦ 33V	—	15	360	mV
			24V ≦ V_{in} ≦ 30V	—	5.0	180	mV
Load Regulation	$\delta V_{o\ load}$	T_j=25℃	5mA ≦ I_{out} ≦ 1.5A	—	12	360	mV
			250mA ≦ I_{out} ≦ 750mA	—	4.0	180	mV
Quiescent Current	I_Q	T_j=25℃, I_{out}=0		—	4.5	8.0	mA
Quiescent Current Change	δI_Q	21V ≦ V_{in} ≦ 33V		—	—	1.0	mA
		5mA ≦ I_{out} ≦ 1.0A		—	—	0.5	mA
Output Noise Voltage	V_n	Ta=25℃, 10Hz ≦ f ≦ 100kHz		—	110	—	μV
Ripple Rejection Ratio	R_{REJ}	f=120Hz		53	69	—	dB
Voltage Drop	V_{DROP}	I_{out}=1.0A, T_j=25℃		—	2.0	—	V
Output Resistance	R_{out}	f=1kHz		—	22	—	mΩ
Output Short Circuit Current	I_{OS}	T_j=25℃		—	200	—	mA
Peak Output Current	$I_{o\ peak}$	T_j=25℃		—	2.1	—	A
Tempecrature Coefficient of Output Voltage	$\delta V_{out}/\delta T_j$	I_{out}=5mA, 0℃ ≦ T_j ≦ 125℃		—	−1.0	—	mV/℃

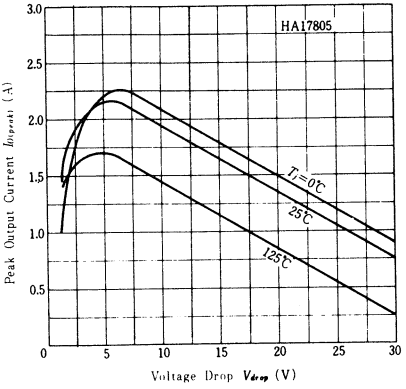
HA17824P, HA17824 ELECTRICAL CHARACTERISTICS

(V_{in}=33V, I_{out}=500mA, 0℃ ≦ T_j ≦ 125℃, C_{in}=0.33μF, C_{out}=0.1μF; unless otherwise specified.)

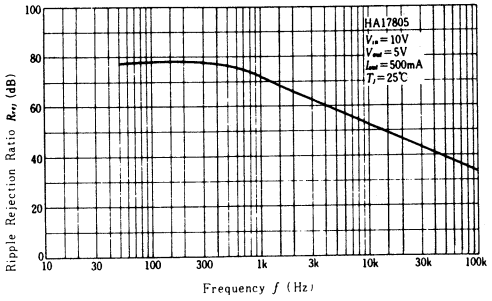
Item	Symbol	Test Conditions		min	typ	max	Unit
Output Voltage	V_{out}	T_j=25℃		23.0	24.0	25.0	V
		27V ≦ V_{in} ≦ 38V, 5mA ≦ I_{out} ≦ 1.0A, P_T ≦ 15W		22.8	—	25.2	V
Line Regulation	$\delta V_{o\ line}$	T_j=25℃	27V ≦ V_{in} ≦ 38V	—	18	480	mV
			30V ≦ V_{in} ≦ 36V	—	6	240	mV
Load Regulation	$\delta V_{o\ load}$	T_j=25℃	5mA ≦ I_{out} ≦ 1.5A	—	12	480	mV
			250mA ≦ I_{out} ≦ 750mA	—	4	240	mV
Quiescent Current	I_Q	T_j=25℃, I_{out}=0		—	4.6	8.0	mA
Quiescent Current Change	δI_Q	27V ≦ V_{in} ≦ 38V		—	—	1.0	mA
		5mA ≦ I_{out} ≦ 1.0A		—	—	0.5	mA
Output Noise Voltage	V_n	Ta=25℃, 10Hz ≦ f ≦ 100kHz		—	170	—	μV
Ripple Rejection Ratio	R_{REJ}	f=120Hz		50	66	—	dB
Voltage Drop	V_{DROP}	I_{out}=1.0A, T_j=25℃		—	2.0	—	V
Output Resistance	R_{out}	f=1kHz		—	28	—	mΩ
Output Short Circuit Current	I_{OS}	T_j=25℃		—	150	—	mA
Peak Output Current	$I_{o\ peak}$	T_j=25℃		—	2.1	—	A
Temperature Coefficient of Output Voltage	$\delta V_{out}/\delta T_j$	I_{out}=5mA, 0℃ ≦ T_j ≦ 125℃		—	−1.5	—	mV/℃

■ CHARACTERISTICS CURVE

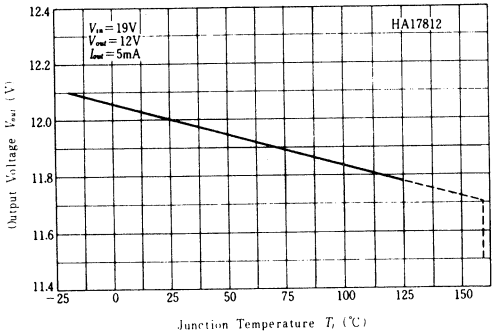
PEAK OUTPUT VS. VOLTAGE DROP CURRENT



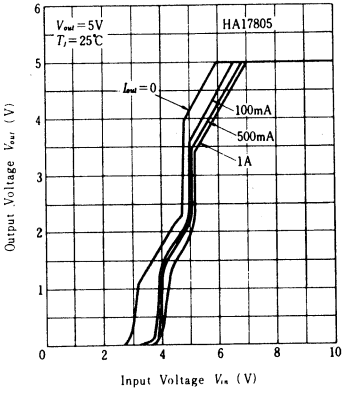
RIPPLE REJECTION VS. FREQUENCY RATIO



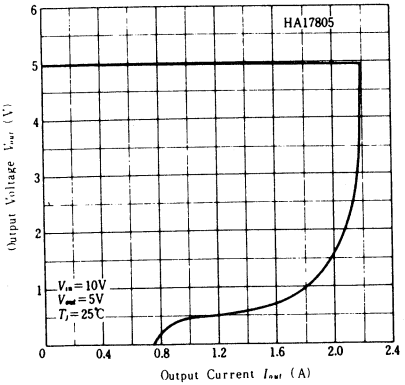
OUTPUT VOLTAGE VS. JUNCTION TEMPERATURE



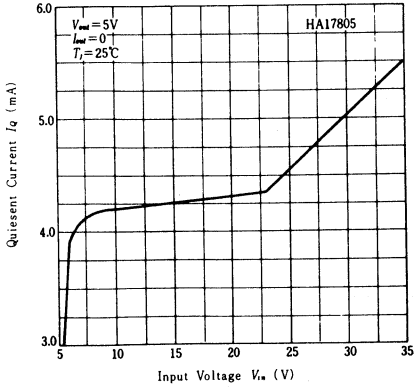
OUTPUT VOLTAGE VS. INPUT VOLTAGE



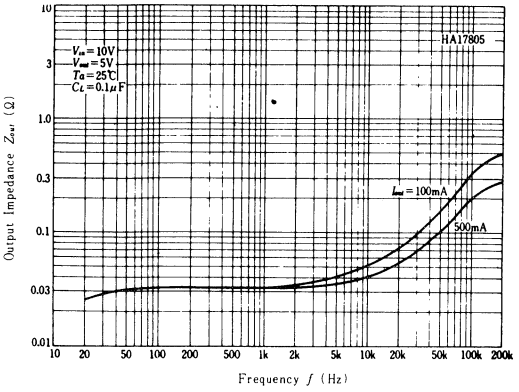
OUTPUT VOLTAGE VS. OUTPUT CURRENT



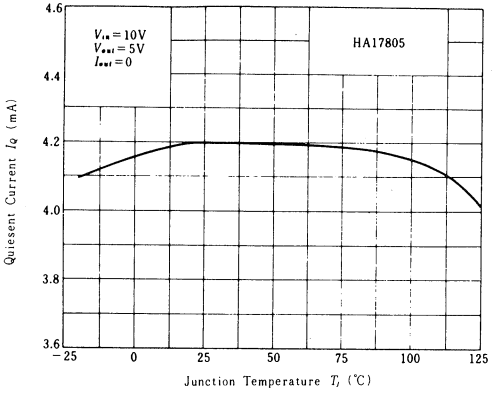
QUIESCENT CURRENT VS. INPUT VOLTAGE



OUTPUT IMPEDANCE VS. FREQUENCY



QUIESCENT CURRENT VS. JUNCTION TEMPERATURE



APPLICATION NOTE

In HA17800 Series, external compensating circuits are eliminated and easy mounting and radiation design like transistors are enabled by employing the TO-220AB package. Output current 1A is available when using a heat sink. To protect devices from destruction, three protection circuit; current limiter, one against load short circuit and one to control the operating junction temperature, are built-in. HA17800 series are usable fixed voltage sources and the followings shall explain some examples of circuit constructions and applications for further use.

1. Circuit Constructions of HA17800 Series

Fig. 1 shows the internal equivalent circuit and Fig. 2 shows its block diagram of HA17800 Series.

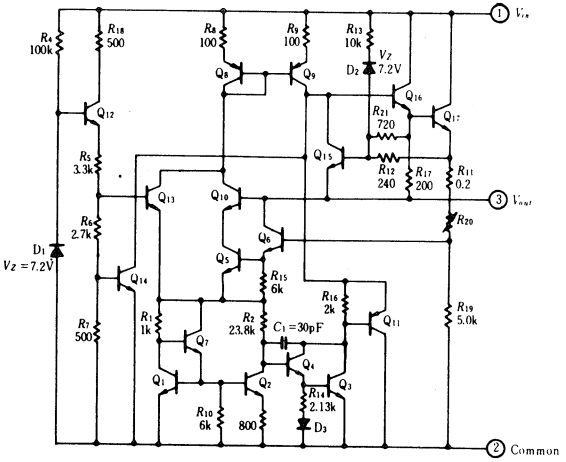


Fig.2 Block Diagram of HA17800 Series

Fig.1 Internal Equivalent Circuit of HA17800 Series

(1) Reference Voltage Circuit

For examplaining the part generating the reference voltage, the equivalent circuit shall be shown in Fig. 3. As this figure shows clearly, the difference from the conventional method using zener diodes is that the reference voltage is generated by only the base-emitter forward characteristics of transistors. The reference voltage V_{REF} is;

$$V_{REF} = V_{BE4} + V_{BE5} + V_{BE6} + V_{BE3} + R_2 I_{C2} \quad \cdots\cdots (1)$$

$$R_1 I_{C1} + V_{BE1} = R_2 I_{C2} + V_{BE3} \quad \cdots\cdots (2)$$

$$V_{BE1} = V_{BE2} + R_3 I_{E2} \quad \cdots\cdots (3)$$

$$V_{BE} = \frac{kT}{q} ln \frac{I_C}{I_O} \quad \cdots\cdots (4)$$

where, assuming that $V_{BE1} \fallingdotseq V_{BE3}$

$$I_{E2} \fallingdotseq \frac{kT}{q} \frac{1}{R_3} ln \frac{R_2}{R_1} \quad \cdots\cdots (5)$$

$$V_{REF} = V_{BE3} + V_{BE4} + V_{BE5} + V_{BE6} + \frac{kT}{q} \frac{R_2}{R_3} ln \frac{R_2}{R_1} \quad \cdots\cdots (6)$$

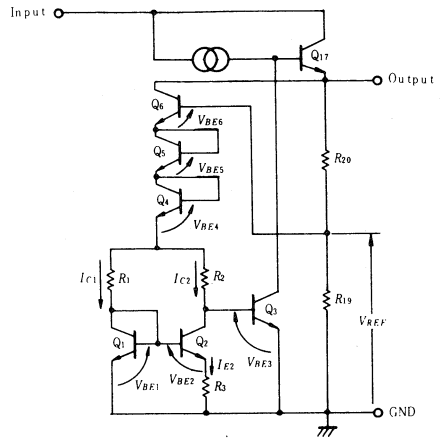


Fig.3 Circuit Generating Reference Voltage

In equation (6), the first four terms in the right to equal sign are V_{BE} and have negative temperature coefficient. On the other hand, the last term has positive temperature coefficient. Then, give value to R_1, R_2 and R_3 so that $V_{REF} \fallingdotseq 5V$ $\delta V_{REF}/\delta T = 0$. This reference voltage source which utilize the base-emitter forward voltage of transistors has less noise than the conventional ones using zener diodes. The output voltage is as shown in Fig. 3;

$$V_{out} = V_{REF}\left(1+\frac{R_{20}}{R_{19}}\right) \quad \cdots\cdots(7)$$

(2) Protection Circuit

In the HA17800 Series three kinds of protection circuit are provided. One is current limiter constructed by R_{11}, R_{12}, R_{21} and Q_{15}. Another is one to control output when load is short circuited or the power dissipation of output transistor Q_{17} exceeds a limit value, constructed by R_{13} and D_2. The other is one constructed by Q_{14} which prevents temperature rise on the whole chip.

(3) Other Circuits

The Darlington connection, Q_4–Q_3 in the Fig. 1 operates as an error amplifier as well as a reference voltage generator. As the collector load of Q_3 is a load with high impedance constructing the fixed current source from Q_9, MOS capacitance shall be applied to compensate the frequency characteristics of the error amplifier. It is aiming at stable operation when load conditions changes. Q_{13} operates as the so-called ignition circuit which flows current to Q_8 when a regulator turns ON and is turned OFF by the rised emitter potential when regulator provides output.

2. CAUTIONS ON USE

Package used in HA17800 Series are TO-220AB, which is used for mid-power transistors and, therefore, the mechanical treatment is as same as in the case of transistors. The other important points are radiation design and the way to by-pass.

2.1 Radiation Design

When the power dissipation of HA17800 series exceeds to 1.67W, a radiator or a heat sink must be attached so that the junction temperature is below the specified value. If you use the radiators on the market, you must select one with required thermal resistance and pay attention to mounting. If you design by yourself, you can utilize the data in Figs. 4 thru 6.

(An Example of Designing a Heat Sink)

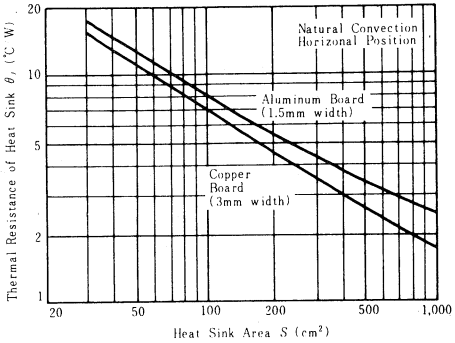


Fig.4 Areas vs Thermal Resistance of Heat Sink

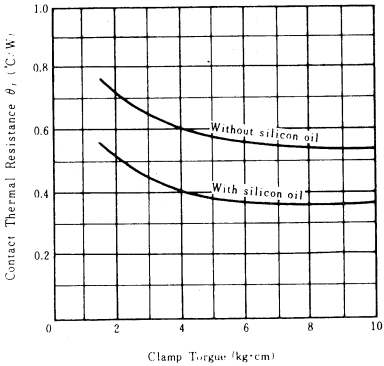


Fig.5 Clamp Torque vs Contact Thermal Resistance

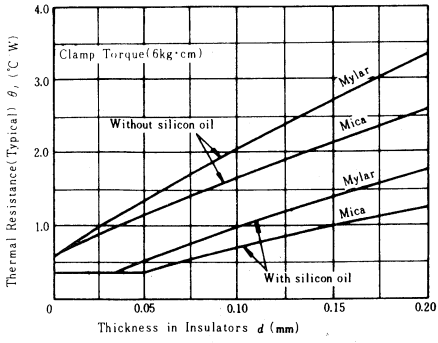


Fig.6 Thickness in Insulators vs Thermal Resistance (Typical)

Assuming to design a radiator which is required when HA17800 Series dissipates 10W in the condition of the maximum ambient temperature is 50°C.

(1) Ratings of HA17800 Series Junction Temperature T_j = 125°C
Thermal Resistance $\theta_{j\text{-}C}$ = 5°C/W
Junction – Case

(2) When a radiator is used, the relationship between the junction temperature rise and power dissipation will be;

$$\therefore \theta_f = \frac{T_j - Ta}{P_T} - \theta_{j-c} - \theta_S$$

Thus the thermal resistance of the required radiator is;

$$\theta_f = \frac{125-50}{10} - 5 - 0.4 = 2.1°C/W$$

(3) As Fig. 4 indicates, the required area of the heat sink will be 760cm² when copperplate of thickness; 3 mm. Then, the heat sink is placed horizontally. If this area is too large, it can be smaller by air-cooling by wind from a fan.

2.2 Way to By-Pass

HA17800 Series may be used as regulators in a simple form, but stable operation requires connection of capacitors for by-passing at input and output as shown in Fig. 7. The capacitor at input, C_{in} must be at least 0.22μF to improve the stability in operations and the large capacitance capacitor for smoothing, C may be used at input. The capacitor at output, C_{out} is provided aiming at preventing oscillation and improving transfer characteristics. The output impedance of the regulator increases with increasement of frequency. This phenomenon is caused that the gain with devices decreases with the increasement of frequency. So, adding a capacitor of about 50μF to output as shown in Fig. 8 improves it. When supplying voltage to load which switches in high speed as TTL load, ceramic capacitor or film capacitor with good frequency characteristics shall be connected at output.

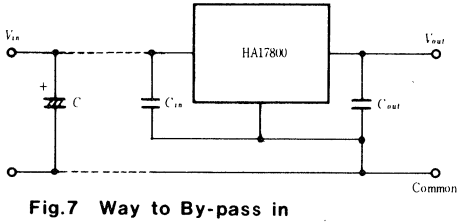


Fig.7 Way to By-pass in HA17800 Series

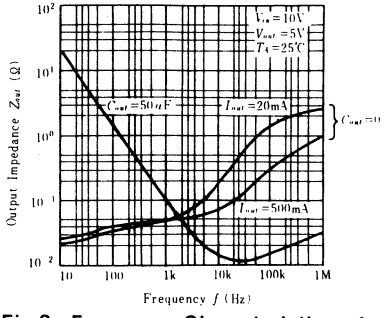


Fig.8 Frequency Characteristics of Output Impedance

3. APPLICATIONS

3.1 Fixed Output Regulators

Fig. 9 shows the most basic form of the 3-terminal fixed output regulator. Fig. 10 shows the operational characteristics of this type regulators.

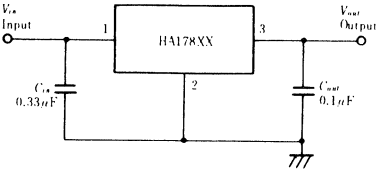
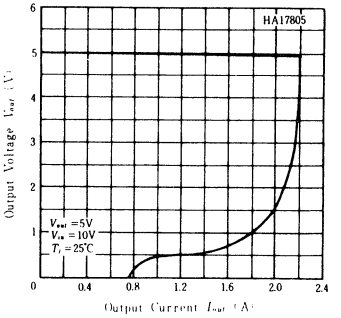
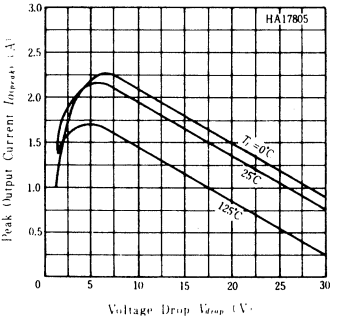


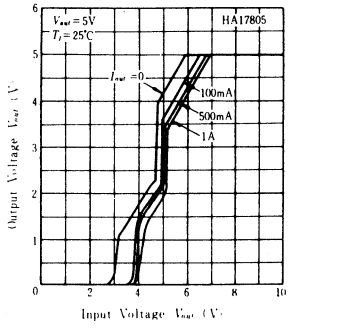
Fig.9 Fixed Output Regulator



(a) Output Voltage vs Output Current



(b) Peak Output Current vs Voltage Drop



(c) Output Voltage vs Input Voltage

Fig.10 Operational Characteristics of Fixed Output Regulator

3.2 A Regulator with Increased Output Voltage

Fig. 11 shows the circuit diagram to increase output voltage utilizing fixed output voltage. The output voltage V_{out} is;

$$V_{out} = \left(1 + \frac{R_2}{R_1}\right) V_{XX} + I_Q R_2$$

where, V_{XX}: Output voltage in HA17800 Series
I_Q: Quiescent Current in HA17800 Series

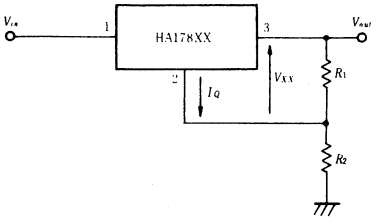


Fig.11 Regulator with Increased Output Voltage

If the resistance ratio, R_2/R_1 are equal, adopting smaller R_1 and R_2 value enables to ignore the voltage drop because of quiescent current, I_QR_2.
However, as smaller resistance causes the larger power dissipation at the resistor, attention must be paid to the power capacitance of the resistor.

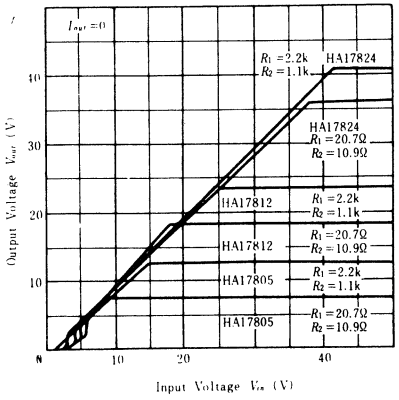


Fig.12 Operational Characteristics of the Regulator with Increased Voltage

3.3 Fixed Current Regulator

Fig. 13 shows the circuit of a fixed current regulator to provide a fixed current. This circuit utilizes the fixed output voltage of HA17800 series to generate a fixed current and is easily designed.

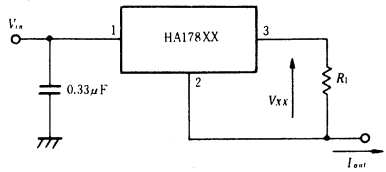


Fig.13 Fixed Current Regulator

The fixed current output, I_{out} is;

$$I_{out} = \frac{V_{XX}}{R_1} + I_Q$$

where, V_{XX}: Output Voltage of HA17800 Series
I_Q: Quiescent Current of HA17800 Series

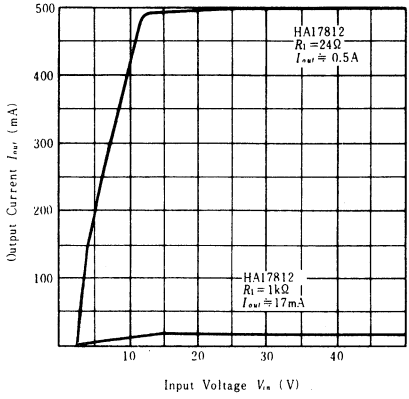


Fig.14 Operational Characteristics of Fixed Current Regulator

If the resistance of R_1 is small and V_{XX}/R_1 is far larger than I_Q, I_{out} is nearly equal to V_{XX}/R_1. The maximum value of the fixed current output, I_{out} is maximum output current of HA17800 Series, 1.5A. Then, the power of the resistor R_1 and the maximum power dissipation of HA17800 Series must be considered.

3.4 Variable Output Voltage (7 to 30V, 0.5 to 10V) Regulator

Fig. 15 shows the circuit of a regulator whose output voltage is variable from 7 to 30 volts and Fig. 17 shows that of a regulator whose output voltage is variable from 0.5 to 10V. In each case, output voltage is controlled by an operational amplifier and the output voltage is;

$$V_{out} = \left(1 + \frac{R_2}{R_1}\right) V_{XX} \quad \text{(In case of Fig. 15)}$$

$$V_{out} = \left(\frac{R_1 + R_2}{R_3 + R_4}\right) \times \frac{R_3}{R_1} V_{XX} \quad \text{(In case of Fig. 17)}$$

The relationships of the adjusting point potential of the variable resistor, R, V_R and output voltage, V_{out} are shown in Fig. 16 and Fig. 18. Operational amplifiers should be selected considering supply voltage, common mode input voltage range, output voltage range and so on. When oscillation happened, inserting a capacitor between V_{in} and Common Terminal is an effective measure.

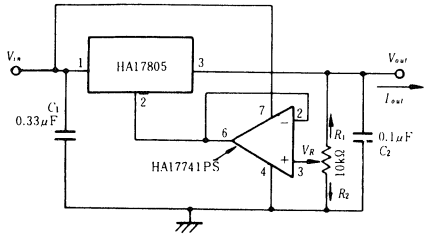


Fig.15 Variable Output Voltage (7 to 30V) Regulator

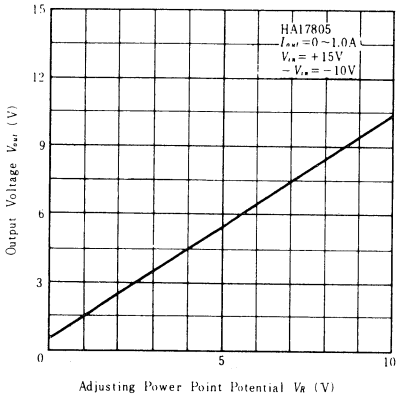


Fig.16 The Variable Output Voltage (7 to 30V) Regulator—Adjusting Power Point Potential, V_R Characteristics

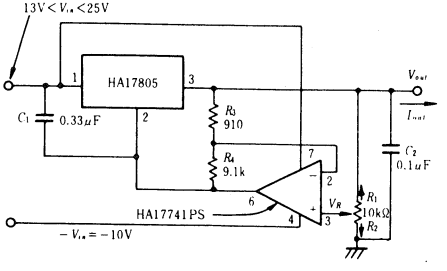


Fig.17 Variable Output Voltage (0.5 to 10V) Regulator

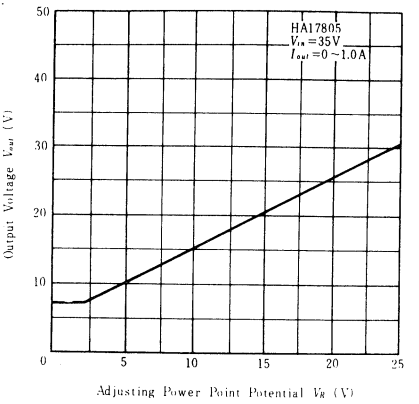


Fig.18 The Variable Output Voltage (0.5 to 10V) Regulator—Adjusting Power Point Potential, V_R Characteristics

3.5 Regulator with Increased Output Current

In HA17800 Series, output current above 1A is available and larger current is available by externally adding a transistor as shown in Fig. 19. Then, the relationship of the current amplification factor, h_{FE} of the transistor Q_1 and current in each parts must be

$$h_{FE}(Q_1) \geqq \frac{I_{out}}{I_{REG}}$$

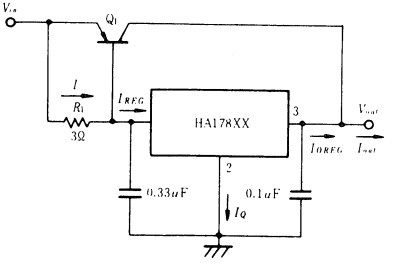


Fig.19 Regulator with Increased Output Current (1)

$$I_{out} = (1+h_{FE})I_{OREG} + h_{FE}I_Q - h_{FE}I$$

$$I_{OREG} = \frac{h_{FE}}{1+h_{FE}}\left(\frac{I_{out}}{h_{FE}} + I - I_Q\right)$$

The output current decreases from I_{out} to I_{OREG} in appearance and the load regulation will be improved.

A circuit where a current limiter is added to the basic regulator with increased output current in Fig. 19 shall be shown in Fig. 20. The limit value of the output current I_{out} limit is determined as;

$$I_{out}\ \text{limit} = \frac{V_{BE(Q2)}}{R_{SC}}$$

Fig. 21 shows the operational characteristics of the circuit in Fig. 20. On determining R_{CS}, line impedance and contact resistance should be considered.

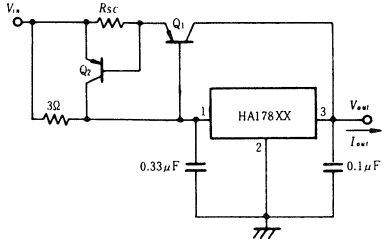


Fig.20 Regulator with Increased Output Current (2)

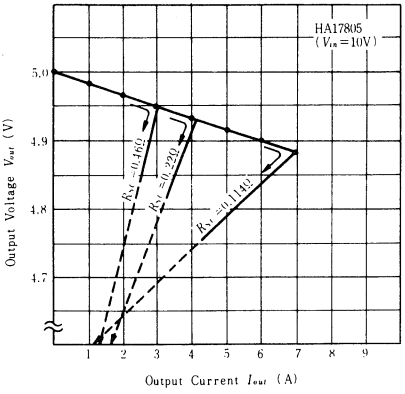


Fig.21 Operational Characteristics of the Regulator with Increased Output Current (2)

3.6 Positive and Negative Voltage Regulator

Fig. 22 shows the circuit of a regulator which provides both positive and negative output, constructed by 2 devices of HA17800 Series. The portion providing positive output is basically the same as in 3.1 the fixed output regulator.

In the portion providing negative output, the input of HA17800 series is floating state, output terminal V_{out} is grounded and the negative voltage is taken out of the common terminal.

Fig. 22 shows the circuit to get larger power than the commercial source. Its ripple voltage at output will be determined by the characteristics of the smoothing circuit and ripple rejection ratio in HA17800 series –78dB typ: in case of 05P, 05.

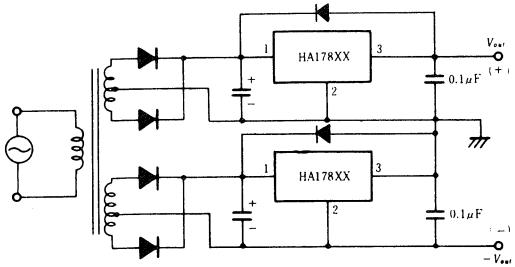
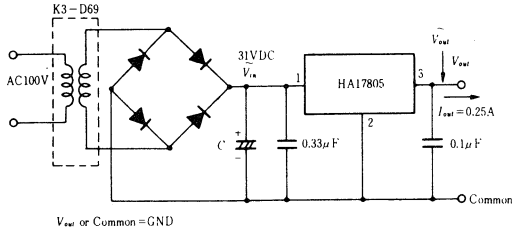
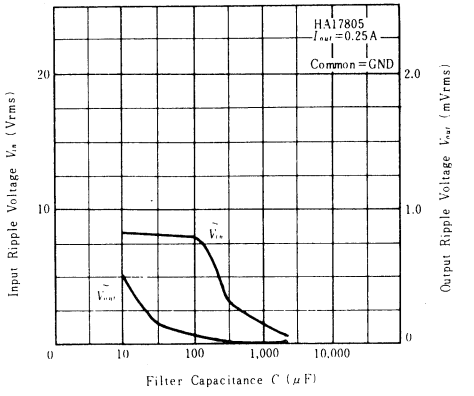


Fig.22 Positive and Negative Voltage Regulator

Fig. 23 shows the smoothing capacitance C and ripple characteristics at input and output when the transformer K3-D69 is employed.



(a) Fixed Output Regulator



(b) Input Output Ripple Characteristics

Fig.23 Characteristics of Fixed Output Regulator with a Rectifier

3.7 Switching Regulator

Fig. 24 shows the circuit of a switching regulator. This circuit stabilizes the output voltage with self-oscillating and the change in output voltage will be absorbed by changing the conducting period of the switching transistor Q. The minimum operational input voltage, V_{in} min is;

$$V_{in}\,\min = V_{XX} + V_Z(ZD_1) + V_{EB}(Q)$$

The zener diode, ZD_1 is to reduce the voltage applied to HA17800P and HA17800 series. The period during the switching element Q is ON becomes longer with the increasement of load current and the oscillation cycle is nearly proportional to the inductance L. The current capacitance of Q must be twice as large as the load current.

Fig. 25 shows the operational characteristics of the circuit in Fig. 24.

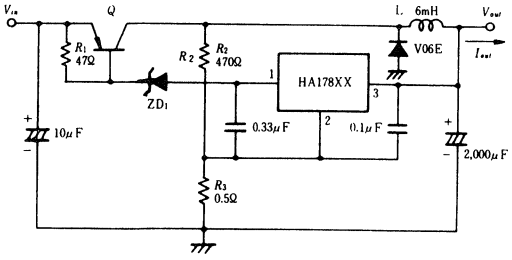


Fig.24 Switching Regulator

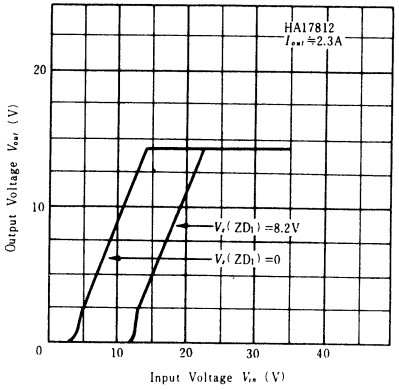


Fig.25 Operational Characteristics of the Switching Regulator

HA178L00P, HA178L00 Series

● 100mA 3-terminal Fixed Voltage Regulators

—Preliminary—

HA178L00 Series are 3-terminal fixed output voltage regulators. ICs can be applicable not only for stabilized power source, but also for zener diode because of its small outline package.

(TO-92M)

■TYPE AND GRADE

Output Voltage / Application	Standard Voltage tolerance ±8%	A version Voltage tolerance ±5%
Industrial Use	HA178L00P	HA178L00PA
Commercial Use	HA178L00	HA178L00A

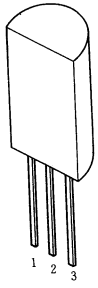
■FEATURES

- Maximum Output Current 150mA (Tj= 25°C)
- Large maximum power dissipation 800mW
- High accuracy voltage series (±5%) is provided.
- Overcurrent protection.
- Small TO –92 MOD package enable high density assembling.

■OUTPUT VOLTAGE AND TYPE

Output Voltage (V)	Type
2.5	HA178L02
5	HA178L05
5.6	HA178L56
6	HA178L06
8	HA178L08
9	HA178L09
10	HA178L10
12	HA178L12
15	HA178L15

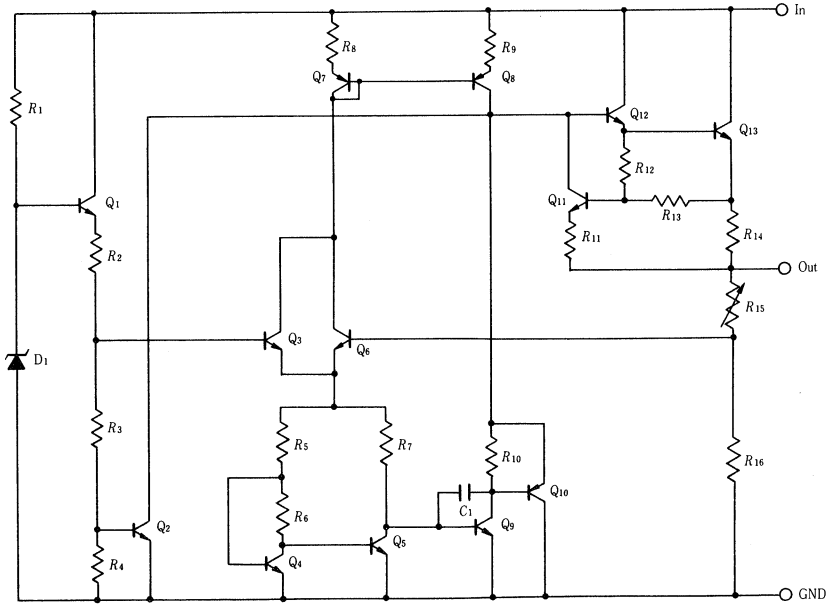
■PIN ARRANGEMENT



1. OUT
2. GND
3. IN

(Top View)

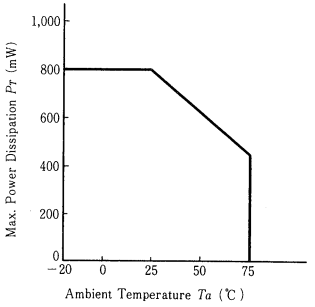
■CIRCUIT SCHEMATIC



■ABSOLUTE MAXIMUM RATINGS (T_a=25°C)

Item	Symbol	HA178L00PA HA178L00A HA178L00P HA178L00 Series	Unit
Input Voltage	V_{in}	35	V
Power Dissipation	P_T	800*	mW
Operating Ambient Temperature	T_{opr}	−20 to +75	°C
Storage Temperature	T_{stg}	−55 to +150	°C

* Value under T_a≧25°C in case of more than, 6.4mW/°C derating be down.



■HA178L02 ELECTRICAL CHARACTERISTICS

(V_{in} =10V, I_{out}=40mA, 0°C≦ T_j ≦125°C, C_{in}=0.33μF, C_{out} =0.1μF)

Item	Symbol	Test Conditions		HA178L02P HA178L02 min	typ	max	HA178L02PA HA178L02A min	typ	max	Unit
Output Voltage	V_{out}	T_j=25°C		2.32	2.48	2.64	2.38	2.48	2.58	V
Line Regulation	$\delta V_{O\ line}$	T_j=25°C	7V≦ V_{in} ≦20V	−	35	125	−	35	95	mV
			8V≦ V_{in} ≦20V	−	30	100	−	30	75	
Load Regulation	$\delta V_{O\ load}$	T_j=25°C	1.0mA≦ I_{out} ≦150mA	−	14	−	−	14	−	mV
			1.0mA≦ I_{out} ≦100mA	−	9.5	50	−	9.5	50	
			1.0mA≦ I_{out} ≦40mA	−	4.5	25	−	4.5	25	
Output Voltage	V_{out}	7V≦ V_{in} ≦20V, 1.0mA≦ I_{out} ≦40mA		2.28	−	2.68	2.35	−	2.61	V
		V_{in}=9V, 1.0mA≦ I_{out} ≦70mA		2.28	−	2.68	2.35	−	2.61	
Quiescent Current	I_Q	T_j=25°C		−	3.0	6.0	−	3.0	6.0	mA
		T_j=125°C		−	−	5.5	−	−	5.5	
Quiescent Current Change	δI_Q	8V≦ V_{in} ≦20V		−	−	1.5	−	−	1.5	mA
		1.0mA≦ I_{out} ≦40mA		−	−	0.2	−	−	0.1	
Output Noise Voltage	V_n	T_a=25°C, 10Hz≦ f ≦100kHz		−	30	−	−	30	−	μV
Ripple Rejection Ratio	R_{REJ}	f=120Hz, 8.0V≦ V_{in} ≦18V, T_j=25°C		−	51	−	−	51	−	dB
Temperature Coefficient of Output Voltage	$\delta V_{out}/\delta T_j$	I_{out}=5mA		−	−0.32	−	−	−0.32	−	mV/°C

■HA178L05 ELECTRICAL CHARACTERISTICS

(V_{in}=10V, I_{out}=40mA, 0°C≦T_j≦125°C, C_{in}=0.33μF, C_{out}=0.1μF)

Item	Symbol	Test Conditions		HA178L05P HA178L05			HA178L05PA HA178L05A			Unit
				min	typ	max	min	typ	max	
Output Voltage	V_{out}	T_j=25°C		4.68	5.0	5.32	4.8	5.0	5.2	V
Line Regulation	$\delta V_{O\ line}$	T_j=25°C	7V≦V_{in}≦20V	–	55	200	–	55	150	mV
			8V≦V_{in}≦20V	–	45	150	–	45	100	
Load Regulation	$\delta V_{O\ load}$	T_j=25°C	1.0mA≦I_{out}≦150mA	–	16	–	–	16	–	mV
			1.0mA≦I_{out}≦100mA	–	11	60	–	11	60	
			1.0mA≦I_{out}≦40mA	–	5.0	30	–	5.0	30	
Output Voltage	V_{out}	7V≦V_{in}≦20V, 1.0mA≦I_{out}≦40mA		4.6	–	5.4	4.75	–	5.25	V
		V_{in}=10V, 1.0mA≦I_{out}≦70mA		4.6	–	5.4	4.75	–	5.25	
Quiescent Current	I_Q	T_j=25°C		–	3.0	6.0	–	3.0	6.0	mA
		T_j=125°C		–	–	5.5	–	–	5.5	
Quiescent Current Change	δI_Q	8.0V≦V_{in}≦20V		–	–	1.5	–	–	1.5	mA
		1.0mA≦I_{out}≦40mA		–	–	0.2	–	–	0.1	
Output Noise Voltage	V_n	T_a=25°C, 10Hz≦f≦100kHz		–	40	–	–	40	–	μV
Ripple Rejection Ratio	R_{REJ}	f=120Hz, 8.0V≦V_{in}≦18V, T_j=25°C		–	49	–	–	49	–	dB
Temperature Coefficient of Output Voltage	$\delta V_{out}/\delta T_j$	I_{out}=5mA		–	−0.6	–	–	−0.6	–	mV/°C
Voltage Drop	V_{drop}	T_j=25°C		–	1.7	–	–	1.7	–	V

■HA178L56 ELECTRICAL CHARACTERISTICS

(V_{in}=11V, I_{out}=40mA, 0°C≦T_j≦125°C, C_{in}=0.33μF, C_{out}=0.1μF)

Item	Symbol	Test Conditions		HA178L56P HA178L56			HA178L56PA HA178L56A			Unit
				min	typ	max	min	typ	max	
Output Voltage	V_{out}	T_j=25°C		5.24	5.6	5.96	5.38	5.6	5.82	V
Line Regulation	$\delta V_{O\ line}$	T_j=25°C	7.6V≦V_{in}≦21V	–	50	200	–	50	150	mV
			8.5V≦V_{in}≦21V	–	45	150	–	45	100	
Load Regulation	$\delta V_{O\ load}$	T_j=25°C	1.0mA≦I_{out}≦150mA	–	17	–	–	17	–	mV
			1.0mA≦I_{out}≦100mA	–	11	60	–	11	60	
			1.0mA≦I_{out}≦40mA	–	5.0	30	–	5.0	30	
Output Voltage	V_{out}	7.6V≦V_{in}≦21V, 1.0mA≦I_{out}≦40mA		5.16	–	6.04	5.32	–	5.88	V
		V_{in}=11V, 1.0mA≦I_{out}≦70mA		5.16	–	6.04	5.32	–	5.88	
Quiescent Current	I_Q	T_j=25°C		–	3.0	6.0	–	3.0	6.0	mA
		T_j=125°C		–	–	5.5	–	–	5.5	
Quiescent Current Change	δI_Q	8.5V≦V_{in}≦20V		–	–	1.5	–	–	1.5	mA
		1.0mA≦I_{out}≦40mA		–	–	0.2	–	–	0.1	
Output Noise Voltage	V_n	T_a=25°C, 10Hz≦f≦100kHz		–	40	–	–	40	–	μV
Ripple Rejection Ratio	R_{REJ}	f=120Hz, 8.5V≦V_{in}≦18.5V, T_j=25°C		–	49	–	–	49	–	dB
Temperature Coefficient of Output Voltage	$\delta V_{out}/\delta T_j$	I_{out}=5mA		–	−0.65	–	–	−0.65	–	mV/°C
Voltage Drop	V_{drop}	T_j=25°C		–	1.7	–	–	1.7	–	V

■HA178L06 ELECTRICAL CHARACTERISTICS

(V_{in}=11V, I_{out}=40mA, 0°C≦T_j≦125°C, C_{in}=0.33μF, C_{out}=0.1μF)

Item	Symbol	Test Conditions		HA178L06P HA178L06			HA178L06PA HA178L06A			Unit
				min	typ	max	min	typ	max	
Output Voltage	V_{out}	T_j=25°C		5.61	6.0	6.39	5.76	6.0	6.24	V
Line Regulation	$\delta V_{O\ line}$	T_j=25°C	8.1V≦V_{in}≦21V	–	50	200	–	50	150	mV
			9.0V≦V_{in}≦21V	–	45	150	–	45	110	
Load Regulation	$\delta V_{O\ load}$	T_j=25°C	1.0mA≦I_{out}≦150mA	–	17.5	–	–	17.5	–	mV
			1.0mA≦I_{out}≦100mA	–	12	70	–	12	70	
			1.0mA≦I_{out}≦40mA	–	5.5	25	–	5.5	35	
Output Voltage	V_{out}	8.1V≦V_{in}≦21V, 1.0mA≦I_{out}≦40mA		5.52	–	6.48	5.7	–	6.3	V
		V_{in}=11V, 1.0mA≦I_{out}≦70mA		5.52	–	6.48	5.7	–	6.3	
Quiescent Current	I_Q	T_j=25°C		–	3.0	6.0	–	3.0	6.0	mA
		T_j=125°C		–	–	5.5	–	–	5.5	
Quiescent Current Change	δI_Q	9.0V≦V_{in}≦20V		–	–	1.5	–	–	1.5	mA
		1.0mA≦I_{out}≦40mA		–	–	0.2	–	–	0.1	
Output Noise Voltage	V_n	T_a=25°C, 10Hz≦f≦100kHz		–	40	–	–	40	–	μV
Ripple Rejection Ratio	R_{REJ}	f=120Hz, 9.0V≦V_{in}≦19V, T_j=25°C		–	47	–	–	47	–	dB
Temperature Coeffieient of Output Voltage	$\delta V_{out}/\delta T_j$	I_{out}=5mA		–	−0.7	–	–	−0.7	–	mV/°C
Voltage Drop	V_{drop}	T_j=25°C		–	1.7	–	–	1.7	–	V

■HA178L08 ELECTRICAL CHARACTERISTICS

(V_{in}=14V, I_{out}=40mA, 0°C≦T_j≦125°C, C_{in}=0.33μF, C_{out}=0.1μF)

Item	Symbol	Test Conditions		HA178L08P HA178L08			HA178L08PA HA178L08A			Unit
				min	typ	max	min	typ	max	
Output Voltage	V_{out}	T_j=25°C		7.48	8.0	8.52	7.7	8.0	8.3	V
Line Regulation	$\delta V_{O\ line}$	T_j=25°C	10.5V≦V_{in}≦23V	–	20	200	–	20	175	mV
			11V≦V_{in}≦23V	–	12	150	–	12	125	
Load Regulation	$\delta V_{O\ load}$	T_j=25°C	1.0mA≦I_{out}≦150mA	–	22	–	–	22	–	mV
			1.0mA≦I_{out}≦100mA	–	15	80	–	15	80	
			1.0mA≦I_{out}≦40mA	–	7.0	40	–	7.0	40	
Output Voltage	V_{out}	10.5V≦V_{in}≦23V, 1.0mA≦I_{out}≦40mA		7.36	–	8.64	7.6	–	8.4	V
		V_{in}=14V, 1.0mA≦I_{out}≦70mA		7.36	–	8.64	7.6	–	8.4	
Quiescent Current	I_Q	T_j=25°C		–	3.0	6.5	–	3.0	6.5	mA
		T_j=125°C		–	–	6.0	–	–	6.0	
Quiescent Current Change	δI_Q	11V≦V_{in}≦23V		–	–	1.5	–	–	1.5	mA
		1.0mA≦I_{out}≦40mA		–	–	0.2	–	–	0.1	
Output Noise Voltage	V_n	T_a=25°C, 10Hz≦f≦100kHz		–	60	–	–	60	–	μV
Ripple Rejection Ratio	R_{REJ}	f=120Hz, 12V≦V_{in}≦23V, T_j=25°C		–	45	–	–	45	–	dB
Temperature Coefficient of Output Voltage	$\delta V_{out}/\delta T_j$	I_{out}=5mA		–	−0.8	–	–	−0.8	–	mV/°C
Voltage Drop	V_{drop}	T_j=25°C		–	1.7	–	–	1.7	–	V

■HA178L09 ELECTRICAL CHARACTERISTICS

(V_{in}=15V, I_{out}=40mA, 0°C≦T_j≦125°C, C_{in}=0.33μF, C_{out}=0.1μF)

Item	Symbol	Test Conditions		HA178L09P HA178L09			HA178L09PA HA178L09A			Unit
				min	typ	max	min	typ	max	
Output Voltage	V_{out}	T_j=25°C		8.42	9.0	9.58	8.64	9.0	9.36	V
Line Regulation	$\delta V_{O\ line}$	T_j=25°C	11.4V≦V_{in}≦24V	–	80	230	–	80	200	mV
			12V≦V_{in}≦24V	–	20	160	–	20	160	
Load Regulation	$\delta V_{O\ load}$	T_j=25°C	1.0mA≦I_{out}≦150mA	–	24.5	–	–	24.5	–	mV
			1.0mA≦I_{out}≦100mA	–	17	90	–	17	90	
			1.0mA≦I_{out}≦40mA	–	8.0	45	–	8.0	45	
Output Voltage	V_{out}	11.4V≦V_{in}≦24V, 1.0mA≦I_{out}≦40mA		8.28	–	9.72	8.55	–	9.45	V
		V_{in}=15V, 1.0mA≦I_{out}≦70mA		8.28	–	9.72	8.55	–	9.45	
Quiescent Current	I_Q	T_j=25°C		–	3.1	6.5	–	3.1	6.5	mA
		T_j=125°C		–	–	6.0	–	–	6.0	
Quiescent Current Change	δI_Q	12V≦V_{in}≦24V		–	–	1.5	–	–	1.5	mA
		1.0mA≦I_{out}≦40mA		–	–	0.2	–	–	0.1	
Output Noise Voltage	V_n	T_a=25°C, 10Hz≦f≦100kHz		–	65	–	–	65	–	μV
Ripple Rejection Ratio	R_{REJ}	f=120Hz, 12V≦V_{in}≦24V, T_j=25°C		–	44	–	–	44	–	dB
Temperature Coefficient of Output Voltage	$\delta V_{out}/\delta T_j$	I_{out}=5mA		–	−0.85	–	–	−0.85	–	mV/°C
Voltage Drop	V_{drop}	T_j=25°C		–	1.7	–	–	1.7	–	V

■HA178L10 ELECTRICAL CHARACTERISTICS

(V_{in}=16V, I_{out}=40mA, 0°C≦T_j≦125°C, C_{in}=0.33μF, C_{out}=0.1μF)

Item	Symbol	Test Conditions		HA178L10P HA178L10			HA178L10PA HA178L10A			Unit
				min	typ	max	min	typ	max	
Output Voltage	V_{out}	T_j=25°C		9.35	10	10.65	9.6	10	10.4	V
Line Regulation	$\delta V_{O line}$	T_j=25°C	12.5V≦V_{in}≦25V	–	80	230	–	80	230	mV
			13V≦V_{in}≦25V	–	30	170	–	30	170	
Load Regulation	$\delta V_{O\ load}$	T_j=25°C	1.0mA≦I_{out}≦150mA	–	26	–	–	26	–	mV
			1.0mA≦I_{out}≦100mA	–	18	90	–	18	90	
			1.0mA≦I_{out}≦40mA	–	8.5	45	–	8.5	45	
Output Voltage	V_{out}	12.5V≦V_{in}≦25V, 1.0mA≦I_{out}≦40mA		9.2	–	10.8	9.5	–	10.5	V
		V_{in}=16V, 1.0mA≦I_{out}≦70mA		9.2	–	10.8	9.5	–	10.5	
Quiescent Current	I_Q	T_j=25°C		–	3.1	6.5	–	3.1	6.5	mA
		T_j=125°C		–	–	6.0	–	–	6.0	
Quiescent Current Change	δI_Q	13V≦V_{in}≦25V		–	–	1.5	–	–	1.5	mA
		1.0mA≦I_{out}≦40mA		–	–	0.2	–	–	0.1	
Output Noise Voltage	V_n	T_a=25°C, 10Hz≦f≦100kHz		–	70	–	–	70	–	μV
Ripple Rejection Ratio	R_{REJ}	f=120Hz, 13V≦V_{in}≦24V, T_j=25°C		–	43	–	–	43	–	dB
Temperature Coefficient of Output Voltage	$\delta V_{out}/\delta T_j$	I_{out}=5mA		–	−0.9	–	–	−0.9	–	mV/°C
Voltage Drop	V_{drop}	T_j=25°C		–	1.7	–	–	1.7	–	V

■HA178L12 ELECTRICAL CHARACTERISTICS

(V_{in}=19V, I_{out}=40mA, 0°C≦T_j≦125°C, C_{in}=0.33μF, C_{out}=0.1μF)

Item	Symbol	Test Conditions		HA178L12P HA178L12			HA178L12PA HA178L12A			Unit
				min	typ	max	min	typ	max	
Output Voltage	V_{out}	T_j=25°C		11.22	12	12.78	11.5	12	12.5	V
Line Regulation	$\delta V_{O\ line}$	T_j=25°C	14.5V≦V_{in}≦27V	–	120	250	–	120	250	mV
			16V≦V_{in}≦27V	–	100	200	–	100	200	
Load Regulation	$\delta V_{O\ load}$	T_j=25°C	1.0mA≦I_{out}≦150mA	–	28.5	–	–	28.5	–	mV
			1.0mA≦I_{out}≦100mA	–	20	100	–	20	100	
			1.0mA≦I_{out}≦40mA	–	10	50	–	10	50	
Output Voltage	V_{out}	14.5V≦V_{in}≦27V, 1.0mA≦I_{out}≦40mA		11.04	–	12.96	11.4	–	12.6	V
		V_{in}=19V, 1.0mA≦I_{out}≦70mA		11.04	–	12.96	11.4	–	12.6	
Quiescent Current	I_Q	T_j=25°C		–	3.1	6.5	–	3.1	6.5	mA
		T_j=125°C		–	–	6.0	–	–	6.0	
Quiescent Current Change	δI_Q	16V≦V_{in}≦27V		–	–	1.5	–	–	1.5	mA
		1.0mA≦I_{out}≦40mA		–	–	0.2	–	–	0.1	
Output Noise Voltage	V_n	T_a=25°C, 10Hz≦f≦100kHz		–	80	–	–	80	–	μV
Ripple Rejection Ratio	R_{REJ}	f=120Hz, 15V≦V_{in}≦25V, T_j=25°C		–	41	–	–	41	–	dB
Temperature Coefficient of Output Voltage	$\delta V_{out}/\delta T_j$	I_{out}=5mA		–	−1.0	–	–	−1.0	–	mV/°C
Voltage Drop	V_{drop}	T_j=25°C		–	1.7	–	–	1.7	–	V

■HA178L15 ELECTRICAL CHARACTERISTICS

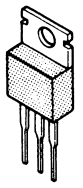
(V_{in}=23V, I_{out}=40mA, 0°C≦T_j≦125°C, C_{in}=0.33μF, C_{out}=0.1μF)

Item	Symbol	Test Conditions		HA178L15P HA178L15			HA178L15PA HA178L15A			Unit
				min	typ	max	min	typ	max	
Output Voltage	V_{out}	T_j=25°C		14.03	15	15.97	14.4	15	15.6	V
Line Regulation	$\delta V_{O\ line}$	T_j=25°C	17.5V≦V_{in}≦30V	–	130	300	–	130	300	mV
			20V≦V_{in}≦30V	–	110	250	–	110	250	
Load Regulation	$\delta V_{O\ load}$	T_j=25°C	1.0mA≦I_{out}≦150mA	–	36	–	–	36	–	mV
			1.0mA≦I_{out}≦100mA	–	25	150	–	25	150	
			1.0mA≦I_{out}≦40mA	–	12	75	–	12	75	
Output Voltage	V_{out}	17.5V≦V_{in}≦30V, 1.0mA≦I_{out}≦40mA		13.8	–	16.2	14.25	–	15.75	V
		V_{in}=23V, 1.0mA≦I_{out}≦70mA		13.8	–	16.2	14.25	–	15.75	
Quiescent Current	I_Q	T_j=25°C		–	3.2	6.5	–	3.2	6.5	mA
		T_j=125°C		–	–	6.0	–	–	6.0	
Quiescent Current Change	δI_Q	20V≦V_{in}≦30V		–	–	1.5	–	–	1.5	mA
		1.0mA≦I_{out}≦40mA		–	–	0.2	–	–	0.1	
Output Noise Voltage	V_n	T_a=25°C, 10Hz≦f≦100kHz		–	90	–	–	90	–	μV
Ripple Rejection Ratio	R_{REJ}	f=120Hz, 18.5V≦V_{in}≦28.5V, T_j=25°C		–	40	–	–	40	–	dB
Temperature Coefficient of Output Voltage	$\delta V_{out}/\delta T_j$	I_{out}=5mA		–	−1.3	–	–	−1.3	–	mV/°C
Voltage Drop	V_{drop}	T_j=25°C		–	1.7	–	–	1.7	–	V

HA178M00P,HA178M00 Series ● 3-terminal Fixed Voltage Regulators

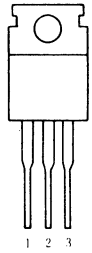
■ FEATURES

- Output Current more than 500mA
- Possible to be widely used as power source with various output voltage; 5V, 6V, 7V, 8V, 12V, 15V, 18V, 20V & 24V
- No external compensation circuit required.
- T0-220AB package and easy mounting & easy design for heat sink, as same as a transistor.
- Built-in current control circuit protects elements from destruction by short circuit.
- Chip junction temperature limiting circuit built in protects elements from thermal destruction.
- Internal power dissipation limiting circuit built in protects transistors in output stage.
- Industrial Use; . . . . . HA178M00P Series
- Commercial Use; . . . . . HA178M00 Series



(T-220AB)

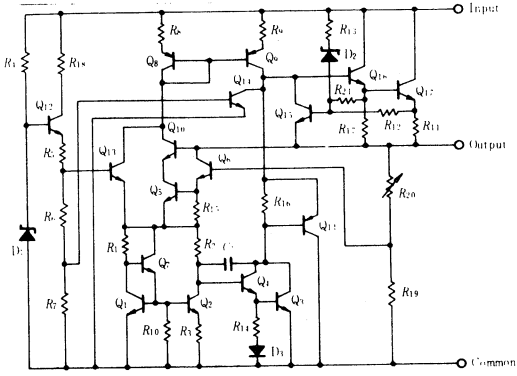
■ PIN ARRANGEMENT



Top View

1. Input
2. Common
3. Output

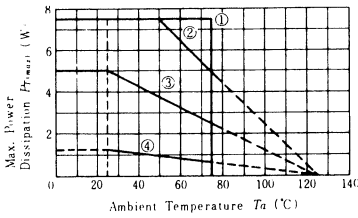
■ CIRCUIT SCHEMATIC



■ ABSOLUTE MAXIMUM RATINGS ($Ta = 25°C$)

Item	Symbol	Rating	Unit
Input Voltage	V_{in}*	35	V
Input Voltage	V_{in}**	40	V
Power Dissipation	P_T***	7.5	W
Operating Temperature	T_{opr}	−20 to +75	°C
Junction Temperature	T_j	−20 to +125	°C
Storage Temperature	T_{stg}	−55 to +125	°C

Note * For HA178M05P ~ HA178M18P, HA178M05 ~ HA178M18
** For HA178M20P, HA178M24P, HA178M20, HA178M24
*** Follow the derating curve shown below.

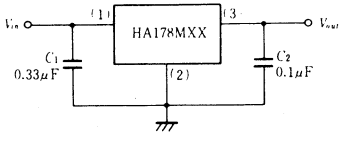


① Infinity heat sink
② 5°C/W heat sink | Included fixed thermal
③ 15°C/W heat sink | resistance
④ No heat sink

thermal resistance

θ_{j-c} = 3.0°C/W (typ)
5.0°C/W (max)
θ_{j-a} = 62°C/W (typ)
72°C/W (max)

■ STANDARD CONNECTING CIRCUIT



HA178M05P,HA178M05 ELECTRICAL CHARACTERISTICS

(V_{in}=10V, I_{out}=350mA, 0°C ≦ T_j ≦ 125°C, C_{in}=0.33μF, C_{out}=0.1μF, unless otherwise specified.)

Item	Symbol	Test Condition		min	typ	max	Unit
Output Voltage	V_{out}	T_j=25°C		4.8	5.0	5.2	V
		7V ≦ V_{in} ≦ 20V, P_T ≦ 7.5W, 5mA ≦ I_{out} ≦ 350mA		4.75	—	5.25	
Line Regulation	$\delta V_{o\ line}$	T_j=25°C	7V ≦ V_{in} ≦ 25V, I_{out}=200mA	—	3	100	mV
			8V ≦ V_{in} ≦ 25V, I_{out}=200mA	—	1	50	
Load Regulation	$\delta V_{o\ load}$	T_j=25°C	5mA ≦ I_{out} ≦ 500mA	—	20	100	mV
			5mA ≦ I_{out} ≦ 200mA	—	10	50	
Quiescent Current	I_Q	T_j=25°C, I_{out}=0		—	4.5	6.0	mA
Quiescent Current Change	δI_Q	8V ≦ V_{in} ≦ 25V, I_{out}=200mA		—	—	0.8	mA
		5mA ≦ I_{out} ≦ 350mA		—	—	0.5	
Output Noise Voltage	V_n	Ta=25°C, 10Hz ≦ f ≦ 100kHz		—	40	—	μV
Ripple Rejection Ratio	R_{REJ}	f=120Hz, T_j=25°C	I_{out}=100mA	62	80	—	dB
			I_{out}=300mA	62	80	—	
Drop Out Voltage	V_{drop}	I_{out}=350mA, T_j=25°C		—	2.0	—	V
Output Short-circuit Current	I_{OS}	T_j=25°C, V_{in}=35V		—	300	—	mA
Peak Output Current	$I_{o\ peak}$	T_j=25°C		—	700	—	mA
Temperature Coefficient of Output Voltage	$\delta V_{out}/\delta T_j$	I_{out}=5mA, 0°C ≦ T_j ≦ 125°C		—	−1.0	—	mV/°C

HA178M06P,HA178M06 ELECTRICAL CHARACTERISTICS

(V_{in}=11V, I_{out}=350mA, 0°C ≦ T_j ≦ 125°C, C_{in}=0.33μF, C_{out}=0.1μF, unless otherwise specified.)

Item	Symbol	Test Condition		min	typ	max	Unit
Output Voltage	V_{out}	T_j=25°C		5.75	6.0	6.25	V
		8V ≦ V_{in} ≦ 21V, P_T ≦ 7.5W, 5mA ≦ I_{out} ≦ 350mA		5.7	—	6.3	
Line Regulation	δV_{line}	T_j=25°C	8V ≦ V_{in} ≦ 25V, I_{out}=200mA	—	5	100	mV
			9V ≦ V_{in} ≦ 25V, I_{out}=200mA	—	1.5	50	
Load Regulation	δV_{load}	T_j=25°C	5mA ≦ I_{out} ≦ 500mA	—	20	120	mV
			5mA ≦ I_{out} ≦ 200mA	—	10	60	
Quiescent Current	I_Q	T_j=25°C, I_{out}=0		—	4.5	6.0	mA
Quiescent Current Change	δI_Q	9V ≦ V_{in} ≦ 25V, I_{out} ≦ 200mA		—	—	0.8	mA
		5mA ≦ I_{out} ≦ 350mA		—	—	0.5	
Output Noise Voltage	V_n	Ta=25°C, 10Hz ≦ f ≦ 100kHz		—	45	—	μV
Ripple Rejection Ratio	R_{REF}	f=120Hz, T_j=25°C	I_{out}=100mA	59	80	—	dB
			I_{out}=300mA	59	80	—	
Drop Out Voltage	V_{drop}	I_{out}=350mA, T_j=25°C		—	2.0	—	V
Output Short-circuit Current	I_{OS}	T_j=25°C, V_{in}=35V		—	270	—	mA
Peak Output Current	$I_{o\ peak}$	T_j=25°C		—	700	—	mA
Temperature Coefficient of Output Voltage	$\delta V_{out}/\delta T_j$	I_{out}=5mA, 0°C ≦ T_j ≦ 125°C		—	−0.5	—	mV/°C

HA178M07P,HA178M07 ELECTRICAL CHARACTERISTICS

(V_{in}=12.5V, I_{out}=350mA, 0°C ≦ T_j ≦ 125°C, C_{in}=0.33μF, C_{out}=0.1μF, unless otherwise specified.)

Item	Symbol	Test Condition		min	typ	max	Unit
Output Voltage	V_{out}	T_j=25°C		6.72	7.0	7.28	V
		9V ≦ V_{in} ≦ 22V, P_T ≦ 7.5W, 5mA ≦ I_{out} ≦ 350mA		6.65	—	7.35	
Line Regulation	$\delta V_{o\ line}$	T_j=25°C	9V ≦ V_{in} ≦ 25V, I_{out}=200mA	—	5.5	100	mV
			10V ≦ V_{in} ≦ 25V, I_{out}=200mA	—	1.7	50	
Load Regulation	$\delta V_{o\ load}$	T_j=25°C	5mA ≦ I_{out} ≦ 500mA	—	23	140	mV
			5mA ≦ I_{out} ≦ 200mA	—	10	70	
Quiescent Current	I_Q	T_j=25°C, I_{out}=0		—	4.6	6.0	mA
Quiescent Current Change	δI_Q	10V ≦ V_{in} ≦ 25V, I_{out}=200mA		—	—	0.8	mA
		5mA ≦ I_{out} ≦ 350mA		—	—	0.5	
Output Noise Voltage	V_n	Ta=25°C, 10Hz ≦ f ≦ 100kHz		—	48.5	—	μV
Ripple Rejection Ratio	R_{REF}	f=120Hz, T_j=25°C	I_{out}=100mA	57	80	—	dB
			I_{out}=300mA	57	80	—	
Drop Out Voltage	V_{drop}	I_{out}=350mA, T_j=25°C		—	2.0	—	V
Output Short-circuit Current	I_{OS}	T_j=25°C, V_{in}=35V		—	260	—	mA
Peak Output Current	$I_{o\ peak}$	T_j=25°C		—	700	—	mA
Temperature Coefficient of Output Voltage	$\delta V_{out}/\delta T_j$	I_{out}=5mA, 0°C ≦ T_j ≦ 125°C		—	−0.5	—	mV/°C

■HA178M08P,HA178M08 ELECTRICAL CHARACTERISTICS

(V_{in}=14V, I_{out}=350mA, 0°C≦T_j≦125°C, C_{in}=0.33μF, C_{out}=0.1μF, unless otherwise specified.)

Item	Symbol	Test Condition		min	typ	max	Unit
Output Voltage	V_{out}	T_j=25°C		7.7	8.0	8.3	V
		10.5V≦V_{in}≦23V, P_T≦7.5W, 5mA≦I_{out}≦350mA		7.6	—	8.4	
Line Regulation	$\delta V_{o\ line}$	T_j=25°C	10.5V≦V_{in}≦25V, I_{out}=200mA	—	6.0	100	mV
			11V≦V_{in}≦25V, I_{out}=200mA	—	2.0	50	
Load Regulation	$\delta V_{o\ load}$	T_j=25°C	5mA≦I_{out}≦500mA	—	25	160	mV
			5mA≦I_{out}≦200mA	—	10	80	
Quiescent Current	I_Q	T_j=25°C, I_{out}=0		—	4.6	6.0	mA
Quiescent Current Change	δI_Q	10.5V≦V_{in}≦25V, I_{out}=200mA		—	—	0.8	mA
		5mA≦I_{out}≦350mA		—	—	0.5	
Output Noise Voltage	V_n	Ta=25°C, 10Hz≦f≦100kHz		—	52	—	μV
Ripple Rejection Ratio	R_{REF}	f=120Hz,	I_{out}=100mA	56	80	—	dB
		T_j=25°C	I_{out}=300mA	56	80	—	
Drop Out Voltage	V_{drop}	I_{out}=350mA, T_j=25°C		—	2.0	—	V
Output Short-circuit Current	I_{OS}	T_j=25°C, V_{in}=35V		—	250	—	mA
Peak Output Current	$I_{o\ peak}$	T_j=25°C		—	700	—	mA
Temperature Coefficient of Output Voltage	$\delta V_{out}/\delta T_j$	I_{out}=5mA, 0°C≦T_j≦125°C		—	−0.5	—	mV/°C

■HA178M12P,HA178M12 ELECTRICAL CHARACTERISTICS

(V_{in}=19V, I_{out}=350mA, 0°C≦T_j≦125°C, C_{in}=0.33μF, C_{out}=0.1μF, unless otherwise specified.)

Item	Symbol	Test Condition		min	typ	max	Unit
Output Voltage	V_{out}	T_j=25°C		11.5	12.0	12.5	V
		14.5V≦V_{in}≦27V, P_T≦7.5W, 5mA≦I_{out}≦350mA		11.4	—	12.6	
Line Regulation	$\delta V_{o\ line}$	T_j=25°C	14.5V≦V_{in}≦30V, I_{out}=200mA	—	8.0	100	mV
			16V≦V_{in}≦30V, I_{out}=200mA	—	2.0	50	
Load Regulation	$\delta V_{o\ load}$	T_j=25°C	5mA≦I_{out}≦500mA	—	25	240	mV
			5mA≦I_{out}≦200mA	—	10	120	
Quiescent Current	I_Q	T_j=25°C, I_{out}=0		—	4.8	6.0	mA
Quiescent Current Change	δI_Q	14.5V≦V_{in}≦30V, I_{out}=200mA		—	—	0.8	mA
		5mA≦I_{out}≦350mA		—	—	0.5	
Output Noise Voltage	V_n	Ta=25°C, 10Hz≦f≦100kHz		—	75	—	μV
Ripple Rejection Ratio	R_{REF}	f=120Hz,	I_{out}=100mA	55	80	—	dB
		T_j=25°C	I_{out}=300mA	55	80	—	
Drop Out Voltage	V_{drop}	I_{out}=350mA, T_j=25°C		—	2.0	—	V
Output Short-circuit Current	I_{OS}	T_j=25°C, V_{in}=35V		—	440	—	mA
Peak Output Current	$I_{o\ peak}$	T_j=25°C		—	700	—	mA
Temperature Coefficient of Output Voltage	$\delta V_{out}/\delta T_j$	I_{out}=5mA, 0°C≦T_j≦125°C		—	−1.0	—	mV/°C

■HA178M15P,HA178M15 ELECTRICAL CHARACTERISTICS

(V_{in}=23V, I_{out}=350mA, 0°C≦T_j≦125°C, C_{in}=0.33μF, C_{out}=0.1μF, unless otherwise specified.)

Item	Symbol	Test Condition		min	typ	max	Unit
Output Voltage	V_{out}	T_j=25°C		14.4	15.0	15.6	V
		17.5V≦V_{in}≦30V, P_T≦7.5W, 5mA≦I_{out}≦350mA		14.25	—	15.75	
Line Regulation	$\delta V_{o\ line}$	T_j=25°C	17.5V≦V_{in}≦30V, I_{out}=200mA	—	10	100	mV
			20V≦V_{in}≦30V, I_{out}=200mA	—	3.0	50	
Load Regulation	$\delta V_{o\ load}$	T_j=25°C	5mA≦I_{out}≦500mA	—	25	300	mV
			5mA≦I_{out}≦200mA	—	10	150	
Quiescent Current	I_Q	T_j=25°C, I_{out}=0		—	4.8	6.0	mA
Quiescent Current Change	δI_Q	17.5V≦V_{in}≦30V, I_{out}=200mA		—	—	0.8	mA
		5mA≦I_{out}≦350mA		—	—	0.5	
Output Noise Voltage	V_n	Ta=25°C, 10Hz≦f≦100kHz		—	90	—	μV
Ripple Rejection Ratio	R_{REF}	f=120Hz,	I_{out}=100mA	54	70	—	dB
		T_j=25°C	I_{out}=300mA	54	70	—	
Drop Out Voltage	V_{drop}	I_{out}=350mA, T_j=25°C		—	2.0	—	V
Output Short-circuit Current	I_{OS}	T_j=25°C, V_{in}=35V		—	240	—	mA
Peak Output Current	$I_{o\ peak}$	T_j=25°C		—	700	—	mA
Temperature Coefficient of Output Voltage	$\delta V_{out}/\delta T_j$	I_{out}=5mA, 0°C≦T_j≦125°C		—	−1.0	—	mV/°C

■ HA178M18P,HA178M18 ELECTRICAL CHARACTERISTICS

(V_{in}=27V, I_{out}=350mA, 0℃ ≦ T_j ≦ 125℃, C_{in}=0.33μF, C_{out}=0.1μF, unless otherwise specified.)

Item	Symbol	Test Condition		min	typ	max	Unit
Output Voltage	V_{out}	T_j=25℃		17.3	18.0	18.7	V
		21V ≦ V_{in} ≦ 33V, P_T ≦ 7.5W, 5mA ≦ I_{out} ≦ 350mA		17.1	—	18.9	
Line Regulation	$\delta V_{o\ line}$	T_j=25℃	21V ≦ V_{in} ≦ 33V, I_{out}=200mA	—	10	100	mV
			24V ≦ V_{in} ≦ 33V, I_{out}=200mA	—	5.0	50	
Load Regulation	$\delta V_{o\ load}$	T_j=25℃	5mA ≦ I_{out} ≦ 500mA	—	25	360	mV
			5mA ≦ I_{out} ≦ 200mA	—	10	180	
Quiescent Current	I_Q	T_j=25℃, I_{out}=0		—	4.8	6.0	mA
Quiescent Current Change	δI_Q	21 ≦ V_{in} ≦ 35V, I_{out}=200mA		—	—	0.8	mA
		5mA ≦ I_{out} ≦ 350mA		—	—	0.5	
Output Noise Voltage	V_n	Ta=25℃, 10Hz ≦ f ≦ 100kHz		—	110	—	μV
Ripple Rejection Ratio	R_{REF}	f=120Hz, T_j=25℃	I_{out}=100mA	53	70	—	dB
			I_{out}=300mA	53	70	—	
Drop Out Voltage	V_{drop}	I_{out}=350mA, T_j=25℃		—	2.0	—	V
Output Short-circuit Current	I_{OS}	T_j=25℃, V_{in}=35V		—	240	—	mA
Peak Output Current	$I_{o\ peak}$	T_j=25℃		—	700	—	mA
Temperature Coefficient of Output Voltage	$\delta V_{out}/\delta T_j$	I_{out}=5mA, 0℃ ≦ T_j ≦ 125℃		—	−1.0	—	mV/℃

■ HA178M20P,HA178M20 ELECTRICAL CHARACTERISTICS

(V_{in}=29V, I_{out}=350mA, 0℃ ≦ T_j ≦ 125℃, C_{in}=0.33μF, C_{out}=0.1μF, unless otherwise specified.)

Item	Symbol	Test Condition		min	typ	max	Unit
Output Voltage	V_{out}	T_j=25℃		19.2	20	20.8	V
		23V ≦ V_{in} ≦ 35V, P_T ≦ 7.5W, 5mA ≦ I_{out} ≦ 350mA		19	—	21	
Line Regulation	$\delta V_{o\ line}$	T_j=25℃	23V ≦ V_{in} ≦ 35V, I_{out}=200mA	—	10	100	mV
			24V ≦ V_{in} ≦ 35V, I_{out}=200mA	—	5.0	50	
Load Regulation	$\delta V_{o\ load}$	T_j=25℃	5mA ≦ I_{out} ≦ 500mA	—	30	400	mV
			5mA ≦ I_{out} ≦ 200mA	—	10	200	
Quiescent Current	I_Q	T_j=25℃, I_{out}=0		—	4.9	6.0	mA
Quiescent Current	δI_Q	23V ≦ V_{in} ≦ 35V, I_{out}=200mA		—	—	0.8	mA
		5mA ≦ I_{out} ≦ 350mA		—	—	0.5	
Output Noise Voltage	V_n	Ta=25℃, 10Hz ≦ f ≦ 100kHz		—	110	—	μV
Ripple Rejection Ratio	R_{REF}	f=120Hz, T_j=25℃	I_{out}=100mA	53	70	—	dB
			I_{out}=300mA	53	70	—	
Drop Out Voltage	V_{drop}	I_{out}=350mA, T_j=25℃		—	2.0	—	V
Output Short-circuit Current	I_{OS}	T_j=25℃, V_{in}=35V		—	240	—	mA
Peak Output Current	$I_{o\ peak}$	T_j=25℃		—	700	—	mA
Temperature Coefficient of Output Voltage	$\delta V_{out}/\delta T_j$	I_{out}=5mA, 0℃ ≦ T_j ≦ 125℃		—	−1.1	—	mV/℃

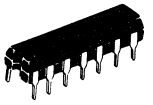
■ HA178M24P,HA178M24 ELECTRICAL CHARACTERISTICS

(V_{in}=33V, I_{out}=350mA, 0℃ ≦ T_j ≦ 125℃, C_{in}=0.33μF, C_{out}=0.1μF, unless otherwise specified.)

Item	Symbol	Test Condition		min	typ	max	Unit
Output Voltage	V_{out}	T_j=25℃		23.0	24.0	25.0	V
		27V ≦ V_{in} ≦ 38V, P_T ≦ 7.5W, 5mA ≦ I_{out} ≦ 350mA		22.8	—	25.2	
Line Regulation	$\delta V_{o\ line}$	T_j=25℃	27V ≦ V_{in} ≦ 38V, I_{out}=200mA	—	10	100	mV
			28V ≦ V_{in} ≦ 38V, I_{out}=200mA	—	5.0	50	
Load Regulation	$\delta V_{o\ load}$	T_j=25℃	5mA ≦ I_{out} ≦ 500mA	—	30	480	mV
			5mA ≦ I_{out} ≦ 200mA	—	10	240	
Quiescent Current	I_Q	T_j=25℃, I_{out}=0		—	4.6	8.0	mA
Quiescent Current Change	δI_Q	27V ≦ V_{in} ≦ 38V, I_{out}=200mA		—	—	0.8	mA
		5mA ≦ I_{out} ≦ 350mA		—	—	0.5	
Output Noise Voltage	V_n	Ta=25℃, 10Hz ≦ f ≦ 100kHz		—	170	—	μV
Ripple Rejection Ratio	R_{REF}	f=120Hz, T_j=25℃	I_{out}=100mA	50	70	—	dB
			I_{out}=300mA	50	70	—	
Drop Out Voltage	V_{drop}	I_{out}=350mA, T_j=25℃		—	2.0	—	V
Output Short-circuit Current	I_{OS}	T_j=25℃, V_{in}=35V		—	240	—	mA
Peak Output Current	$I_{o\ peak}$	T_j=25℃		—	700	—	mA
Temperature Coefficient of Output Voltage	$\delta V_{out}/\delta T_j$	I_{out}=5mA, 0℃ ≦ T_j ≦ 125℃		—	−1.2	—	mV/℃

HA1835P ●Voltage Regulator Control with Fail Detector for Digital System

The HA1835P is a monolithic voltage regulator control designed for microcomputer system. In addition to voltage regulator, it includes watch dog timer function and power on reset function.
In various microcomputer system, this IC's every function can operate with a few external parts.

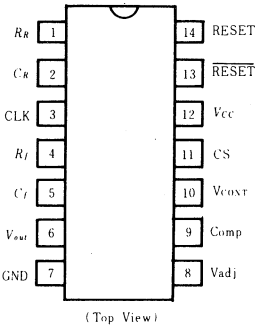


(DP-14)

■FEATURES

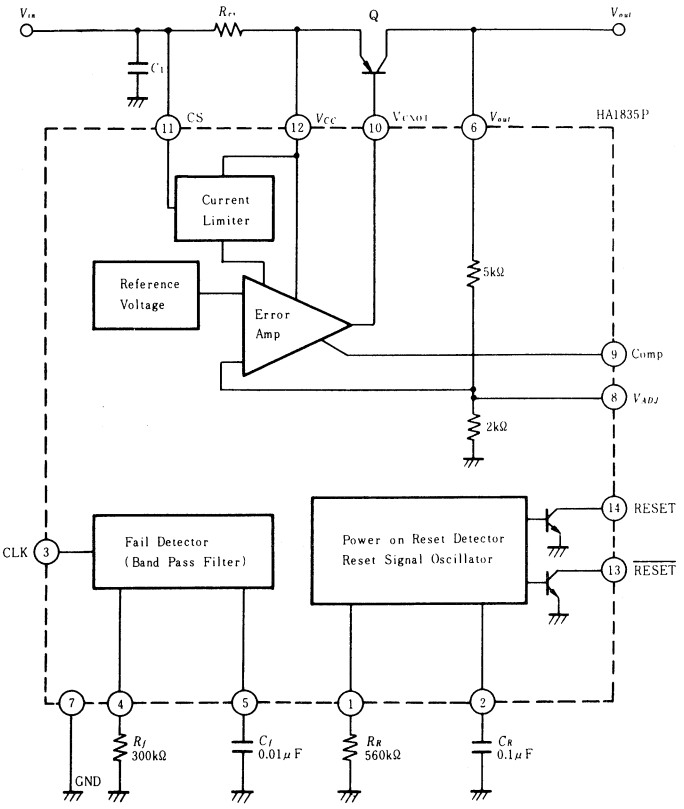
- 5V Regulated power supply control circuit
  - Voltage drop can minimize with external PNP-type transistor.
  - Internal over current protection circuit for external PNP-type transistor.
- **Watch dog timer**
  - Internal Digital band pass filter control circuit of pulse width detect type and Oscillation control circuit of constant current charge-discharge type, so Watch dog timer function controled by microcomputer's software.
  - Band pass filter characteristic and Oscillation characteristic can also set up at will with external circuit.
- **Power on automatic RESET pulse generator**

■PIN ARRANGEMENT



(Top View)

■BLOCK DIAGRAM



■ ABSOLUTE MAXIMUM RATINGS (Ta=25℃)

Item	Symbol	Rating	Unit
Supply Voltage	V_{CC}	30	V
Input Voltage	V_{CLK}	−0.3 to Vout	V
Output Voltage	V_{RESET}	17.5	V
	$V_{\overline{RESET}}$	17.5	V
Output Current	I_{RESET}	2	mA
	$I_{\overline{RESET}}$	2	mA
Control Terminal Voltage	V_{CONT}	V_{CC}	V
Control Terminal Current	I_{CONT}	20	mA
Power Dissipation	P_T*	400	mW
Operating Temperature Range	T_{opr}	−40 to +85	℃
Storage Temperature Range	T_{stg}	−50 to +125	℃
Operating Supply Voltage Range	$V_{CC(opr)}$	6 to +17.5	V
Soldering Temperature	T_{sold}	260 (T<10sec)	℃

* Value under $Ta \leqq 77$℃, In case of more than it, 8.3mV/℃ derating shall be done.

■ ELECTRICAL CHARACTERISTICS (Ta=25℃, V_{CC}= 12V, V_{out}=5V unless otherwise noted)

Item	Symbol	Conditions	min	typ	max	Unit
Supply Current	I_{CC}	V_{CC}=17.5V, with PNP Transistor	—	6.3	12	mA
● Voltage Regulator Control						
Output Voltage	$V_{out}1$	V_{CC}=6~17.5V Ta=40~+85℃, I_{out}=0.5A	4.75	5	5.25	V
	$V_{out}2$	V_{CC}=6~17.5V Ta=−40~+85℃, I_{out}=1A	4.70	5	5.30	V
Line Regulation	$V_{out\ line}$	V_{CC}=6~17.5V, I_{out}=0.5A	−50	—	+50	mV
Load Regulation	$V_{out\ load}$	V_{CC}=13.3V, I_{out}=10mA~0.5A	−100	—	+100	mV
Ripple Rejection	R_{REJ}	ei=0.5Vrms, fi=1kHz	45	75	—	dB
Limiter Operating Current	I_{CS}	R_{CS}=0.2Ω	1.0	—	2.0	A
Output Voltage Temperature Coefficient	$\delta V_{out}/\sigma T$		—	−0.6	—	mV/℃
● Watch Dog Timer						
"L"-level input Current	I_{IL}	V_{IL}=0V	−120	−60	—	μA
"L"-level input Voltage	V_{IL}		—	—	0.8	V
"H"-level input Voltage	V_{IH}		2.0	—	—	V
"H"-level input Current	I_{IH}	V_{CC}=13.3V, V_{out}=5V, V_{IH}=5V	—	1.8	3.0	mA
● Power on Reset						
"$\overline{\text{RESET}}$" Terminal Low-Voltage	$V_{OL}1$	I_{OL}=2mA	—	—	0.4	V
"$\overline{\text{RESET}}$" Terminal Leakage Current	$I_{OH}1$	V_{OH}=5V	—	—	5	μA
"$\overline{\text{RESET}}$" Terminal Leakage Current	$I_{OH}3$	V_{OH}=17.5V	—	—	30	μA

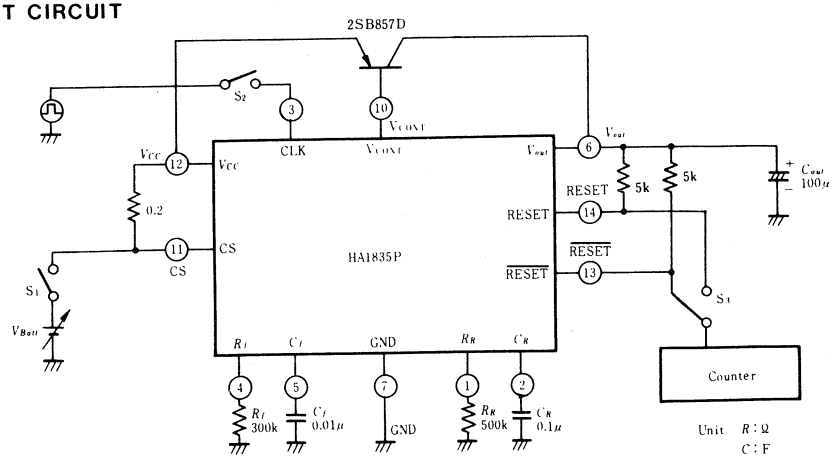
Item	Symbol	Conditions	min	typ	max	Unit
● Reset Time						
Power on Reset Time	t_{on}	R_f=300kΩ, R_R=560kΩ, C_f=0.01μF, C_R=0.1μF	80	130	200	ms
CLK off Reset Time	t_{off}		60	130	220	ms
Reset Pulse Low Level Time	t_{RL}		40	80	160	ms
Reset Pulse High Level Time	t_{RH}		50	100	200	ms

■ TERMINAL' S FUNCTION

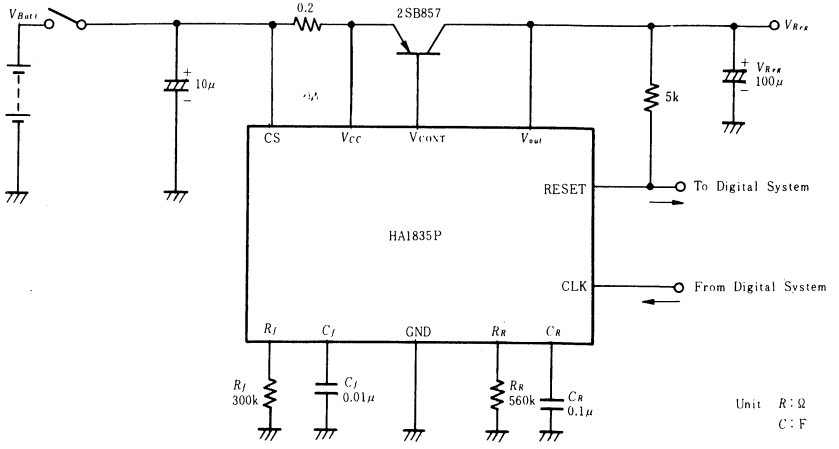
Terminal No.	Symbol	Function
1	R_R	Connect the resistor "R_R". Reset pulse width depended on "R_R".
2	C_R	Connect the capacitor "C_R". Reset pulse width depended on "C_R".
3	*CLK*	Clock pulse input terminal for watch dog timer.
4	R_f	Connect the resistor "R_f". Frequency band width of filter circuit depended on "R_f".
5	C_f	Connect the capacitor "C_f". Frequency band width of filter circuit depended on "C_f".
6	V_{out}	Connect the external PNP-type transistor's collector. This terminal supply 5V regulated voltage for internal circuit.
7	*GND*	Ground.
8	V_{adj}	Output voltage fine tuning terminal.
9	*COMP*	Phase compensate terminal. Phase compensate could obtained by the capacitor less than 100pF connected between V_{CC} treminal.
10	V_{CONT}	The externalPNP-type transistor's base control terminal.
11	C_S	The current sense resistor that protect the external PNP-type transistor connected between V_{CC} terminal.
12	V_{CC}	Supply voltage terminal. Operating supply voltage range is 6V to 17.5V.
13	$\overline{RESET}$	$\overline{\text{RESET}}$ pulse output terminal for "L" level reset type microcomputer.
14	*RESET*	RESET pulse output terminal for "H" level reset type microcomputer.

Note) RESET and $\overline{\text{RESET}}$ terminal are open collector output type.
So both terminal should connect the pull-up resistor about 5kΩ.

■ TEST CIRCUIT



APPLICATION CIRCUIT



OUTLINE OF THE FUNCTION

(1) Voltage Regulator

- Wide operational supply voltage range. 5V regulated output voltage realized wide Vcc range. (Vcc = 6 ~ 17.5V)
- The external PNP-type transistor should selected by supply current value that flows the system.
- For the realization of 5V regulated output voltage, connect the more than 100μF capacitor between Vout terminal and GND terminal.

(2) Method of Output Voltage Fine Tuning

- Output voltage fine tuning could obtained by the resistor connected from Vadj terminal to Vout terminal or GND terminal.
- The resistor connected between Vadj terminal and Vout terminal could decrease output voltage.
- The Resistor connected between Vadj terminal and GND terminal could increase output voltage.

(3) Current Limiter

- For the protection of the external transistor from over current, connect the current sense resistor between Cs terminal and Vcc terminal.
  The value of current sense resistor is given by the expression:

$$\text{Iout (limit)} \simeq \frac{0.3\text{V}}{\text{Rcs}} \quad (\text{at Ta} = 25^\circ\text{C})$$

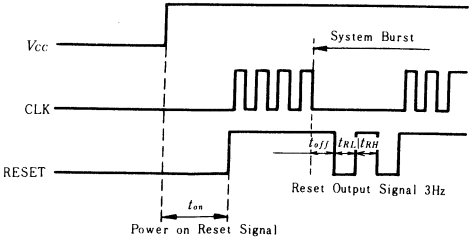
(4) Power on Reset

- The reset pulse could output for the microcomputer reset start when power on.
- Reset time for microcomputer system reset when power on could set external parts resistor "R_R" and capacitor "C_R".

(5) Watch Dog Timer (Prevent function of system run-away)

- Watch dog timer is fail-safe function. This function could reset the microcomputer system when system run-away.
- The pulse that output from microcomputer's soft ware would detected by this IC's internal band pass filter. If the pulse frequency is off the normal microcomputer's frequency band, then this IC output the reset pulse.
- The internal band pass filter's characteristics could set external parts "R_f" and "C_f".

Remarks: RESET terminal and $\overline{\text{RESET}}$ terminal are open collector output type. So both terminal should connect the pull-up resistor about 5kΩ.



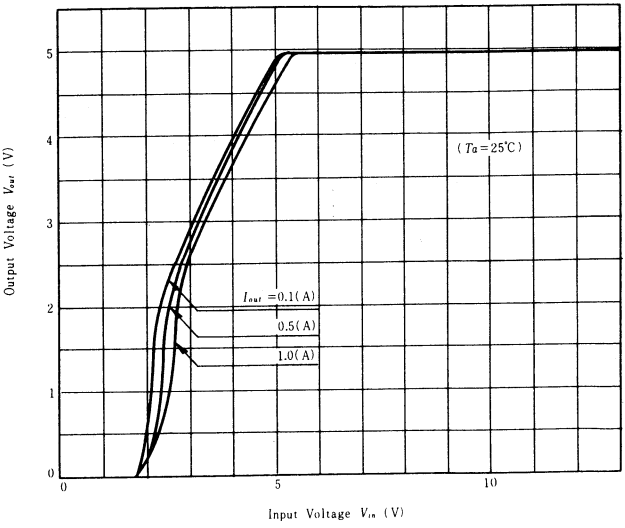


Fig. 1 Vin-Vout Characteristics

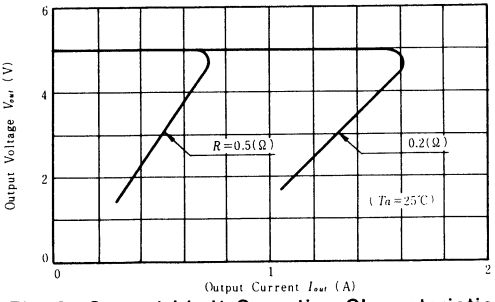


Fig. 2 Current Limit Operation Characteristics

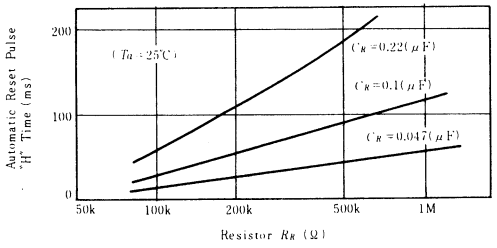


Fig. 3 R_R-Reset "H" Time Characteristics

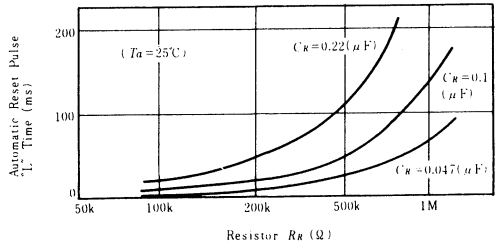


Fig. 4 R_R-Reset "L" Time Characteristics

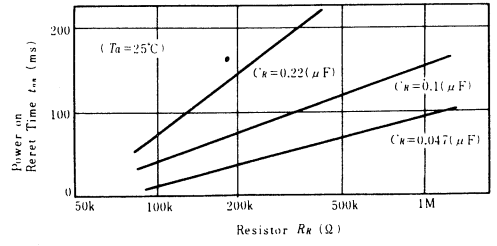


Fig. 5 R_R-ton Characteristics

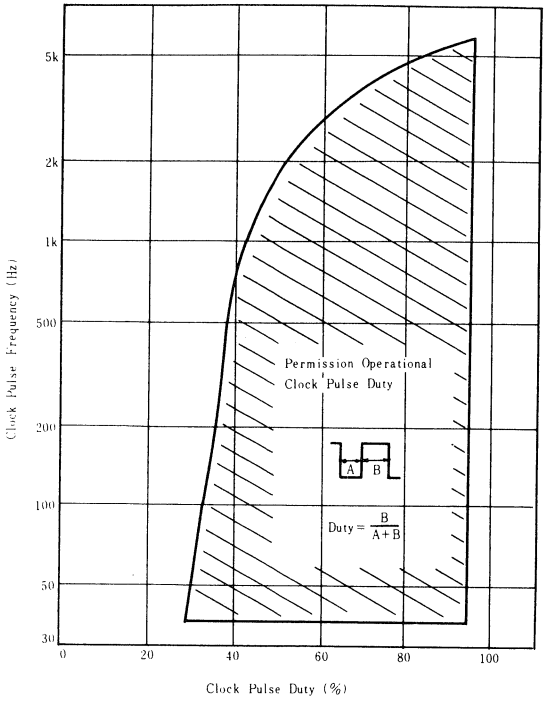


Fig.6 Permission Operational Colck Pulse Duty VS. Freqency

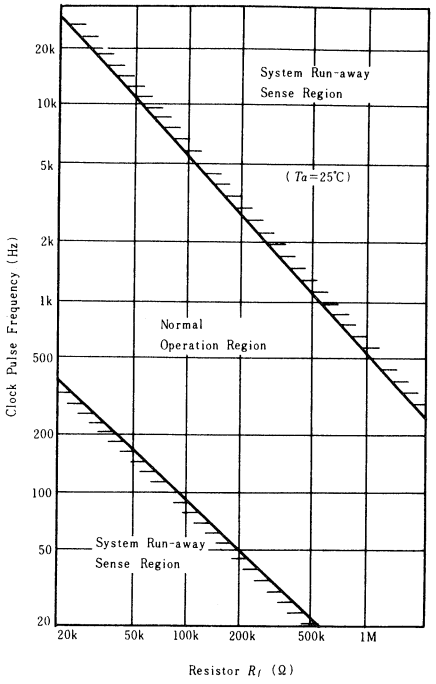


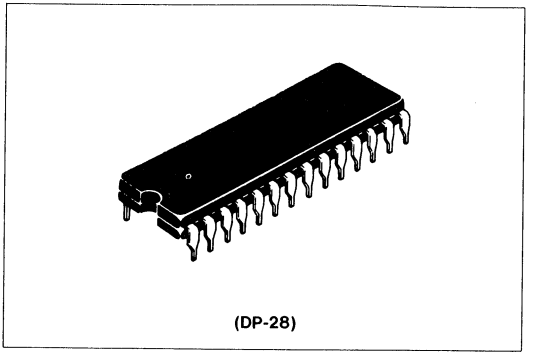
Fig.7 Clock Pulse Frequency Input RangeVS. R_f

DATA SHEETS

A/D,D/A Converters

HA16613A ●8-bit Dual Slope Type A/D Converter

HA16613A is a 8-bit Dual Slope Type A/D Converter, which is bipolar IIL structure and is designed for +5V mono power source. It is suitable for microcomputer, home appliance, industrial equipment, etc.

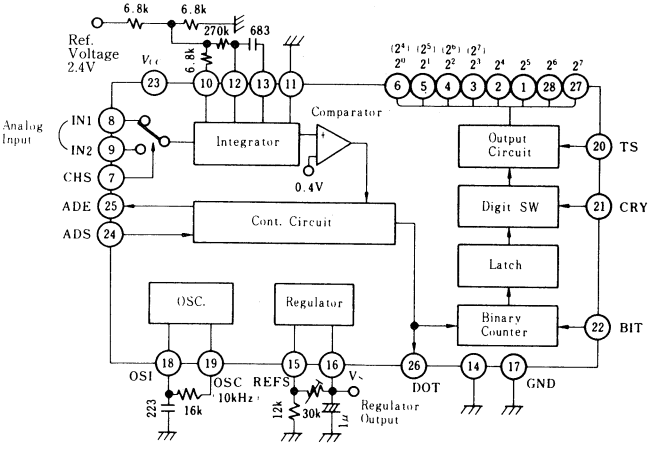


(DP-28)

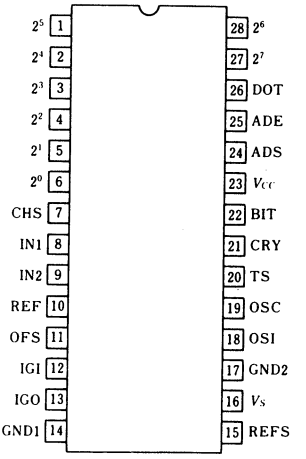
■ FEATURES

- Two-channel analog input
- Series count output and 4-bit parallel output as well as 8-bit parallel output are possible.
- Oscillator and regulator are built in.

■ BLOCK DIAGRAM



■ PIN ARRANGEMENT



(Top View)

■ ABSOLUTE MAXIMUM RATINGS (Ta=25°C)

Item	Symbol	Rating	Unit
Terminal Voltage	V_T	−0.3 to V_{CC}	V
Supply Voltage	V_{CC}	7	V
Standard Current of Power Source	I_S	−5	mA
Logic Output Current	I_O	±500	μA
Integrated Output Current	I_{INT}	±200	μA
Operating Temperature	T_{opr}	−20 to +75	°C
Storage Temperature	T_{stg}	−55 to +125	°C

■ ELECTRICAL CHARACTERISTICS (V_{CC}=5V, V_{FS}=2.0V, V_{ZS}=0.8V, V_r=2.4V constant, f_{OSC}=10kHz, Ta=25°C)

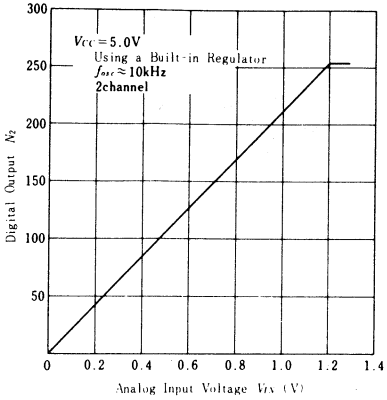
Item	Symbol	Test Condition		min	typ	max	Unit
Conversion Time		f_{osc}=200kHz		—	—	5.2	ms
Resolution				—	—	8or6	bit
Accuracy		$N_2 \geqq 16$	T_a=0~+40°C	—	0.39	—	%
			T_a=−20~+75°C	—	0.39+1step	—	
Analog Input Voltage Range	$V_{IN(opr)}$			0	—	V_{CC}-2	V
Standard Voltage Tmprature Dependency	$\Delta V_S/\Delta T_a$	Short circuit between Pin 15&16 R_L=2.4kΩ	T_a=0~+40°C	—	±50	—	ppm/°C
			T_a=−20~+75°C	—	±100	—	
Standard Voltage Spply Voltage Dependency	$\Delta V_S/\Delta V_{CC}$		V_{CC}=4~6V, $I_{o(source)}$=−500μA	−7	0	+7	mV/V
Standard Voltage Internal Resistance	$\Delta V_S/\Delta I_L$		I_L=1~5mA	—	2.4	5	Ω
Oscillation Frequency Temperature Dependency	$\Delta f_{osc}/\Delta T_a$	f_{osc}=100kHz, T_a=−20~+75°C		—	±0.3	—	%/°C
Oscillation Frequency Voltage Dependency	$\Delta f_{osc}/\Delta V_{CC}$	f_{osc}=100kHz		—	±1.8	—	%/V
Reference Voltage	V_{REF}	Short circuit between Pin 15&16, $I_{o(source)}$=−500μA		1.110	1.20	1.340	V
Analog Input Current	I_{IN}	V_{IN}=0V		−0.2	—	—	μA
Logic Output Current*	$I_{o(source)}$	V_{OH}=V_{CC}/2		—	−100	−50	μA
	$I_{o(sink)}$	V_{OL}=0.4V		500	—	—	μA
Logic Input Current*	I_{IL}	V_{IN}=0V		−20	—	—	μA
	I_{IH}	V_{IN}=V_{CC}		—	—	20	μA
Input Voltage**	V_{IH}			1.0	—	—	V
	V_{IL}			—	—	0.4	V
Operating Supply Voltage Range	$V_{cc(opr)}$	T_a=−20~+75°C		4	5	V_{CC} max	V
Maximum Operating Frequency	$f_{osc(opr)}$			200	—	—	kHz
Power Dissipation	P_T	V_{CC}=5V		—	30	60	mW
Three-state Output Leak Current	I_{OL}	V_o=0~V_{CC}		−5	—	5	μA

Note) * : Applied to 2^0~2^7, ADE, & DOT.
** : Applied to ADS, TS, CRY, BIT, & CHS.

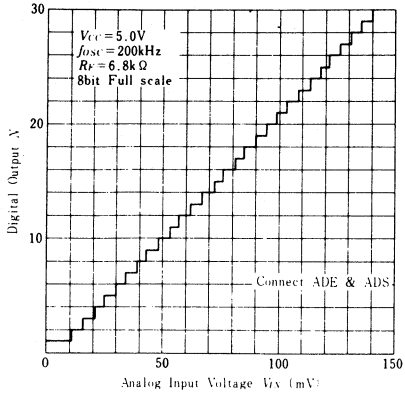
■ TERMINAL DESCRIPTION

Terminal	Description
IN1 · IN2	Analog input voltage is applied. (IN 1 ····· 1 channel / IN 2 ····· 2 channel)
CHS	For switching the analog input terminal. (0 : 1 channel / 1 : 2 channel)
ADE	A/D Conversion end signal is applied. (0 : End / 1 : under conversion)
ADS	A/D Conversion start signal is applied. When ADE=1, A/D conversion starts at negative edge of ADS input signal.
DOT	A/D converted pulse is directly outputted between ADS and ADE. (3 state is impossible.)
BIT	For switching 6-bit or 8-bit full scale. (0 : 8 bit / 1 : 6 bit)
CRY	Digit switching at 4-bit parallel transfer. (0 : 4 bit lower + 4 bit upper / 1 : 4 bit upper + 4 bit upper)
TS	Make 8-bit output terminal to be high impedance. (0 : Output / 1 : High Impedance)
$2^0 \sim 2^7$	Binary output terminal During A/D conversion, the previous data is available.
OSI, OSC	Oscillator external terminal. When a clock is applied from external part, a resistor of some hundred k Ω shall be added to OSI.
REFS · Vs	Regulator terminal
REF	Reference voltage for integrator is applied.
IGI · IGO	Input & output terminal of integrator
OFS	Generally connected to GND. Terminal for offset adjustment, in case of small digital output through A/D conversion.

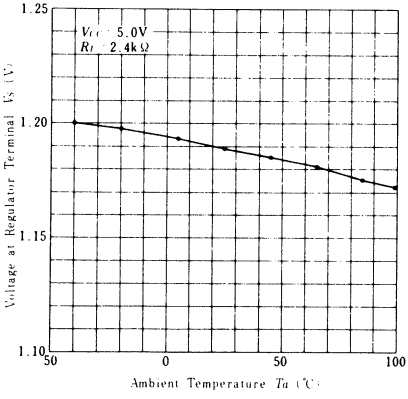
LINEARITY CHARACTERISTICS



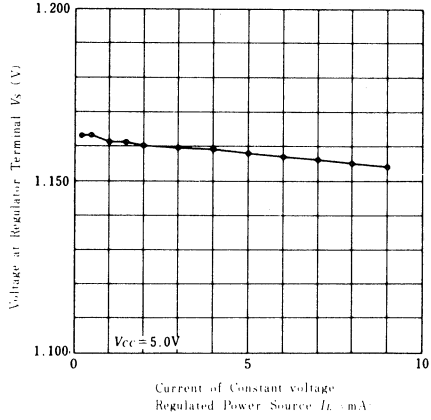
LINEARITY CHARACTERISTICS (LEADING EDGE)



CONSTANT VOLTAGE-TEMPERATURE DEPENDENCY



CONSTANT-VOLTAGE INTERNAL RESISTANCE



■ HINTS FOR USE

1. In the equation on the preceding page (Note 1), if R_3 = 0, Vzs = 0V (possible to convert from input of 0V). However, the linearity around V_{IN} = 0V will worsen.
   It is recommended to use under condition Vzs is more than 0.1V.
2. After Three State is applied, the time required for changing from digital output to high impedance and vice versa is 4 ~ 8μs. The quantity of current flowing through digital output terminal is equal to that of a LSTTL. Therefore, when connecting digital output to a busline and reading it into a microprocessor in a high speed, a three-state buffer is required for it.
3. If an analog input changes during A/D conversion, there may occur some troubles in the output data. In this case, Sample & Hold is necessary.
4. Timing from CHS (Channel Switch) to ADS (A/D Conversion Start) is more than or equal to 0 seconds. It may be accepted that CHS and ADS are performed at the same time.

■ NOTE

When input analog voltage of ZS or less, input analog voltage of ZS or more and A/D conversion is done, after the maximum conversion time perform A/D conversion.

HA17008R Series

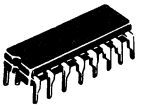
●8-bit Multiplying Digital-to-Analog Converter

HA17008R is a 8-bit monolithic D/A Converter, with a reference current amplifier, a ladder resistor of R-2R and eight high speed current switches built in. By establishing a reference current and resistance, it is possible to change the maximum output current according to the applications. And it is pin-for-pin compatible with DAC08 and its power dissipation is small and realizes high settling speed.

The reference current is divided into current value of each bit by the ladder resistor of R-2R and maximum output current will be 255/256 of the reference current. For example, the maximum output current gained from reference input current of 2.0mA will be 1.992mA.

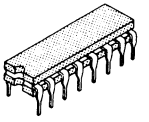
HA17008R provides a wide scope of application including CRT display, control of step motor, programmable power source, audio instrument, attenuator, etc.

HA17008RP



(DP-16)

HA17008RG

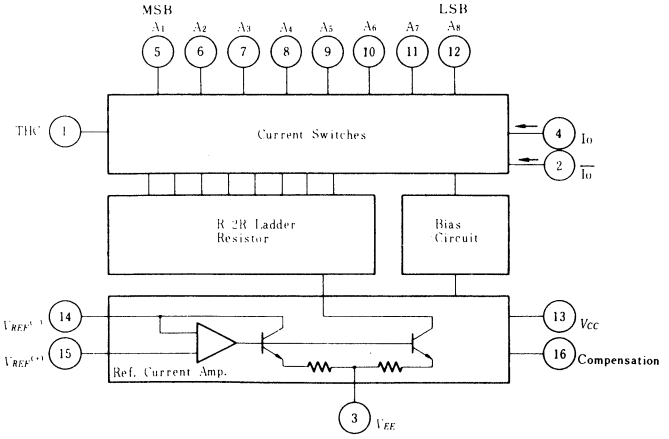


(DG-16)

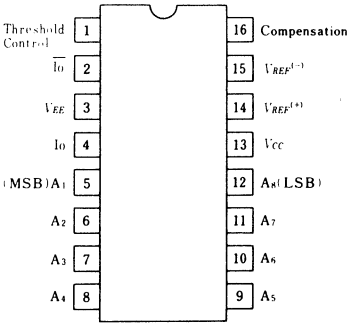
■ FEATURES

- A linearity of ±0.19% (±1/2 LSB) is guaranteed.
- Since the settling time is short, 85ns typ, and fast conversion is possible.
- Low power dissipation, 135mW typ.
- Compatible with TTL, CMOS logic.
- Reference Supply Voltage is;
  V_{CC} = +15V, V_{EE} = −15V.
- Output Voltage Range is wide; −10V to +18V.

■ BLOCK DIAGRAM



■ PIN ARRANGEMENT



(Top View)

HITACHI

■ ABSOLUTE MAXIMUM RATINGS (Ta=25°C)

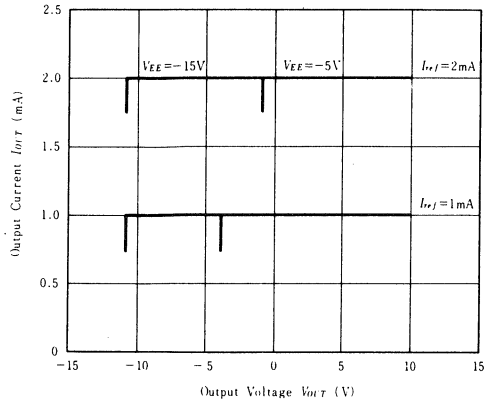
Item	Symbol	Rating	Unit
Supply Voltage	V_{CC}	+18	V
	V_{EE}	−18	V
Digtal Input Voltage	V_5 V_{12}	V_{EE} to V_{EE}+36V	V
Reference Current	I_{14}	5	mA
Input Voltage Range of Reference Amplifier	V_{REF}	V_{CC}, V_{EE}	V
Power Dissipation	P_T	500	mW
Operating Temperature	T_{opr}	−20 to +75	°C
Storage Temperature	T_{stg}*	−55 to +125	°C

* : In HA17008RG; −65 to +150°C

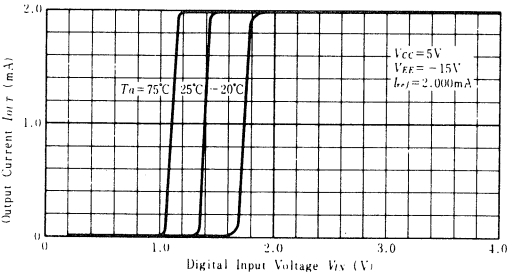
■ ELECTRICAL CHARACTERISTICS (V_{CC}=15V, V_{EE}=−15V, I_{ref}=2mA, V_{THC}=0V, Ta=25°C)

Item	Symbol	Test Condition	min	typ	max	Unit
Relative Error	E_R		—	—	±0.19	%FS
Settling Time(±1/2LSB)	t_s	All Bits OFF to ON	—	85	150	ns
Propagation Delay Time	t_{PHL}, t_{PLH}		—	35	60	ns
Maximum Output Current Drift	T_{CIO}		—	±10	±50	ppm/°C
Digital Input Level	V_{IH}		2.0	—	—	V
	V_{IL}		—	—	0.8	V
Digital Input Current (MSB)	I_{IH}	V_{IH}=5.0V	—	0.002	10	μA
	I_{IL}	V_{IL}=0.8V	−10	−2.0	—	μA
Reference Bias Current	I_{15}		−3.0	−1.0		μA
Output Current Range	I_{OR}	V_{EE}=−5.0V	0	2.0	2.1	mA
		V_{EE}=−8.0 to −18V	0	2.0	4.2	
Output Current	I_o	V_{ref}=10.000V R_{14}, R_{15}=5.000kΩ	1.94	1.99	2.04	mA
	$I_{o\,min}$	All Bits Low	—	0	2.0	μA
Output Voltage Range	V_o	$\Delta F_S \leqq ½ LSB$	−10		+18	V
Reference Current Slew Rate	SRI_{ref}		4.0	8.0		mA/μs
Supply Current	I_{CC}	V_{CC}=+5V I_{REF}=1mA	—	1.8	3.8	mA
	I_{EE}	V_{EE}=−5V	−5.8	−3.7		
	I_{CC}	V_{CC}=+5V I_{REF}=2mA	—	1.9	3.8	
	I_{EE}	V_{EE}=−15V	−7.8	−5.8		
	I_{CC}	V_{CC}=+15V I_{REF}=2mA	—	2.1	3.8	
	I_{EE}	V_{EE}=−15V	−7.8	−5.9		
Supply Voltage	V_{CC}	I_{REF}=1mA	4.5	15	18	V
	V_{EE}	I_{REF}=1mA	18	15	−4.5	V
Power Dissipation	P_{T1}	V_{CC}=+5V I_{REF}=1mA V_{EE}=−5V	—	33	48	mW
	P_{T2}	V_{CC}=+5V I_{REF}=2mA V_{EE}=−15V		108	136	
	P_{T3}	V_{CC}=+15V I_{REF}=2mA V_{EE}=−15V	—	135	174	
Full Scale Current Difference	I_{FSS}	I_{FS1} I_{FS2}	−8.0	±1.0	+8.0	μA
Digital Input Scale	V_{IS}		−10	—	+18	V
Threshold Control Voltage	V_{THR}	$V_{THR} \fallingdotseq V_{THC}$+1.3	−10	0	13.5	V
Digital Input Threshold Voltage	V_{THL}		—	V_{THR} +1.3	—	V
Power Supply Current	P_{SS} I_{FS}+	V_{CC}=4.5 to 18V, I_{REF}=1mA	−100	—	100	ppmFs/%V
	P_{SS} I_{FS}−	V_{EE}=−4.5 to −18V, I_{REF}=1mA	−100	—	100	

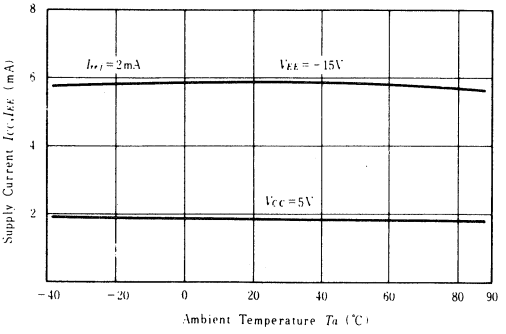
OUTPUT CURRENT VS. OUTPUT VOLTAGE



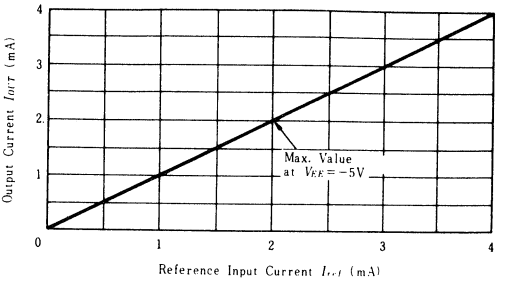
OUTPUT CURRENT VS. DIGITAL INPUT VOLTAGE



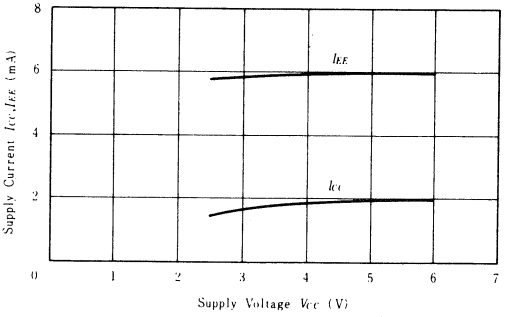
SUPPLY CURRENT VS. AMBIENT TEMPERATURE



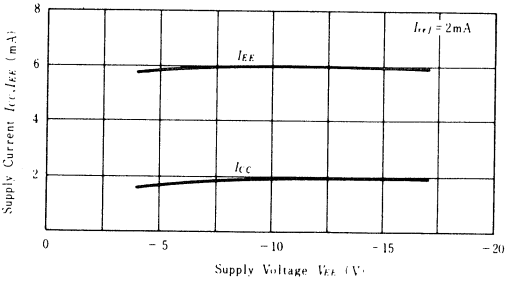
OUTPUT CURRENT VS. REFERENCE INPUT CURRENT



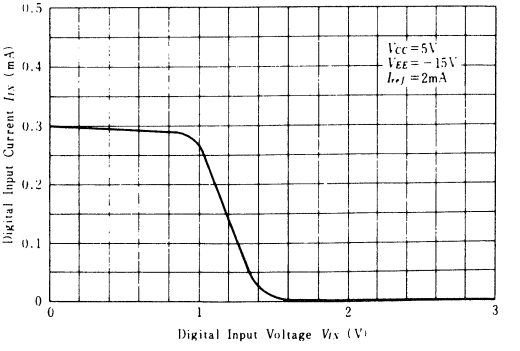
SUPPLY CURRENT VS. SUPPLY VOLTAGE (1)



SUPPLY CURRENT VS. SUPPLY VOLTAGE (2)



DIGITAL INPUT CURRENT VS. DIGITAL INPUT VOLTAGE



■ EXPLANATION OF FUNCTIONS

● Reference Differential Amplifier and Phase Compensation

Reference Amplifier is for converting the reference voltage added to pin 14 from voltage to current. And its converted current is supplied to each bit by current mirror and ladder resistor. Further, use pin 14 with positive or negative porality according to the current flown to it. The reference power source supplies all currents to pin 14. (Refer to Fig. 1)

To input a positive pulse to the reference voltage, as multiplying mode, R_{15} is capable of being connected to the lowest electric potential of input voltage which is equivalent to the negative voltage.

Without R_{15}, the accuracy and the temperature drift is little influenced. To keep the phase margin proper, the capacitance for phase compensation shall be increased with accordance to the increase of R_{14}. For example, when R_{14} is 1kΩ, 2.5kΩ, 5kΩ, the lowest capacitance is 15pF, 37pF, and 75pF respectively. The capacitor shall be connected to V_{EE} or GND. When a high impedance is required, connect R_{14} to GND, and R_{15}, to the negative reference voltage. (Refer to Fig. 2) In this case, capacitor for phase compensation must be connected between V_{EE} and pin 16. In case of using a DC reference voltage, insert by-pass capacitor. It is not recommended to use logic power source of 5V. In case of using a high stable 5V power source for logic control, connect the resistor to the reference power source, and ground 0.1μF capacitance from the connecting point.

As for a reference voltage of 5V or more, ground a clump diode from pin 14.

When pin 14 is controlled by a high impedance such as a power source, phase compensation can not be performed in a way described above. Amplifier shall be fully phase-compensated in all frequency bands.

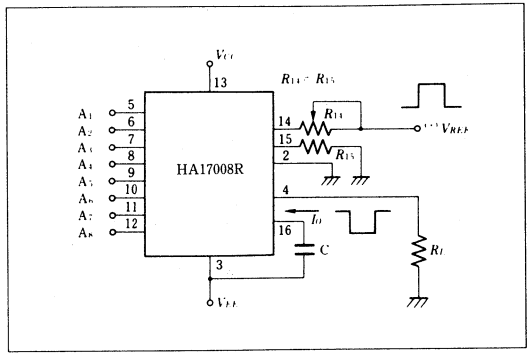


Fig. 1 Positive Reference Voltage

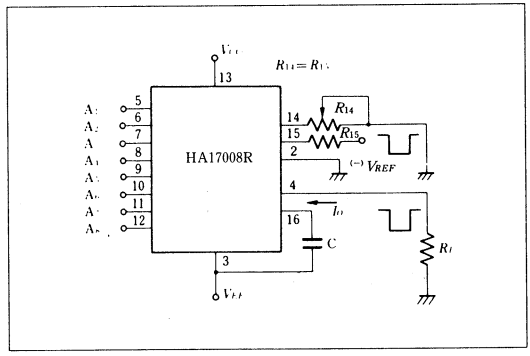


Fig. 2 Negative Reference Voltage

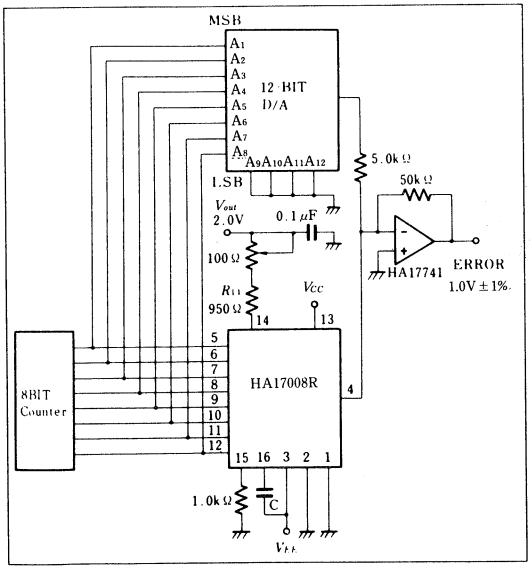


Fig. 3 Circuit to Measure Relative Accuracy

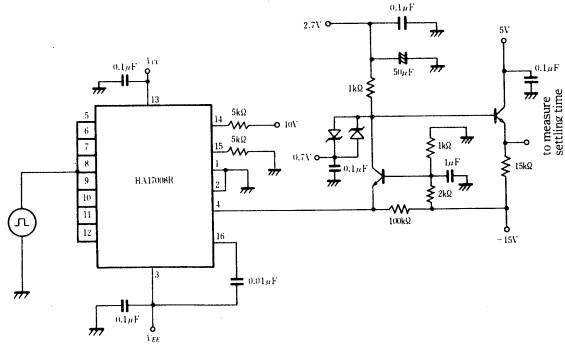
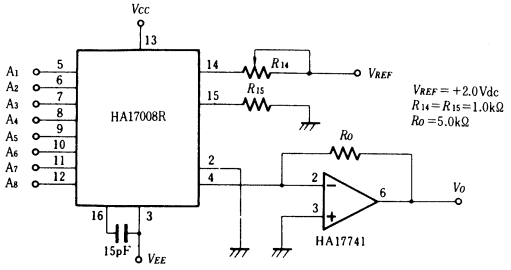


Fig. 4 Circuit to Measure Settling Time

■ AN EXAMPLE OF OPERATION

- Current – Voltage Conversion by an Operational Amplifier



The theoretical output is;

$$V_O = \frac{V_{REF}}{R_{14}}(R_O)\left(\frac{A_1}{2}+\frac{A_2}{4}+\frac{A_3}{8}+\frac{A_4}{16}+\frac{A_5}{32}+\frac{A_6}{64}+\frac{A_7}{128}+\frac{A_8}{256}\right)$$

Once values of V_{REF}, R_{14} and R_0 is determined, the output voltage will be 9.961V under the condition of all bits High.

$$V_O = \frac{2V}{1k}(5k)\left(\frac{1}{2}+\frac{1}{4}+\frac{1}{8}+\frac{1}{16}+\frac{1}{32}+\frac{1}{64}+\frac{1}{128}+\frac{1}{256}\right)$$

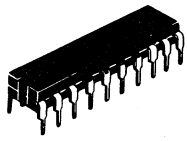
HA17012 Series ●12-bit Multiplying Digital-to-Analog Converter

HA17012 is a monolithic high speed multiplying D/A converter which provides 12-bit resultion and current output. It is divided into two groups according to the accuracy of linearity and the differential error.

■ FEATURES

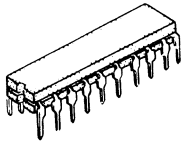
- With differential current attraction terminals (I_0, T_0)
- 4mA full scale output is gained with 1mA reference input current.
- The settling time is short, 250ns (typ), and fast conversion is possible.
- Possible to connect a digital input to TTL and CMOS directly.
- Pin compatible with Am6012 of AMD Ltd.

HA17012P



(DP-20N)

HA17012G

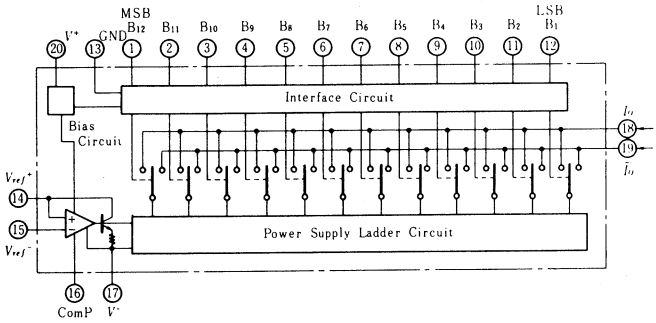


(DG-20NA)

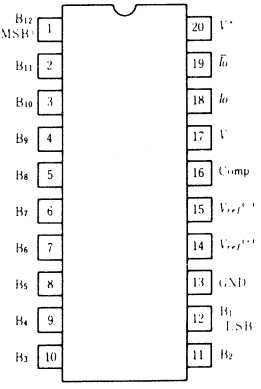
■ ACCURACY

Type No.	Linearity Accuracy		Differential Accuracy	
	Bit	LSB	Bit	LSB
HA17012B	11	±2	12	±1
HA17012C	10	±4	11	+2, −1

■ BLOCK DIAGRAM



■ PIN ARRANGEMENT



(Top View)

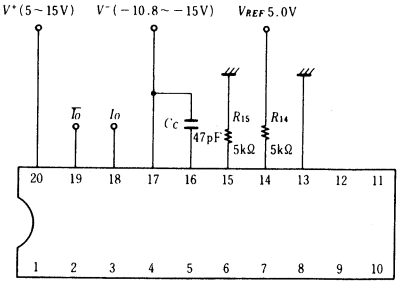
■ ABSOLUTE MAXIMUM RATINGS (Ta=250°C)

Item	Symbol	Rating	Unit
Supply Voltage	V^-	±18	V
Logic Input Voltage	V_{LIN}	−5 to +15	V
Analog Output Voltage	V_{OUT}	−8 to +12	V
Reference Input Voltage	V_{ref}	V^- to V^+	V
Reference Input Current	I_{ref}	1.25	mA
Differential Reference Input Voltage Range	$V_{IN(dif)}$	±18	V
Operating Temperature	T_{opr}	−20 to +75	°C
Storage Temperature *	T_{stg}	−65 to +150	°C

*In HA17012P; −55 to +125°C

■ RECOMMENDED OPERATING CONDITIONS

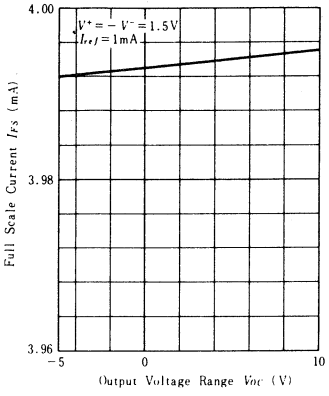
Item	Symbol	Recommended Value	Unit
Supply Voltage	V^+	5 to 15	V
	V^-	−15 to −10.8	V
Logic Input Voltage	V_I	0 to V^+	V
Reference Voltage	V_{REF}	5.0	V
Reference Current	I_{ref}	1.0	mA
Reference Input Resistance	R_{14}, R_{15}	5.0	kΩ
Phase Compen-sation Capacitance	C_C	47	pF
Output Voltage	V_{out}	0	V



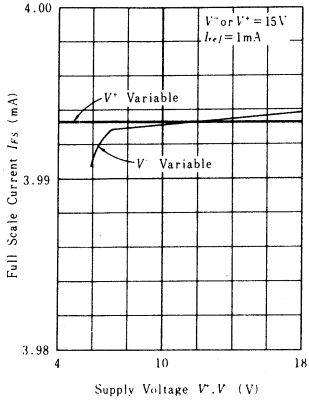
■ ELECTRICAL CHARACTERISTICS ($V^+ = -V^- = 15V$, $I_{ref} = 1mA$, $Ta = 25°C$)

Item	Symbol	Test Condition	HA17012B			HA17012C			Unit
			min	typ	max	min	typ	max	
Resolution			12	12	12	12	12	12	bits
Differential Error	DNL	$V_{out} = 0V$	−0.025	—	+0.025	−0.025	—	+0.05	%FS
Non Linearity	NL	$V_{out} = 0V$	−0.05	—	+0.05	−0.1	—	+0.1	%FS
Full Scale Current	I_{FS}	$V_{ref} = 15V$, $R_{14} = R_{15} = 15k\Omega$	3.935	3.999	4.063	3.871	3.999	4.127	mA
Full Scale Temperature Dependency	$\Delta I_{FS}/I_{FS}$		—	±10	—	—	±20	—	ppm/°C
Output Voltage Range	V_{oc}		−5	—	+10	−5	—	+10	V
Full Scale Subtracted Current	I_{FSS}	$I_{FS} - \overline{I_{FS}}$	−2.0	±0.4	+2.0	−4.0	±0.8	+4.0	μA
Offset Current	I_{ZS}		—	—	0.1	—	—	0.4	μA
Settling Time	t_s	to $\pm\frac{LSB}{2}$ All bits ON,OFF	—	250	—	—	250	—	ns
Delay Time	t_{PLH}, t_{PHL}	50% to 50%	—	25	—	—	25	—	ns
Output Capacitance	C_{out}		—	20	—	—	20	—	pF
Logic Input Voltage	V_{IL}		—	—	0.8	—	—	0.8	V
	V_{IH}		2.0	—	—	2.0	—	—	V
Logic Input Current	I_{IN}	$-5V \leqq V_{IN} \leqq +15V$	−60	—	+20	−60	—	+20	μA
Ligic Input Voltage Range	V_{IS}		−5	—	+15	−5	—	+15	V
Reference Current Range	I_{REF}		0.2	1.0	1.1	0.2	1.0	1.1	mA
Bias Current at Reference Terminal	I_{IS}		−3	—	0	−3	—	0	μA
Supply Voltage Dependency	$PSS \cdot I_{FS}^+$	$13.5V \leqq V^+ \leqq 16.5V$	−10	—	+10	−10	—	+10	ppmFS/%V
	$PSS \cdot I_{FS}^-$	$-16.5 \leqq V^- \leqq -13.5V$	−10	—	+10	−10	—	+10	ppmFS/%V
Supply Voltage Range	V^+	$V_{out} = 0V$	4.5	—	18	4.5	—	18	V
	V^-		−18	—	−10.8	−18	—	−10.8	V
Supply Current	I^+	$V^+ = 15V$	—	5.2	8.5	—	5.2	8.5	mA
	I^-	$V^- = -15V$	−23	−17.2	—	−23	−17.2	—	mA
Power Dissipation	P_T	$V^+ = 15V$, $V^- = -15V$	—	336	473	—	336	473	mW

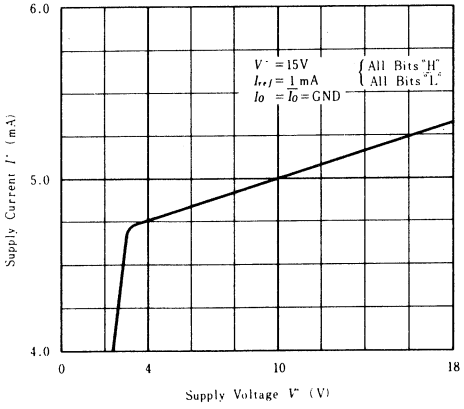
FULLSCALE CURRENT VS. OUTPUT VOLTAGE RANGE



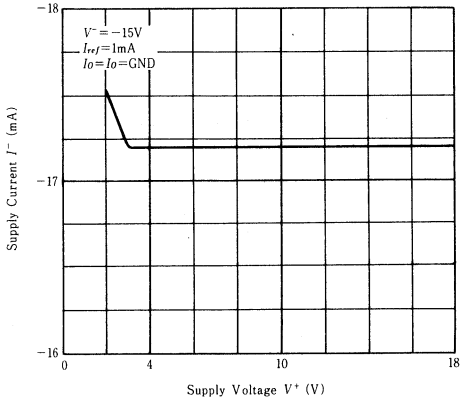
FULLSCALE CURRENT VS. SUPPLY VOLTAGE



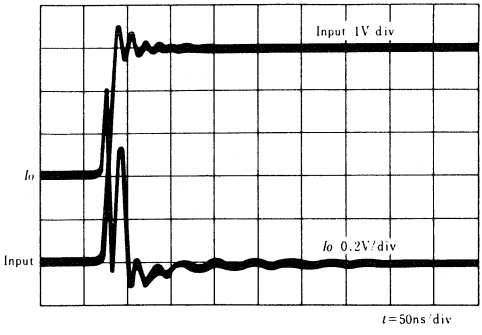
SUPPLY CURRENT VS. SUPPLY VOLTAGE(1)

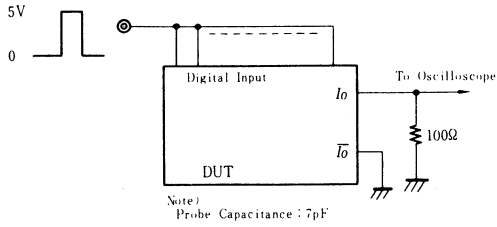


SUPPLY CURRENT VS. SUPPLY VOLTAGE(2)



SETTLING WAVEFORM(ALL BITS ON-OFF)



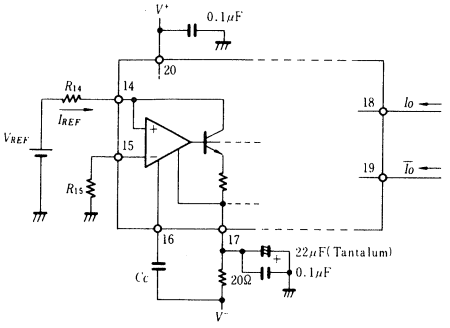


Test Circuit

■ APPLICATION NOTES

1. Method to Apply a Reference Input

● Positive Reference Voltage



The full scale output current ($I_o + \overline{I_o}$) is four times as large as the reference input current (I_{REF}) on account of the internal circuit.

$$I_{FS} = I_o + \overline{I_o} \fallingdotseq 4I_{REF}$$

V_{REF} is converted to the reference input current (I_{REF}) by R_{14}.

$$I_{REF} \fallingdotseq \frac{V_{REF}}{R_{14}}$$

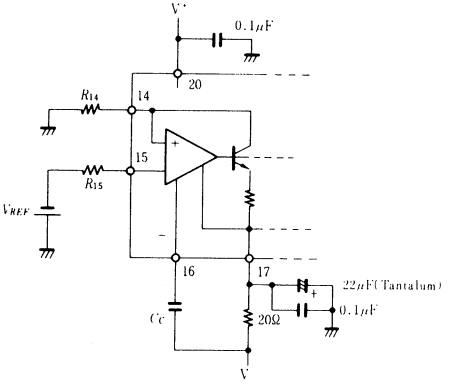
To erase the input bias current error of the input operational amplifier, $R_{14} = R_{15}$.
The phase correction capacitance C_C is 0.01μF generally and the minimum value can be found by;

$$C_C = 5 \times R_{14}\ (k\Omega)\ (pF)$$

For example, when R_{14} 0 5kΩ, the minimum value of C_C is;

$$C_C = 5 \times 5 = 25\ (pF)$$

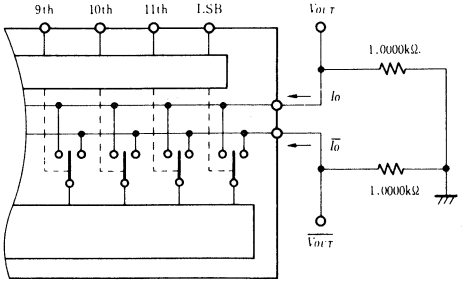
● Negative Reference Voltage



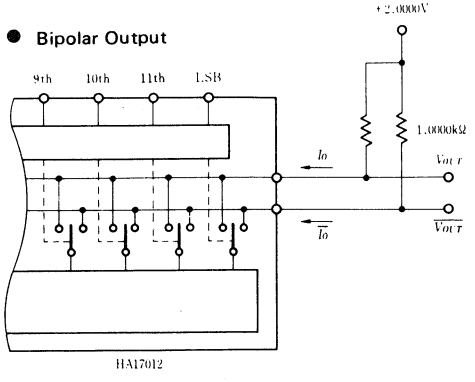
2. Method to Connect Output Circuit

(1) Resistor

● Unipolar Negative Output Voltage



● Bipolar Output



I_{REF} = 1.0000mA

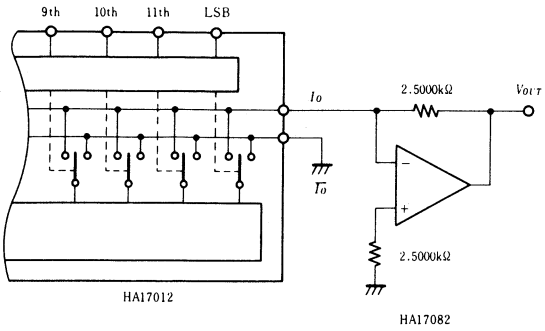
Input Code MSB LSB	I_o (mA)	$\overline{I_o}$ (mA)	V_{OUT} (V)	$\overline{V_{OUT}}$ (V)
1 1 1 1 1 1 1 1 1 1 1 1	3.999	0.000	−3.999	0.000
1 1 1 1 1 1 1 1 1 1 1 0	3.998	0.001	−3.998	−0.001
1 0 0 0 0 0 0 0 0 0 0 0	2.000	1.999	−2.000	−1.999
0 0 0 0 0 0 0 0 0 0 0 1	0.001	3.998	−0.001	−3.998
0 0 0 0 0 0 0 0 0 0 0 0	0.000	3.999	0.000	−3.999

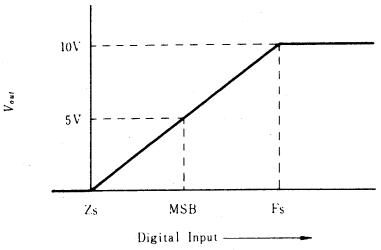
I_{REF} = 1.0000mA

Input Code MSB LSB	I_o (mA)	$\overline{I_o}$ (mA)	V_{OUT} (V)	$\overline{V_{OUT}}$ (V)
1 1 1 1 1 1 1 1 1 1 1 1	3.999	0.000	−1.999	+2.000
1 1 1 1 1 1 1 1 1 1 1 0	3.998	0.001	−1.998	+1.999
1 0 0 0 0 0 0 0 0 0 0 1	2.001	1.998	−0.001	+0.002
1 0 0 0 0 0 0 0 0 0 0 0	2.000	1.999	0.000	+0.001
0 1 1 1 1 1 1 1 1 1 1 1	1.999	2.000	+0.001	0.000
0 0 0 0 0 0 0 0 0 0 0 1	0.001	3.998	+1.999	−1.998
0 0 0 0 0 0 0 0 0 0 0 0	0.000	3.999	+2.000	−1.999

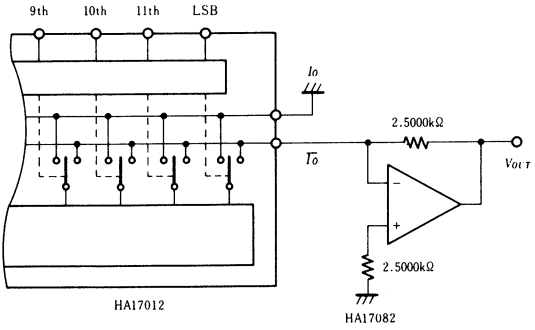
(2) Method to Connect Output Buffer and Amplifier

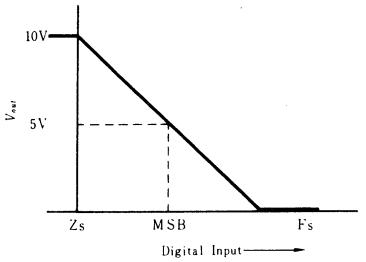
● Unipolar Positive Output Voltage (Straight Binary)



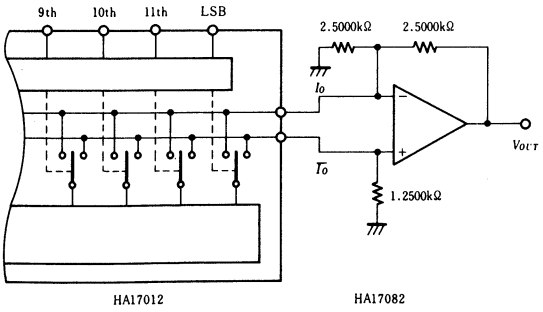


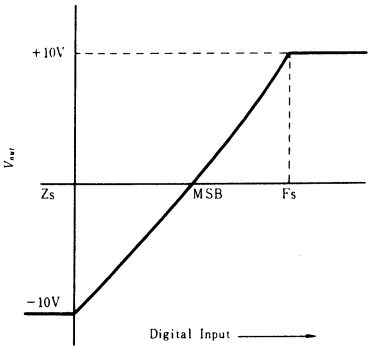
● Unipolar Positive Output Voltage (Complementary Binary)





● Symmetrical Offset Output Voltage





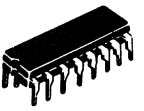
HA17408 Series ●8-bit Multiplying Digital-to-Analog Converter

HA17408 is a 8-bit monolithic D/A converter, with reference current amplifier and a ladder resistor of R-2R, and eight high speed current switches built in. By establishing a reference current and a reference resistor, it is possible to change the maximum output current according to the applications. And it is compatible with MC1508/1408, AM1408, and its power dissipation is small and realizes high settling speed.

Reference current is divided into current value each bit by the ladder resistor or R-2R and maximum output current will be 255/256 of the reference current. For example, the maximum output current gained from reference input current of 2.0mA will be 1.992mA.

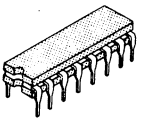
HA17408 provides a wide scope of application including CRT display, control of step motor, programmable power source, audio instrument, attenuator, etc.

HA17408P



(DP-16)

HA17408G

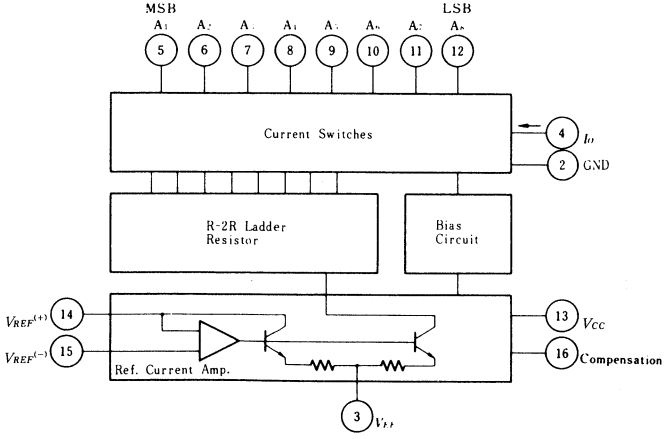


(DG-16)

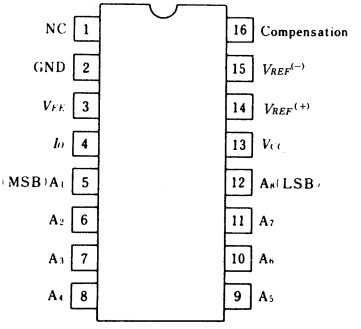
■ FEATURES

- A linearity of ±0.19% (±1/2 LSB) is guaranteed.
- Since settling time is short, 250ns typ, and fast conversion is possible.
- Low Power dissipation, 157mW typ.
- Compatible with TTL, CMOS logic.
- Reference Supply Voltage is;
  V_{CC} = +5.0V, V_{EE} = −5.0V, −15.0V
- Output Voltage Range is wide; −5.0 to +0.5V.

■ BLOCK DIAGRAM



■ PIN ARRANGEMENT



(Top View)

■ ABSOLUTE MAXIMUM RATINGS (Ta=25°C)

Item	Symbol	Rating	Unit
Supply Voltage	V_{CC}	5.5	V
	V_{EE}	−16.5	V
Digital Input Voltage	V_5 to V_{12}	0 to +5.5	V
Output Voltage	V_o	0.5, −5.2	V
Reference Current	I_{14}	5.0	mA
Input Voltage Range of Reference Amplifier	V_{REF}	V_{CC}, V_{EE}	V
Power Dissipation	P_T	625	mW
Operating Temperature	T_{opr}	−20 to +75	°C
Storage Temperature	T_{stg} *	−55 to +125	°C

* : In HA17408G; −65 to +150°C

■ ELECTRICAL CHARACTERISTICS (V_{CC}=5.0V, V_{EE}=−15V, I_{ref}=2mA, Ta=25°C)

Item	Symbol	Test Conditions		min	typ	max	Unit
Relative Error	E_R			−	−	±0.19	%FS
Settling Time(±1/2LSB)	t_s	All bits; OFF to ON		−	250	−	ns
Propagation Delay Time	t_{PLH}, t_{PHL}			−	30	100	ns
Maximum Output Current Drift	T_{CIO}			−	±20	−	pp/°C
Digital Input Level	V_{IH}			2.0	−	−	V
	V_{IL}			−	−	0.8	V
Digital Input Current(MSB)	I_{IH}	V_{IH}=5.0V		−	0	0.04	mA
	I_{IL}	V_{IL}=0.8V		−0.8	−0.002	−	mA
Reference Input Bias Current	I_{15}			−3.0	−1.0	−	μA
Output Current Range	I_{OR}	V_{EE}=−5.0V		0	2.0	2.1	mA
		V_{EE}=−7.0 to −15V		0	2.0	4.2	
Output Current	I_O	V_{ref}=2.000V R_{14}=1000Ω		1.9	1.99	2.1	mA
	$I_{O(min)}$	All Bits Low		−	0	4.0	μA
Output Voltage Range	V_O	V_{EE}=−5V		−0.6	−	+0.5	V
		V_{EE}<−10V		−5.0	−	+0.5	
Reference Current Slew Rate	STI_{ref}			−	4.0	−	mA/μs
Supply Current	I_{CC}			−	1.9	14	mA
	I_{EE}			−13	−5.8	−	mA
Supply Voltage	V_{CC}			4.5	5.0	5.5	V
	V_{EE}			−16.5	−15	−4.5	V
Power Dissipation	P_I	All Bits Low	V_{EE}=−5.0V	−	34	136	mW
			V_{EE}=−15V	−	97	265	
		All Bits High	V_{EE}=−5.0V	−	34	−	
			V_{EE}=−15V	−	97	−	

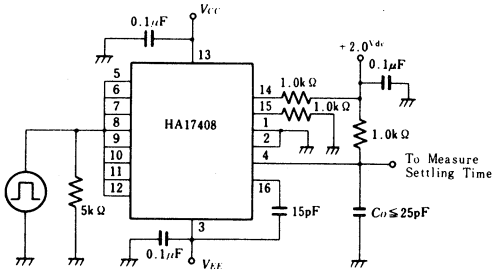


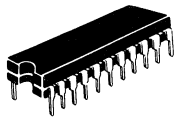
Fig. 1 Circuit to Measure Settling Time

HA19202, HA19203MP ●4-bit A/D Converter

With development of the digital electronic technique, A/D converters have been playing an important role of interfacing analog-to-digital conversion. Requirement for the high-speed, high-performance and low cost A/D converters is increasing especially in color TV applications which need analog-to-digital conversion for video signal processing.

The Hitachi A/D Converter HA19202 has a 4-bit parallel sampling system. The HA19202 is useful for video signal processing.

HA19202



(DP-22)

HA19203MP

(MP-18)

■ FUNCTIONS

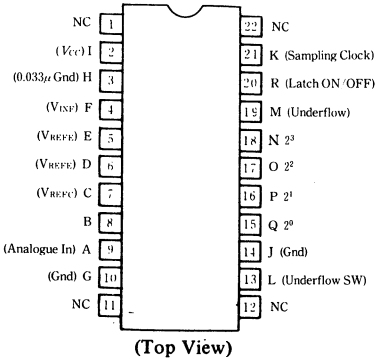
- 4-bit Comparators
- Gray Code Converter
- ECL-to-TTL Converter
- Latch Circuits
- Gray-to-binary Code Converter
- Sampling Clock Pulse Shaper
- Underflow Output Switch

■ FEATURES

- Conversion Time
  The sampling rate is 10 million samples/sec (max).
- Output Stages
  Open-collector type, TTL compatible
- Expansion to 5-bit A/D Converter
  Two HA19202's easily make a 5-bit A/D converter, as shown in Fig. 1. Table 1 shows the output patterns in the 4-bit application. The output patterns in the expanded 5-bit A/D converter is shown in Table 2. V_L is the lowest reference voltage and V_H is the highest reference voltage.
- High-performance
  The comparator utilizes an ECL circuit. The output conversion to Gray code is achieved by an AND/OR circuit. The error at the middle converting point will not exceed an LSB.
- Reference Voltage of Comparator
  The power supplies, V_L and V_H, should have a low impedance to prevent the external influence.

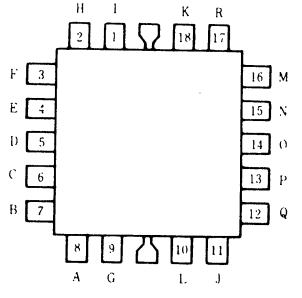
■ PIN ARRANGEMENT

HA19202



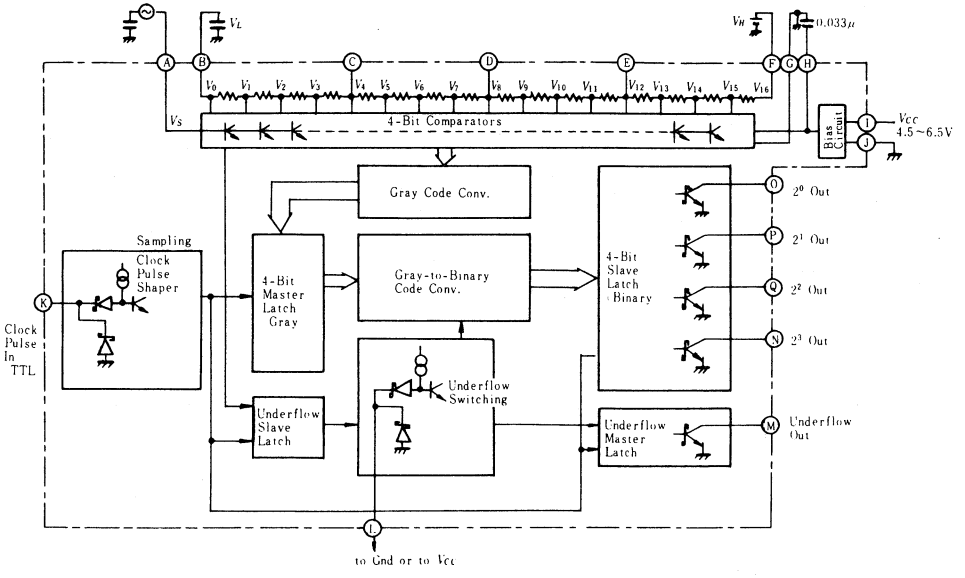
(Top View)

HA19203MP



(Top View)

■ BLOCK DIAGRAM



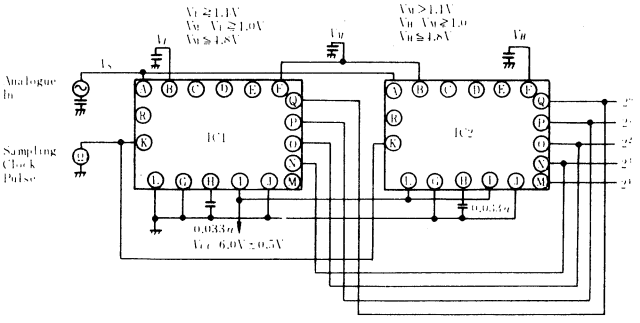


Fig. 1 Expansion to 5-bit A/D Converter

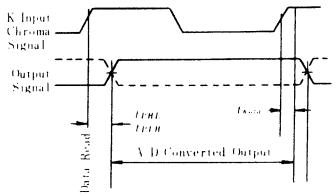


Fig. 2 Timing Chart

■ ABSOLUTE MAXIMUM RATINGS ($Ta = 25°C$)

Item	Symbol	Rating	Unit
Supply Voltage	V_{cc}	7.0	V
Input Voltage at K, L	V_{IN}	7.0	V
Output Voltage at M, Q	V_O	15.0	V
Power Dissipation	P_T	350	mW
Operating Temperature Range	T_{opr}	−10 ~ +75	°C
Storage Temperature Range	T_{stg}	−55 ~ +150	°C
Operating Supply Voltage Range	V_{cc}	4.5 ~ 6.5	V

Table 1: Output Patterns (4-bit)

a) L: GND

	V_S															
	V_0	V_1	V_2	V_3	V_4	V_5	V_6	V_7	V_8	V_9	V_{10}	V_{11}	V_{12}	V_{13}	V_{14}	V_{15}
Ⓠ	L	L	H	L	H	L	H	L	H	L	H	L	H	L	H	L	H
Ⓟ	L	L	L	H	H	L	L	H	H	L	L	H	H	L	L	H	H
Ⓞ	L	L	L	L	L	H	H	H	H	L	L	L	L	H	H	H	H
Ⓝ	L	L	L	L	L	L	L	L	L	H	H	H	H	H	H	H	H
Ⓜ	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H

b) L: Vcc

	V_S															
	V_0	V_1	V_2	V_3	V_4	V_5	V_6	V_7	V_8	V_9	V_{10}	V_{11}	V_{12}	V_{13}	V_{14}	V_{15}
Ⓠ	H	L	H	L	H	L	H	L	H	L	H	L	H	L	H	L	H
Ⓟ	H	L	L	H	H	L	L	H	H	L	L	H	H	L	L	H	H
Ⓞ	H	L	L	L	L	H	H	H	H	L	L	L	L	H	H	H	H
Ⓝ	H	L	L	L	L	L	L	L	L	H	H	H	H	H	H	H	H
Ⓜ	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H

Table 2: Output Patterns (5-bit)

	V_S																															
	V_L																V_M															
	V_0	V_1	V_2	V_3	V_4	V_5	V_6	V_7	V_8	V_9	V_{10}	V_{11}	V_{12}	V_{13}	V_{14}	V_{15}	V_0	V_1	V_2	V_3	V_4	V_5	V_6	V_7	V_8	V_9	V_{10}	V_{11}	V_{12}	V_{13}	V_{14}	V_{15}
2^0	L	L	H	L	H	L	H	L	H	L	H	L	H	L	H	L	H	L	H	L	H	L	H	L	H	L	H	L	H	L	H	L	H
2^1	L	L	L	H	H	L	L	H	H	L	L	H	H	L	L	H	H	L	L	H	H	L	L	H	H	L	L	H	H	L	L	H	H
2^2	L	L	L	L	L	H	H	H	H	L	L	L	L	H	H	H	H	L	L	L	L	H	H	H	H	L	H	L	L	H	H	H	H
2^3	L	L	L	L	L	L	L	L	L	H	H	H	H	H	H	H	H	L	L	L	L	L	L	L	L	H	H	H	H	H	H	H	H
2^4	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H

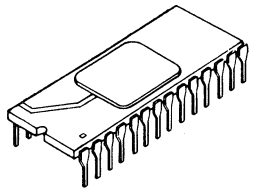
■ ELECTRICAL CHARACTERISTICS (Ta=25°C)

Item	Symbol	Test Conditions	min	typ	max	Unit
Supply Current	I_{CC}	V_{CC}=5.0V; Input Clock Pulse=10MHz	–	33	48	mA
Maximum Sampling Frequency	f_{SC}	V_{CC}=5.0V; duty=50%	10	–	–	MHz
Pin-B Minimum Input Voltage	$V_{IN\ B}$	V_{CC}=5.0V	1.1	–	–	V
Pin-F Maximum Input Voltage	$V_{IN\ F}$		–	–	V_{CC}−0.7	V
Pin-A Maximum Input Voltage	$V_{IN\ A}$		–	–	V_{CC}−0.7	V
Minimum Input Voltage Difference between Pins E and F	ΔV_{EF}		1.0	–	–	V
Pins K and L Input Voltage("H"Level)	V_{IH}		2.0	–	–	V
Pins K and L Input Voltage("L"Level)	V_{IL}		–	–	0.8	V
Pins K and L Input Current("H"Level)	I_{IH}	V_{CC}=5.25V; V_I=2.7V	–	–	20	μA
Pins K and Input L Input Current("L"Level)	I_{IL}	V_{CC}=5.25V; V_I=0.4V	–	–	−0.4	mA
Pin-K Input Clamp Voltage	V_{IK}	V_{CC}=4.75V; I_{IN}=−18mA	–	–	−1.5	V
Pins M~Q Output Voltage	V_{OL}	V_{CC}=4.75V; Low Output Level; I_{OL}=8.0mA	–	–	0.5	V
Pins M~Q Output Voltage	V_{OL}	V_{CC}=4.75V; Output Low Level; I_{OL}=4.0mA	–	–	0.4	V
A-to-D Switching Threshold Voltage		V_{CC}=5.0V; V_B=1.8V; V_F=3.8V	−50	0	+50	mV
Resistance between Pins B and C	R_{BC}		300	400	500	Ω
Resistance between Pins C and D	R_{CD}		300	400	500	Ω
Resistance between Pins D and E	R_{DE}		300	400	500	Ω
Resistance between Pins E and F	R_{EF}		300	400	500	Ω
A-to-D Converter Frequency Response(1MHz)	f_{1H}	V_{CC}=5.0V; Referred to f=100kHz	−1.0	0	+1.0	dB
A-to-D Converter Frequency Response(3MHz)	f_{3H}	V_{CC}=5.0V; Referred to f=100kHz	−3.0	0	+1.0	dB
Pin-A Maximum Input Impedance	$Z_{IN\ A}$	V_{CC}=5.0V; $V_{IN\ A}$=2.8V_{DC}	–	–	100	Ω

HA19209, HA19210 ●8-Bit Flash Type Analog-to-Digital Converter

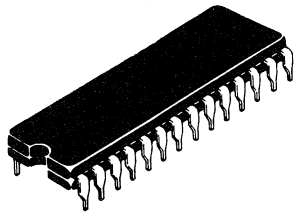
The HA19209/210 are monolithic bipolar LSI's for high speed 8-bit A/D conversion with low power dissipation. Digital data output and clock input terminals are compatible with TTL and CMOS. The device is designed for video signal processing application.

HA19209C, HA19210C



(DC-28)

HA19209P, HA19210P



(DP-28)

■ FEATURES

- 8-bit Resolution (Overflow Included).
- Low Power Dissipation: 250mW (typ).
- High Speed
- Maximum Conversion Rate: 30MSPS.
- Single Power Supply: +5V.
- Input Clock Level and Digital Output Signal Level Compatible with TTL and CMOS. (Can drive one LS TTL IC).
- No Sample & Hold Circuit Necessary.
- 28-pin Package.

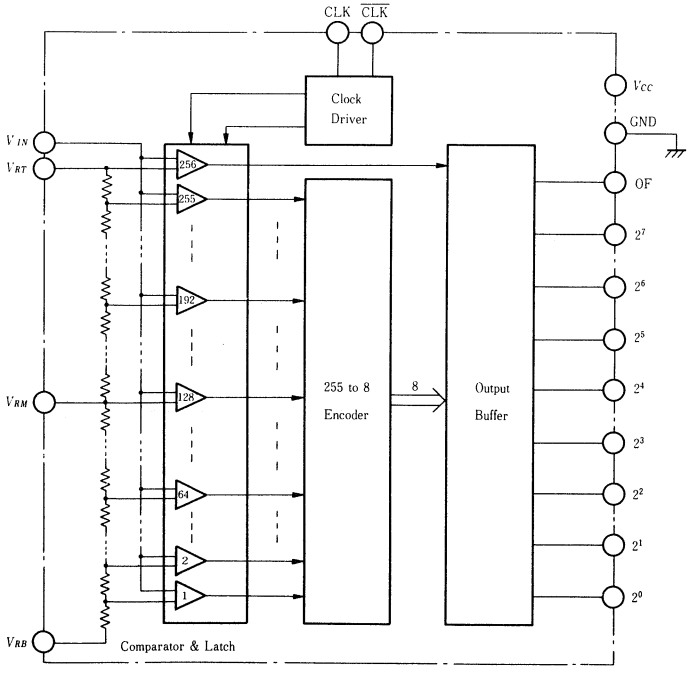
■ APPLICATIONS

- Digital Television Set, Digital Video Tape Recorder.
- Industrial Equipment with Computer for Pattern Recognition.
- High Speed Measuring Instrumentation.

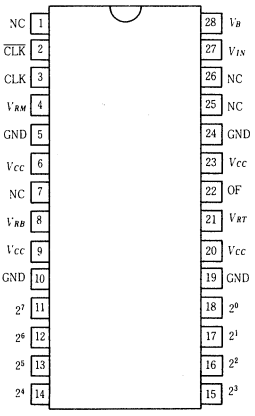
■ DIFFERENCE OF HA19209 and HA19210

- See Output Code Table

■BLOCK DIAGRAM



■PIN ARRANGEMENT



(Top View)

■ABSOLUTE MAXIMUM RATINGS (T_a=25°C, unless otherwise specified.)

Item	Symbol	Rating	Unit	Note
Supply Voltage	V_{CC}	+7.0	V	
Input Signal Voltage	V_{in}	0 to V_{CC}	V	1
Reference Input Terminal Voltage	V_R	0 to V_{CC}	V	1
Clock Input Voltage	V_{CLK}	0 to V_{CC}	V	2
Power Dissipation	P_T	800	mW	
Operating Temperature Range	T_{opr}	0 to +70	°C	
Storage Temperature Range	T_{stg}	−55 to +125	°C	

Note 1) V_{in} and V_R should not be lower than 1.2V at the same time
Note 2) V_{CLK} and $V_{\overline{CLK}}$ should not be lower than 1.5V at the same time.

■ELECTRICAL CHARACTERISTICS (T_a=25°C, V_{CC}=5V, V_{RT}=3.5V, V_{RB}=1.5V, unless otherwise specified.)

Item		Symbol	Test Conditions	min	typ	max	Unit	Note
Resolution			V_{CC}=5.0V	8	8	8	bits	
Supply Voltage Range		V_{CC}		4.75	5.0	5.25	V	
Reference Terminal Voltage Range	RT	V_{RT}	V_{CC}=5.0V	V_{RB}	3.5	V_{CC} −0.9	V	
	RB	V_{RB}	V_{CC}=5.0V	1.2	1.5	V_{RT}	V	
	RM	V_{RM}		2.4	2.5	2.6	V	1
Input Signal Voltage Range		V_{in}	V_{CC}=5.0V	V_{RB} −0.1	−	V_{RT} −0.1	V	
Input Dynamic Range		$V_{RT}-V_{RB}$		−	2.0	2.1	Vp-p	
Supply Current		I_{CC}	V_{CC}=5.0V, f_{CLK}=20MSPS	−	50	−	mA	
Reference Terminal Current	RT	I_{RT}		−	11	−	mA	
	RB	I_{RB}		−	−11	−	mA	
Input Current		I_{in}	V_{in}=4.1V	−	70	−	μA	
Input Capacitance		C_{in}	f_{IN}=1MHz, $V_{RB}<V_{in}<V_{RT}$	−	40	−	pF	
"H" Level Digital Output Voltage		V_{OH1}	I_{OH}=−400μA	−	4.2	−	V	
		V_{OH2}	I_{OH}=−5mA	−	4.0	−	V	
"L" Level Digital Output Voltage		V_{OL}	I_{OL}=400μA	−	0.6	0.75	V	
Clock Input Current		I_I	V_{CLK} : 0V to 2.7V	−	−	100	μA	
"H" Level Clock Input Voltage		V_{IH}		2.0	−	V_{CC}	V	
"L" Level Clock Input Voltage		V_{IL}		0	−	0.8	V	
Static Linearity		$N.L.$		−	±0.5	−	LSB	2
Maximum Conversion Rate		f_{CLK} max.	f_{in}=3.58MHz	20	30	−	MSPS	
Differential Gain		DG	f_{CLK}=20MSPS, NTSC, 40IRE Unlocked	−	1.0	−	%	2
Differential Phase		DP		−	0.5	−	Degree	2
Clock Pulse Width		t_{WH}	f_{CLK}=20MSPS	−	30	−	ns	
		t_{WL}		−	10	−	ns	
Digital Output Propagation Delay		t_{PD}		−	33	−	ns	
Digital Output Rise Time		t_{TLH}	R_L=2kΩ, C_L=10pF	−	10	−	ns	
Digital Output Fall Time		t_{THL}		−	20	−	ns	

Note 1) For correction of reference voltage
Note 2) See Figs. 1, 2 and 3

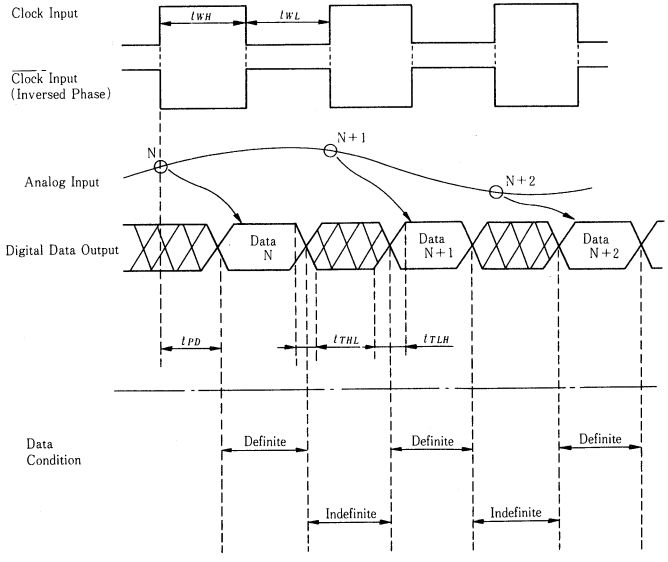
■OUTPUT CODE TABLE

Input Voltage \ Output Code	HA19209						HA19210					
	OF	2^7	2^6	⋯	2^1	2^0	OF	2^7	2^6	⋯	2^1	2^0
V_{RB}	0	0	0	⋯	0	0	0	0	0	⋯	0	0
V_{RB}+1LSB	0	0	0	⋯	0	1	0	0	0	⋯	0	1
V_{RB}+2LSB	0	0	0	⋯	1	0	0	0	0	⋯	1	0
⋮	⋮	⋮	⋮	⋯	⋮	⋮	⋮	⋮	⋮	⋯	⋮	⋮
V_{RB}+127LSB	0	0	1	⋯	1	1	0	0	1	⋯	1	1
V_{RB}+128LSB	0	1	0	⋯	0	0	0	1	0	⋯	0	0
⋮	⋮	⋮	⋮	⋯	⋮	⋮	⋮	⋮	⋮	⋯	⋮	⋮
V_{RT}−2LSB	0	1	1	⋯	1	0	0	1	1	⋯	1	0
V_{RT}−1LSB	0	1	1	⋯	1	1	0	1	1	⋯	1	1
V_{RT}	1	1	1	⋯	1	1	1	0	0	⋯	0	0

■PIN DESCRIPTION

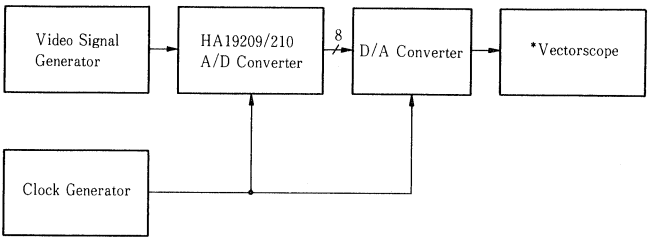
Pin No.	Symbol	Function	Pin No.	Symbol	Function
1	NC	Non Connection Pin	15	2^3	Digital Output Pin
2	$\overline{CLK}$	$\overline{Clock}$ Input Pin	16	2^2	Digital Output Pin
3	CLK	Clock Input Pin	17	2^1	Digital Output Pin
4	V_{RM}	Reference Voltage Correcting Input	18	2^0	Digital Output (LSB) Pin
5	GND	Ground Pin	19	GND	Ground Pin
6	V_{CC}	Power Supply Pin (+5V)	20	V_{CC}	Power Supply Pin (+5V)
7	NC	Non Connection Pin	21	V_{RT}	High Level Reference Input Pin
8	V_{RB}	Low Level Reference Input Pin	22	OF	Overflow Output Pin
9	V_{CC}	Power Supply Pin (+5V)	23	V_{CC}	Power Supply Pin (+5V)
10	GND	Ground Pin	24	GND	Ground Pin
11	2^7	Digital Output (MSB) Pin	25	NC	Non Connection Pin
12	2^6	Digital Output Pin	26	NC	Non Connection Pin
13	2^5	Digital Output Pin	27	V_{IN}	Analog Input Pin
14	2^4	Digital Output Pin	28	V_B	Connect 100kΩ to V_{CC}

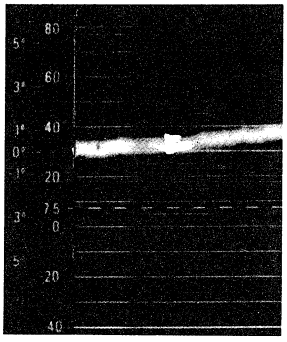
■TIMING DIAGRAM FOR SAMPLING



TEST CIRCUIT BLOCK DIAGRAM

1. Differential Gain (DG), Differential Phase (DP)

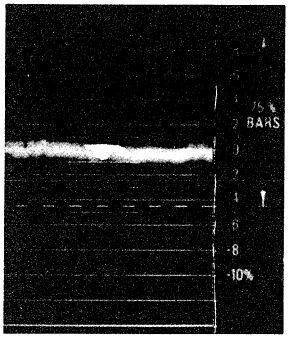




Differential Phase (DP)

[40IRE Modulated
NTSC Ramp
f_{CLK}=20MSPS Unlocked]

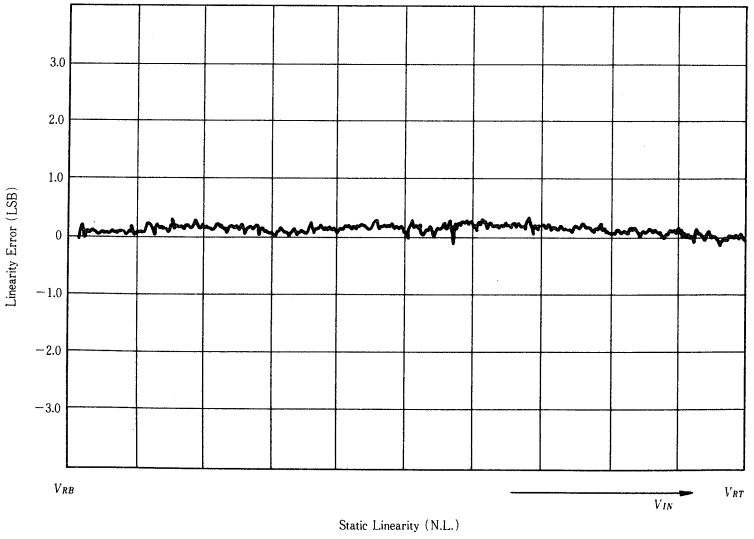
Fig. 1



Differential Gain (DG)

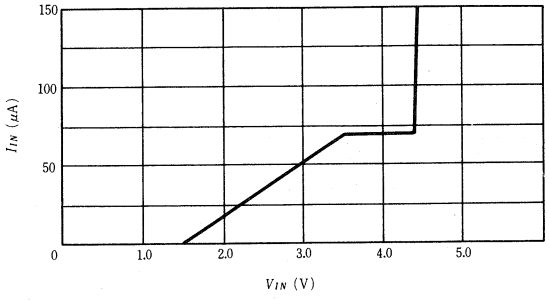
[40IRE Modulated
NTSC Ramp
f_{CLK}=20MSPS Unlocked]

Fig. 2



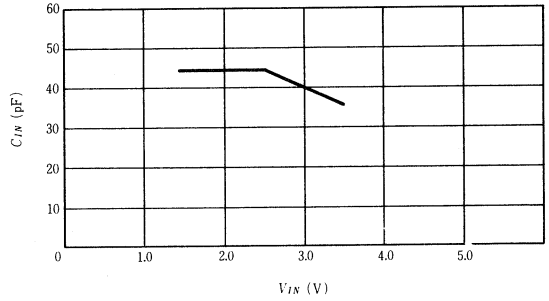
Static Linearity (N.L.) [V_{RT}=3.5V, V_{RB}=1.5V, f_{CLK}=20MSPS]

Fig. 3



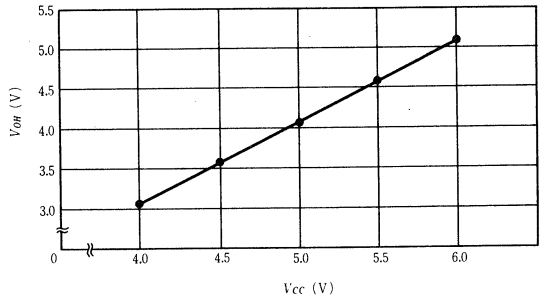
Analog Input Terminal
D.C. Characteristic
[V_{CC}=5.0V, Temp.=25°C
V_{RT}=3.5V, V_{RB}=1.5V]

Fig. 4



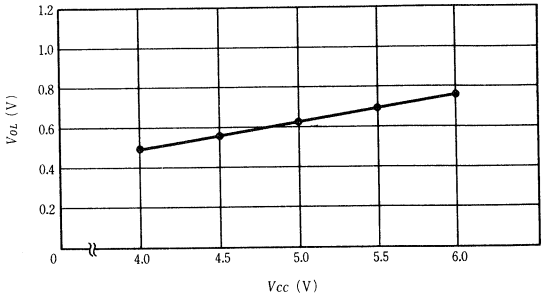
Input Capacitance
Versus Input DC Level
[V_{CC}=5.0V, Temp.=25°C
V_{RT}=3.5V, V_{RB}=1.5V
fin=1MHz]

Fig. 5



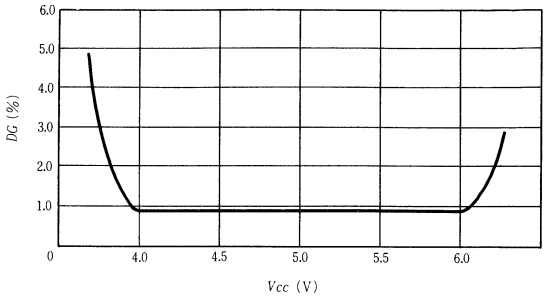
"H" Level Digital Output
Versus Supply Voltage
[Temp.=25°C, I_{OH}=−400μA]

Fig. 6



"L" Level Digital Output
Versus Supply Voltage
[Temp.=25°C, I_{OL}=400μA]

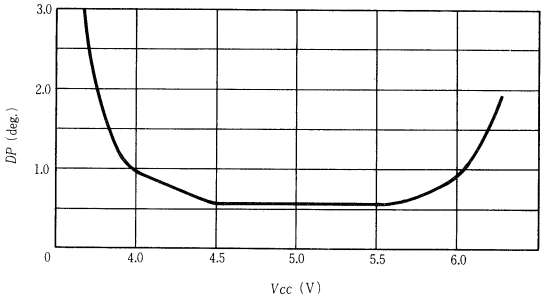
Fig. 7



Differential Gain
Versus Supply Voltage

[f_{CLK} = 20MSPS,
40IRE modulated NTSC
RAMP unlocked,
V_{RT} = 3.5V, V_{RB} = 1.5V
Temp. = 25°C]

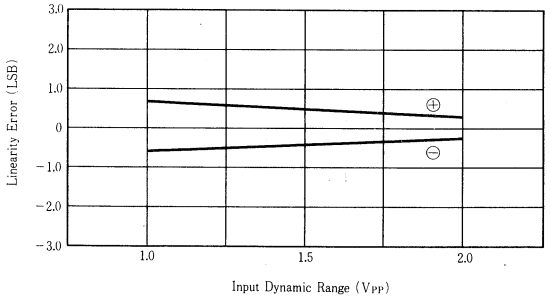
Fig. 8



Differential Phase
Versus Supply Voltage

[f_{CLK} = 20MSPS,
40IRE modulated NTSC
RAMP unlocked,
V_{RT} = 3.5V, V_{RB} = 1.5V
Temp. = 25°C]

Fig. 9



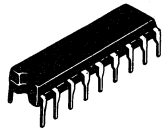
Static Linearity Error
Versus Input Dynamic Range

[V_{CC} = 5.0V, f_{CLK} = 20MSPS
V_{RB} = 1.5V
Temp. = 25°C]

Fig. 10

HA19216P ●6-bit Flash Type Analog-to-Digital Converter

The HA19216P is bipolar LSI for high speed 6-bit A/D conversion. Digital data output and clock input terminals are compatible with TTL and CMOS. The HA19216P is designed for video signal processing application.



(DP-18)

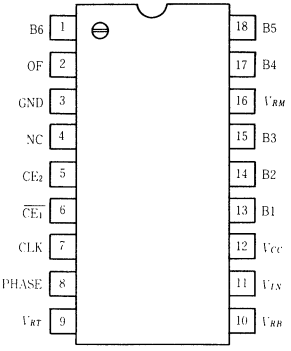
■ FEATURES

- 6-bit Resolution (Overflow Included).
- 6-bit Latched High Impedance State Outputs.
- Maximum Conversion Rate: 30M$_{SPS}$.
- Single Power Supply: +5V.
- Digital Data Output, High Impedance State Control and Clock Input Terminals Compatible with TTL and CMOS.
- No Sample & Hold Circuit Required.
- 18-Pin Package.
- Output Current
  I_{OL} = 2mA (guaranteed)
  I_{OH} = –5mA (guaranteed)

■ APPLICATION

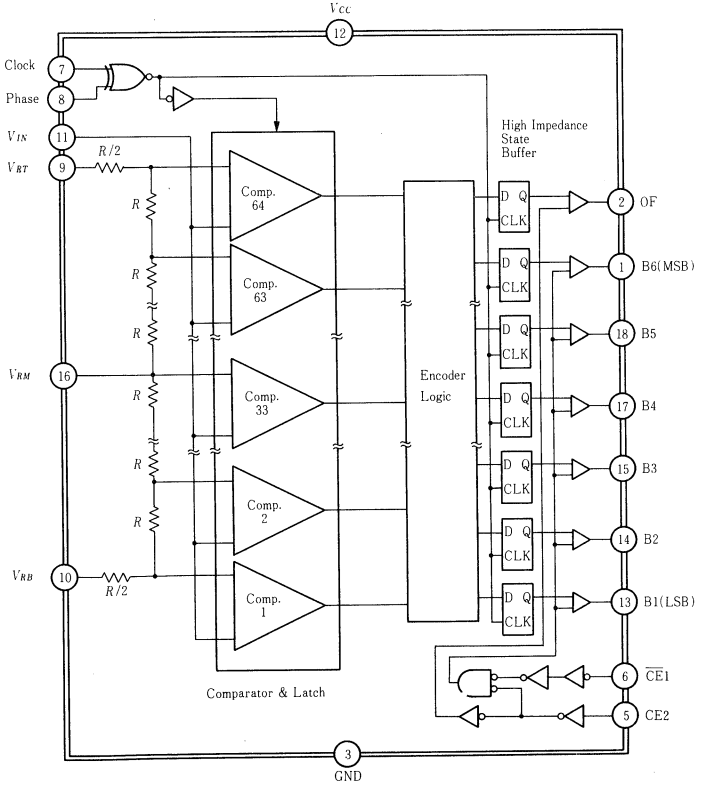
- Pattern recognizor using a computer.
- High-speed measuring instrument.

■PIN ARRANGEMENT



(Top View)

■BLOCK DIAGRAM



■ABSOLUTE MAXIMUM RATINGS (T_a=25°C, unless otherwise specified.)

Item	Symbol	Rating	Unit
Supply Voltage	V_{CC}	+7.0	V
Input Signal Voltage*	V_{IN}	0 to V_{CC}	V
Input Reference Voltage*	V_R	0 to V_{CC}	V
Digital Input Voltage	V_I	0 to V_{CC}	V
Applied Voltage to Digital Output Pin in High Impedance	V_O	0 to V_{CC}	V
Power Dissipation	P_T	550	mW
Operating Temperature	T_{opr}	0 to 70	°C
Stroage Temperature	T_{stg}	−55 to +125	°C

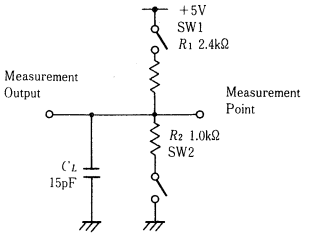
*: V_{IN} and V_R should not be lower than 1.5V at the same time.

■ELECTRICAL CHARACTERISTICS (T_a=25°C, V_{CC}=5.0V, V_{RT}=3.0V, V_{RB}=2.0V, unless otherwise specified.)

Item		Symbol	Test Conditions	min	typ	max	Unit
Resolution				6	6	6	bits
Operating Supply Voltage		V_{CC}		4.75	5.0	5.25	V
Quiescent Current		I_{CC}	f_{CLK}=20 Msps	–	50	84	mA
Reference Pin Voltage Setting Range	RT	V_{RT}	V_{RT}> V_{RM}> V_{RB}	–	3.0	3.5	V
	RB	V_{RB}	V_{RT}> V_{RM}> V_{RB}	1.5	2.0	–	V
	RM	V_{RM}	V_{RT}> V_{RM}> V_{RB}		(V_{RT} + V_{RB})/2±0.1		V
Input Dynamic Range		V_{RT} − V_{RB}		–	1.0	1.3	Vp-p
Digital Input Voltage	H	V_{IH}		2.0	–	V_{CC}	V
	L	V_{IL}		0	–	0.8	V
Digital Input Current	H	I_{IH}	V_I=2.7V	–	–	100	μA
	L	I_{IL}	V_I=0.4V	−100	–	–	μA
Digital Output Voltage	H	V_{OH}	I_{OH}=−5mA	3.4	3.8		V
	L	V_{OL}	I_{OL}=2mA	–	0.61	0.76	V
Digital Output Current*	H	I_{OZH}	V_O=5.0V	–	–	100	μA
	L	I_{OZL}	V_O=0.5V	−100	–	–	μA
Reference Current	RT	I_{RT}	V_{IN}=1.9V	–	8	12	mA
	RB	I_{RB}	V_{IN}=3.1V	−12	−8	–	mA
Input Current		I_{IN}	V_{IN}=3.1V	–	20	50	μA
Input Capacitance		C_{IN}	V_{RB}< V_{IN}< V_{RT}, $f(V_{IN})$=1MHz	–	15	–	pF
Linearity Error		$N.L$		–	±1/4	–	LSB
Max. Conversion Rate		f_{CLK} max.		20	30	–	Msps
Digital Output Propagation Delay		t_{PD}	C_L=15pF	–	34	50	ns
Digital Output Rise Time		t_{TLH}	C_L=15pF	–	10	15	ns
Digital Output Fall Time		t_{THL}	C_L=15pF	–	17	33	ns
Digital Output Enable Time*		t_{ZH}		–	12	20	ns
		t_{ZL}		–	48	70	ns
Digital Output Disable Time*		t_{HZ}		–	32	43	ns
		t_{LZ}		–	23	33	ns
Clock Pulse Width	V_{phase}=0.8V	t_{WH}		28	–	–	ns
		t_{WL}		15	–	–	ns
	V_{phase}=2.0V	t_{WH}		10	–	–	ns
		t_{WL}		33	–	–	ns

* When high impedance state

●Measurement Load of Digital Output, Enable Time, Disable Time



- C_L includes probe, capacity, floating capacity of measurement equipment.
- When t_{ZL}, t_{LZ} measurement: SW1; ON, SW2; OFF
  When t_{ZH}, t_{HZ} measurement: SW1; OFF, SW2; ON

■PIN FUNCTIONS

Pin No.	Symbol	Function	Pin No.	Symbol	Function
1	B6	Digital Output (MSB) Pin	10	V_{RB}	Low Level Reference Voltage Input Pin
2	OF	Didital Output (Overflow) Pin	11	V_{IN}	Analog Input Pin
3	GND	Ground Pin	12	V_{CC}	Power Supply Pin
4	NC	Non Connection Pin*	13	B1	Digital Output (LSB) Pin
5	CE_2	High Impedance Control Input to Digital Output**	14	B2	Digital Output Pin
6	$\overline{CE_1}$	High Impedance Control Input to Digital Output**	15	B3	Digital Output Pin
7	CLK	Clock Input Pin	16	V_{RM}	Reference Voltage Center Tap Pin
8	PHASE	Clock Phase Control Pin	17	B4	Digital Output Pin
9	V_{RT}	High Level Reference Voltage Input Pin	18	B5	Digital Output Pin

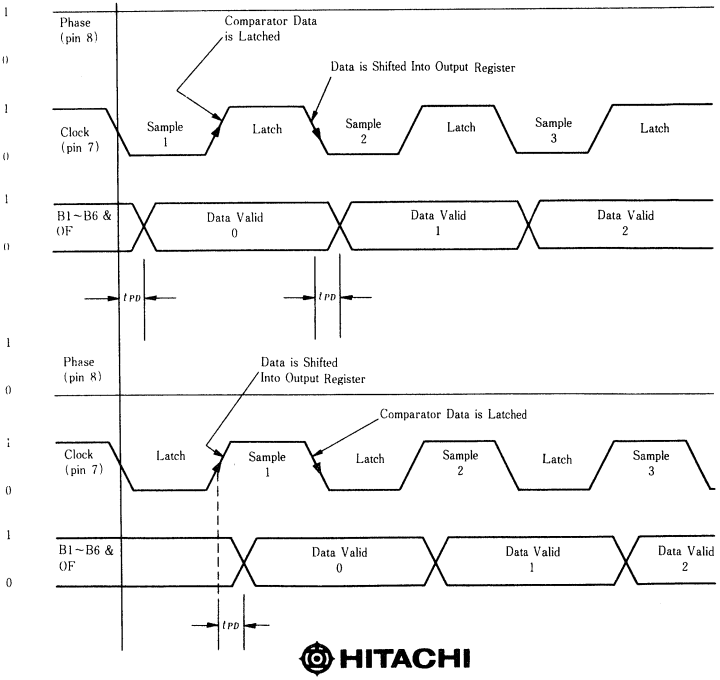
* Use with disconnected NC pin.

**

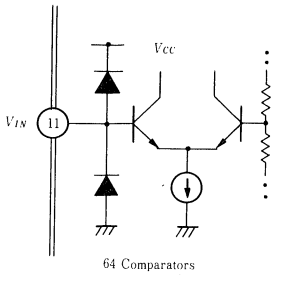
$\overline{CE_1}$	CE_2	B1 ~ B6	OF
×	L	Z	Z
L	H	H/L	H/L
H	H	Z	H/L

H: High Level
L: Low Level
×: Don't care.
Z: High Impedance

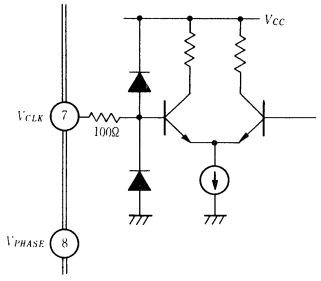
■TIMING DIAGRAM



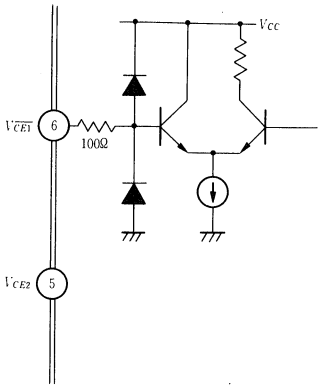
INTERFACE



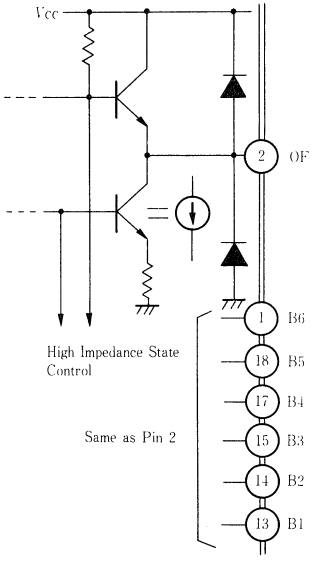
Analog Input



Clock Input



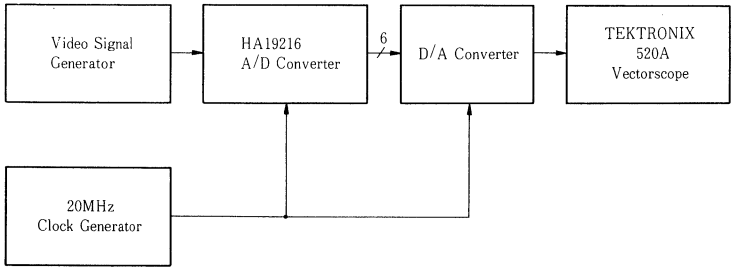
High Impedance State Control Input



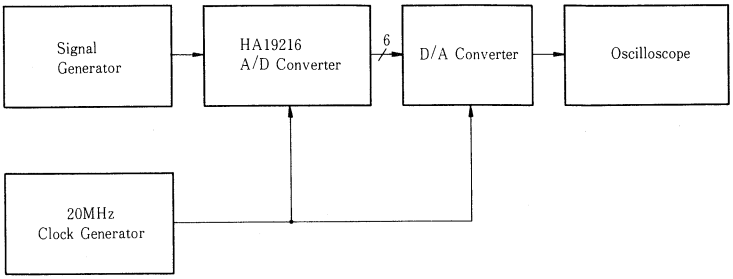
Digital Output

MEASURING CIRCUIT

● Measurement of DG and DP

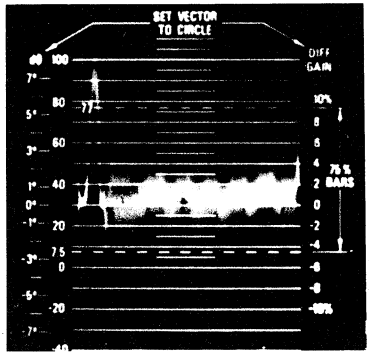


● Measurement of Analog Input Frequency Response



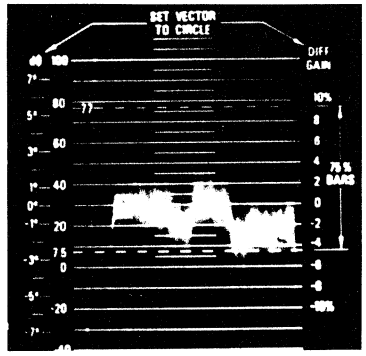
■HIGH FREQUENCY ANALOG INPUT RESPONSE

Differential Phase



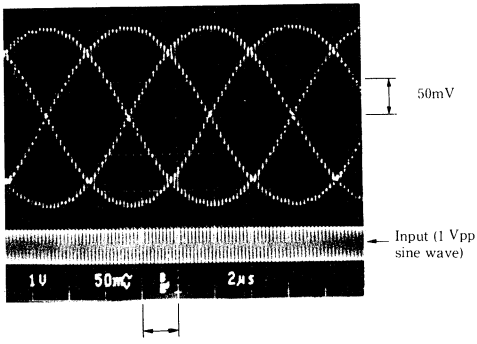
40 I_{RE} Modulated NTSC Ramp
f_{CLK} = 20MSPS Unlocked

Differential Gain

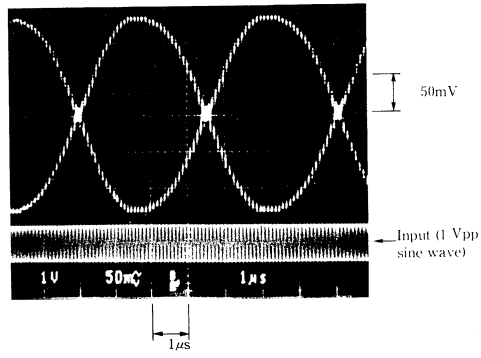


40 I_{RE} Modulated NSTC Ramp
f_{CLK} 20MSPS Unlocked

Beat-frequency waveform of 5.05MHz input signal-sampling at 20MHz



Beat-frequency waveform of 10.14MHz input signal-sampling at 20MHz

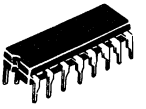


DATA SHEETS

Microprocessor Peripheral

HA13007 ●Quad. Driver

HA13007 is a monolithic, bipolar, high voltage, high current Quad. Driver especially designed for switching applications. This device is recommended for the interfacing from low-level logic to peripheral loads such as relays, solenoids, stepping motors, LED, heaters and other similar high voltage, high current loads.

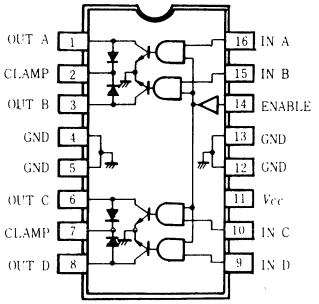


(DP-16A)

■ FEATURES

- Guaranteed minimum output breakdown of 60V, and maximum output current of 0.7A.
- Low output collector-emitter saturation voltage.
- Compatible inputs with TTL, LSTTL and 5V CMOS.
- Included integral transient suppression diodes for inductive loads.
- Less input current.

■ PIN ARRANGEMENT



(Top View)

■ TRUTH TABLE

ENABLE	IN	OUT
H	H	L
H	L	H
L	×	H

for each input:
H = High level; 2.0V
L = Low level; 0.8V
× = Irrelevant

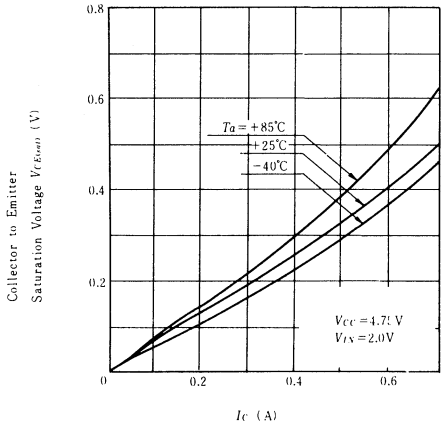
■ ABSOLUTE MAXIMUM RATINGS ($Ta = 25°C$)

Item		Symbol	Rating	Unit	Note
Supply Voltage		V_{CC}	7.0	V	1
Input Voltage		V_{IN}	0 to V_{CC}	V	
Output Voltage		V_{CEX}	60	V	
Output Current		I_{OUT}	0.7	A	
Power Dissipation		P_T	1.85	W	2
Thermal Resistance	Junction-Case	θ_{jc}	15	°C/W	
	Junction-Ambient	θ_{ja}	60	°C/W	
Junction Temperature		T_j	150	°C	
Operating Junction Temperature Range		T_{jop}	−40 to +125	°C	
Storage Temperature Range		T_{stg}	−55 to +125	°C	

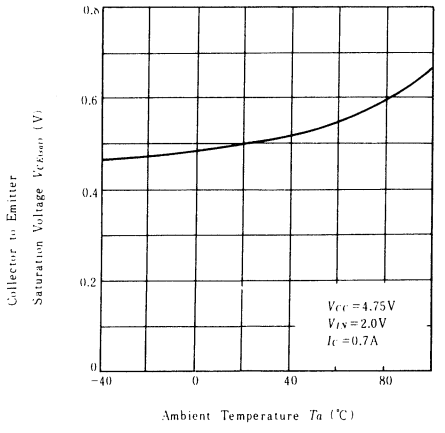
Note) 1. Recommended operating voltage $V_{CC} = 4.75$ to 5.5V
2. Thermal Resistances are as follows:
$\theta_{j-a1} \leqq 60°C/W$ (Soldered on a print circuit board)
$\theta_{j-a2} \leqq 35°C/W$ (Soldered on a print circuit board with copper sufficiently)
$\theta_{j-a3} \leqq 15°C/W$ (Soldered on pin 4, 5, 12 and 13 with an infinity heat sink)

■ELECTRICAL CHARACTERISTICS (Ta=25°C, V_{CC}=5.5V)

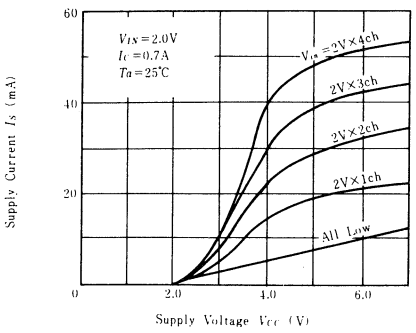
Item	Symbol	Test Condition		min	typ	max	Unit
Output Leakage Current	I_{CEX}	V_{CE}=60V, V_{IN}=0.8V		—	—	100	μA
Output Sustaining Voltage	$V_{CE(sus)}$	V_{IN}=0.8V, I_C=10mA		60	—	—	V
Output Saturation Voltage	$V_{CE(sat)}$	V_{CC}=4.75V, V_{IN}=2.0V	I_C=0.4A	—	0.3	0.5	V
			I_C=0.7A	—	0.5	0.7	
Input Low Voltage	V_{IL}			—	—	0.8	V
Input Low Current	I_{IL}	V_{IN}=0.8V, I_C=0		—	−1	±10	μA
Input High Voltage	V_{IH}			2.0	—	—	V
Input High Current	I_{IH}	I_C=0.7A×4	V_{IN}=2.0V	—	0	±10	μA
			V_{IN}=5.0V	—	—	1.0	mA
Supply Current (All Output ON)	I_S	I_C=0.7A×4, V_{IN}=5.5V (All Inputs)		—	50	65	mA
Supply Current (All Outputs OFF)	I_{SO}	V_{IN}=0.8V (All Inputs)		—	8.0	—	mA
Clamp Diode Leakage Current	I_R	V_R=60V		—	—	100	μA
Clamp Diode Forward Voltage	V_F	V_{IN}=0.8V	I_F=1.0A	—	1.2	1.6	V
			I_F=1.5A	—	1.3	2.0	V
Turn-On Delay	t_{PLH}			—	1.0	—	μs
Turn-Off Delay	t_{PHL}			—	0.3	—	μs



$V_{CE(sat)}$ — I_C



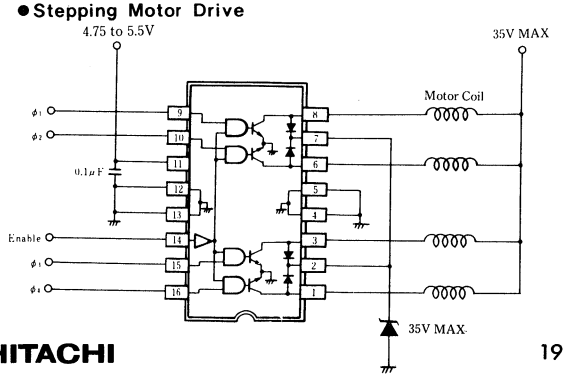
$V_{CE(sat)}$ — Ta



I_S — V_{CC}

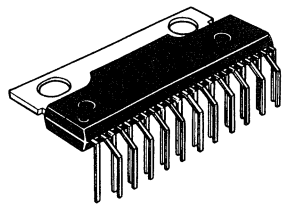
■APPLICATION

●Stepping Motor Drive



HA13406W ● Three-phase Brushless Motor Driver

HA13406W is a power IC developed for use in the three phase brushless motor driving.
This provides hall amp, logic part, output amp, control amp, and forward and back rotation circuit functions in one chip. As the maximum driving current and voltage is as much as 3A x 12V per phase. Therefore, this finds best use in the spindle motor driving of 5.25 inches HDD.



(SP-23TA)

■ FEATURES

- 3A Output Current Capability.
- Low Output Saturation Voltage.
- Hall Amp with Hysteresis.
- With Over Temperature Protection.
- Low Thermal Resistance Package.

■ ABSOLUTE MAXIMUM RATINGS ($Ta=25℃$)

Item		Symbol	Ratings	Unit
Control Stage Supply Voltage (Note 1)		V_{CC1}	7	V
Output Stage Supply Voltage (Note 1)		V_{CC2}	15	V
Output Current		I_O	3	A
Power Dissipation		P_T	25	W
Thermal Resistance	Junction-Case	θ_{j-c}	3.0	℃/W
	Junction-Ambient	θ_{j-a}	40	
Hall Amp Input Voltage		V_H	0 to V_{CC1}	V
Direction Voltage		V_D	0 to V_{CC1}	V
Control Voltage		V_{CTL}	0 to V_{CC1}	V
Junction Temperature		T_j	150	℃
Operating Junction Temperature Range		T_{jop}	−20 to +125	℃
Storage Temperature Range		T_{stg}	−55 to +125	℃

Note) 1. Recommended Operating Voltage

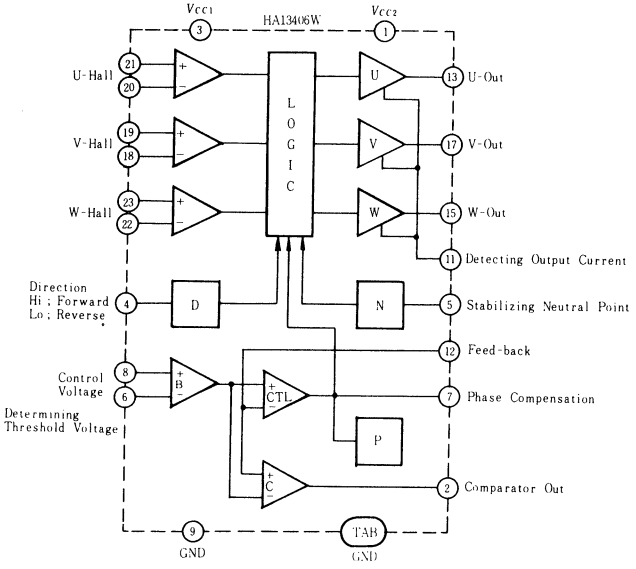
	min	typ	max	Unit
V_{CC1}	4.5	5.0	5.5	V
V_{CC2}	10.2	12	13.8	V

■ ELECTRICAL CHARACTERISTICS (Ta=25℃, V_{CC1}=5V, V_{CC2}=12V)

Item		Test Conditions		min	typ	max	Unit	Test Terminal	Note
Total	Quiescent Current	V_{CTL}=0V	V_{CC1}	—	10	15	mA	3	
			V_{CC2}	—	10	15	mA	1	
		V_{CTL}=V_{CC1}, R_L=Open	V_{CC1}	—	10	15	mA	3	
			V_{CC2}	—	105	150	mA	1	
	Thermal Shut-Down Temperature	V_{CTL}=V_{CC1}, I_O=0.1A		—	150	—	℃		1
Hall Amp to Logic	Input Bias Current			—	—	±50	μA	18~23	
	Input Common-mode Voltage Range			2.0	—	3.0	V	Ditto	
	Hysteresis width	R_F=220Ω		15	—	30	mV	Ditto	
Output	Sustaining Voltage	I_C=20mA		15	—	—	V	13.15.17	
	Leak Current	V_{CE}=15V		—	—	10	mA	Ditto	
	Saturating Voltage	V_{CTL}=V_{CC1}, I_O=2.8A		—	2.8	3.8	V	Ditto	2
Buffer	Internal Reference Voltage			2.35	2.5	2.65	V	6	
	Output Resistance of Reference			—	2.5	—	kΩ	Ditto	
	Threshold Voltage	I_O=20mA		—	100	—	mV	8	3
	Input Current	V_{CTL}=5V		—	0	±10	μA	Ditto	
		V_{CTL}=1V		—	−3	±10	μA	Ditto	
	Voltage Gain	I_O=0.8A, f=500Hz		—	0	—	dB	11	
Control Amp	Input Offset Voltage	I_O=20mA		—	100	—	mV	12	
	Voltage Gain	I_O=0.8A, f=500Hz		—	0	—	dB	11	
Comparator	Leak Current	V_{CE}=15V		—	—	1.0	mA	2	
	Saturation Voltage	I_C=20mA		—	1.0	1.5	V	Ditto	
Direction	Voltage Range for Forward Mode			2.0	—	5	V	4	
	Voltage Range for Reverse Mode			0	—	0.7	V	Ditto	
	Input Current	V_D=GND		—	−1.2	—	mA	Ditto	
		V_D=5V		—	0	—	mA	Ditto	

Notes) 1. The specification indicates the temperature of the case.
2. The specification shows the sum of the upper and lower saturation voltage.
3. Reference to pin 6.

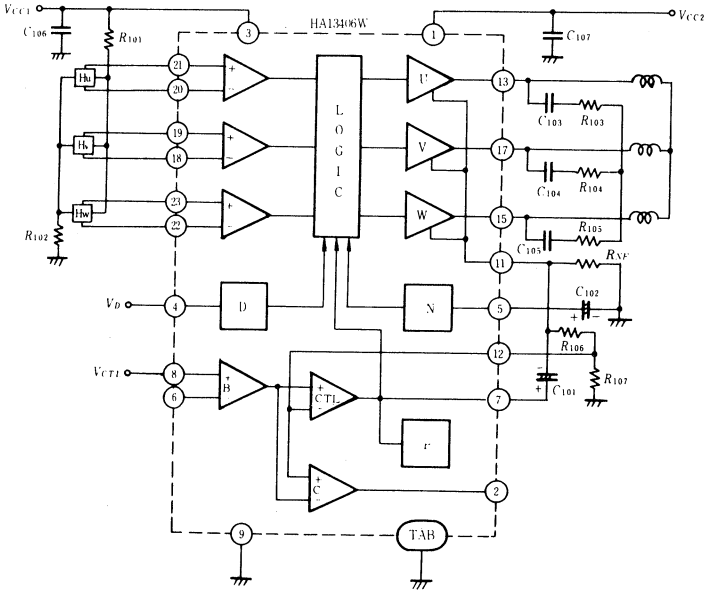
■ BLOCK DIAGRAM



U, V, W : Output Amp
B : Buffer Amp
CTL : Control Amp
C : Comparator
D : Direction
N : Neutral Point Feed-back
P : Protector

■ APPLICATION

● LINEAR DRIVE



Description :

The output stage is saturated at starting and is not saturated in usual. Therefore, the loss is comparatively large and heat sink may be required.

Relationship between the current Io which flows into the motor coil and the control Voltage V_{CTL}, the following is given.

$$I_O = \frac{(R_{106}+R_{107})}{R_{107}} \frac{V_{CTL}-V_{Ref}}{R_{NF}} \quad \cdots\cdots\cdots\cdots(1)$$

where $V_{CTL} \geqq V_{Ref}$

Here, the V_{Ref} is the voltage at pin 6 and determined to $Vcc_1/2$ internally.

Consequently, connecting the output of the servo IC to the terminal 8, constructs the servo motor driving system.

Under the conditions of R106 = 0, R107 = ∞ (i.e. Voltage gain of the control amp is 0dB), Equation (1) will be as follows.

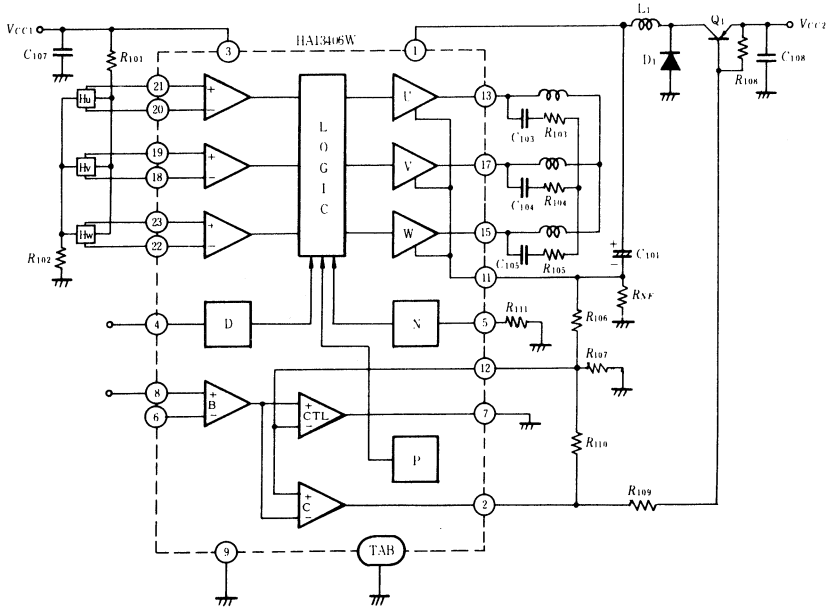
$$I_O = \frac{V_{CTL}-V_{Ref}}{R_{NF}} \quad \cdots\cdots\cdots\cdots(2)$$

External Components

Parts No.	Recommended Value	Purpose	Note
R_{101}, R_{102}	——	For hall elements bias	1
R_{103}, R_{104}, R_{105}	10Ω (1/4W)	For stability	
R_{106}, R_{107}	——	For determining the control amp gain	
R_{NF}	0.22Ω (2W)	For detecting output current	
C_{101}	1μF/16WV	For phase compensation of control amp	
C_{102}	10μF/16WV	For stabilizing the neutral point	
C_{103}, C_{104}, C_{105}	10μF/16WV	For stability	2
C_{106}	0.1μF	For power supply by-passing	
C_{107}	100μF/16WV	For power supply by-passing	

Notes) 1. Determine it so that the input voltage of hall amp (AC) will be more than $100mV_{P-P}$.
2. If the system will be adversely affected by the spike voltage at commutation, make it larger (max 22μF).

●HIGH EFFICIENCY DRIVE



Description :

As the output stage is always saturated, the loss is less than the case in the application of Linear Drive and the efficiency of the system may be increased.

The comparator, C oscillates automatically and its ON-OFF duty is controlled by the control voltage V_{CTL}. Consequently, the ON-OFF duty of the external switching transistor Q_1 is also controlled by V_{CTL}. That results to so-called PWM control of power supply, which means that one pin voltage of IC's is controlled.

To the comparator C, the voltage which appears at current detection resistor R_{NF} feedbacks, so that the relationship between the current which flows the motor coil, Io and the control voltage V_{CTL} is also shown in the equation (1).

The automatic oscillating frequency, fc is mostly determined by the external constant on around the duty of 50%.

$$f_C \doteqdot \frac{R_{NF} R_{110}}{4 L_1 R_{106}} \quad \cdots\cdots (3)$$

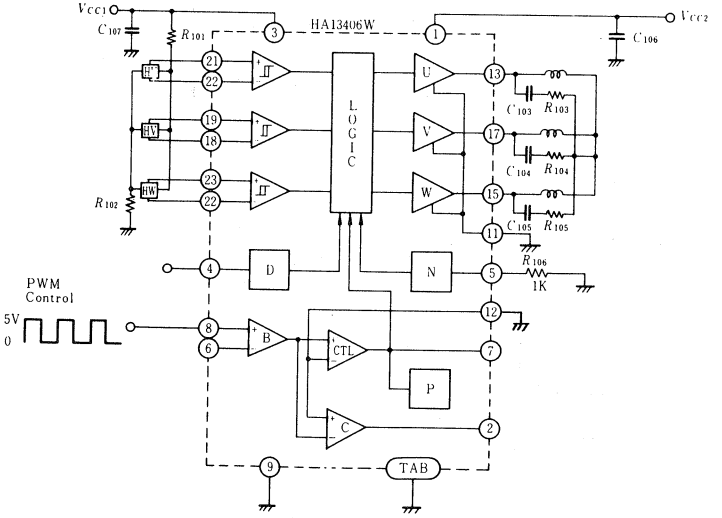
The fc is recommended to be set in the range between 20k and 100 kHz.

External Components

Parts No.	Recommended Value	Purpose	Note
R_{101}, R_{102}	—	For hall elements bias	
R_{103}, R_{104}, R_{105}	10Ω (1/4W)	For stability	1
R_{106}, R_{107}	—	For determining the control	
R_{108}	2.2kΩ (1/4W)	For preventing from error-operation caused by the leak current	
R_{109}	2.2kΩ (1/4W)	For limiting output current of comparator	
R_{110}	—	For determining the hysteresis of comparator	
R_{111}	4.7kΩ	For bias of Neutral Point Feedback Circuit	
R_{NF}	0.22Ω (2W)	For detecting output current	
C_{101}	100μF/16WV	Low pass filter	
C_{103}, C_{104}, C_{105}	0.1μF	For stability	1
C_{107}, C_{108}	0.1μF	For power supply by-passing	
L_1	1mH	Low pass filter	
Q_1	—	For switching power supply	
D_1	—	Fly Wheel Diode	

Note) 1. If no oscillation occurs, it may be deleted.

● HIGH FREQUENCY DRIVE



Description :

As the output stage is always saturated, the loss is less than case in the application (1) and the efficiency of the system may be increased.

In this application, output transistors are saturated or shut off. Output transistors switch on (saturated) at control input "H", switch off at the state "Lo". That is, Motor speed can be controlled by PWM (Pulse Width Modulation)

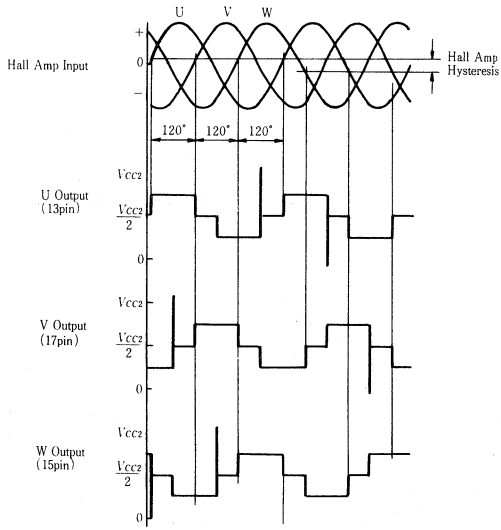
Frequency range from 1 kHz to 20 kHz is recommended for the fundamental frequency.

External Components

Parts No.	Recommended Value	Purpose	Note
R_{101}, R_{102}	—	For Hall elements bias	
R_{103}, R_{104}, R_{105}	10Ω (1/4W)	For stability	1
R_{106}	1kΩ	For output stage bias	
C_{103}, C_{104}, C_{105}	0.1μF	For stability	
C_{106}, C_{107}	0.1μF	For power supply by-passing	

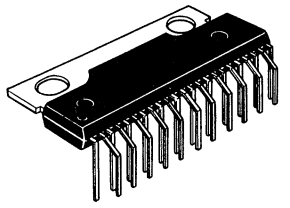
Notes) 1. If no oscillation occurs, it may be deleted.

● TIMING CHRAT



HA13408 ●9-channel Power Driver

HA13408 is 9-channel Power Driver IC, designed for head driver of dot printer. This IC enables to drive 9 dot printers without using any other external components or IC's.
HA13408 can be used for 2 system four-phase step drive, as every channel is used independently.



(SP-23TA)

■ FEATURES

- High output Current (MAX 1.5A/channel)
- High Sustaining Voltage (MIN 50V)
- Low Saturation Voltage
- Low Supply Current
- Low Input Current
- Compatible with TTL, LSTTL & 5V-C-MOS
- Low Thermal Resistance Package
- With Zener Diode

■ ABSOLUTE MAXIMUM RATINGS ($Ta=25℃$)

Item	Symbol	Rating	Unit	Note
Supply Voltage	V_{CC1}	7.0	V	
Input Voltage	V_I	V_{CC1}	V	
Output Voltage	$V_{CE(sus)}$	50	V	
Output Current	I_O	1.5	A	
Power Dissipation	P_T	20	W	1
Junction Temperature	T_j	150	℃	
Operating Junction Temperature Range	T_{jop}	−20 to +125	℃	
Storage Temperature Range	T_{stg}	−55 to +125	℃	

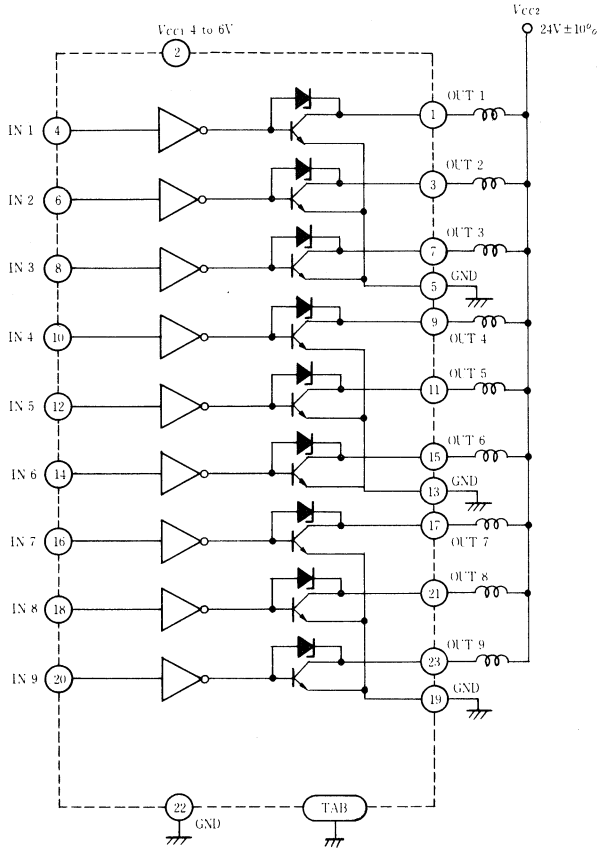
Note) 1. Thermal Resistance $\theta_{j-a} \leqq 40℃/W$
$\theta_{j-c} \leqq 3℃/W$

■ ELECTRICAL CHARACTERISTICS ($Ta=25℃$, $V_{CC1}=5V$)

Test Item	Symbol	Test Conditions	min	typ	max	Unit	Note
Input Low Voltage	V_{IL}	$V_{CC1}=4.0V$	—	—	0.8	V	
Input High Voltage	V_{IH}	$V_{CC1}=6.0V$	2.0	—	—	V	
Input Low Current	I_{IL}	$V_I=0V$	−100	−15	+10	μA	
Input High Current	I_{IH}	$V_I=2.4V$	−10	0	+10	μA	
Supply Current	I_{CCO}	All $V_I=2.4V$	—	30	45	mA	
	I_{CC}	All $V_I=0V$	—	33	50	mA	
Output Cut Off Current	I_{CEO}	$V_{CC1}=6V$, $V_{CC2}=40V$, $V_I=2.0V$	—	—	1.0	mA	
Output Saturation Voltage	$V_{CE(sat)}$	$V_{CC1}=4V$, $I_O=1.0A$, $V_I=0.8V$	—	1.6	2.2	V	
Output Sustaining Voltage	$V_{CE(sus)}$	$I_O=1.0A$	50	—	—	V	1
Delay Time	t_{PLH}	Turn OFF	—	1.5	5	μs	
	t_{PHL}	Turn ON	—	0.3	5	μs	

Note) 1. The conditions of Loading ; Measure at $L_S=5mH$, $R_S=22Ω$.

■BLOCK DIAGRAM



TRUTH TABLE

Input	Output
LO	ON
HI	OFF
OPEN	OFF

■PEAK CURRENT AND TURN-OFF TIME

The Fig. 1 shows waveforms of load current (Iout) and output terminal voltage (Vout) when driving inductive load.

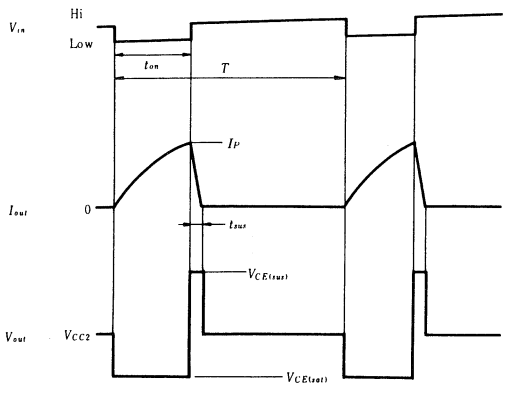


Fig.1

The peak value of output current (Ip) and sustaining time (t_{sus}) are obtained as follows;

$$I_P = \frac{V_{CC2} - V_{CE(sat)}}{R}\left(1 - exp - \frac{R}{L}t_1\right) \fallingdotseq \frac{V_{CC2}}{R}\left(1 - exp\left(-\frac{R}{L}t_o\right.\right. \quad \cdots\cdots(1)$$

$$t_{sus} = \frac{L}{R} l_n \left(1 + \frac{I_P \cdot R}{V_{CE(sus)} - V_{CC2}}\right) \quad \cdots\cdots(2)$$

Where L is self-inductance of load and R is direct current resistance of load.

For example, under the following conditions;

L = 5mH, R = 22Ω, Supply Voltage V_{CC2} = 24V,
The time to drive load ton = 0.42ms.

Peak Current (Ip) and sustaining time (t_{sus}) are obtained as follows;

Ip = 0.87 (A)
t_{sus} = 0.118 (ms)
where $V_{CE(sat)}$ = 1.3V typ. and $V_{CE(sus)}$ = 52V typ.

POWER DISSIPATION

On the other hand, in case of driving inductive load, power dissipation is determined in the following.

At first, average power dissipation (P_{on}) per channel at t_{on} is obtained as follows;

$$P_{on} \fallingdotseq V_{CE(sat)} I_P \left(\frac{V_{CC2}}{R \cdot I_P} - \frac{1}{t_{on}} \frac{L}{R} \right) \quad \cdots\cdots (3)$$

Average power dissipation (P_{sus}) at t_{sus};

$$P_{sus} \fallingdotseq V_{CE(sus)} I_P \left(\frac{1}{t_{sus}} \frac{L}{R} - \frac{V_{CE(sus)} - V_{CC2}}{R \cdot I_P} \right) \quad \cdots\cdots (4)$$

Where I_P and t_{sus} are obtained in the equation (1) and (2).

Average power dissipation (P_T) per channel for a period is obtained as follows;

$$P_T = \frac{1}{T} (P_{on} \cdot t_{on} + P_{sus} \cdot t_{sus}) \quad \cdots\cdots (5)$$

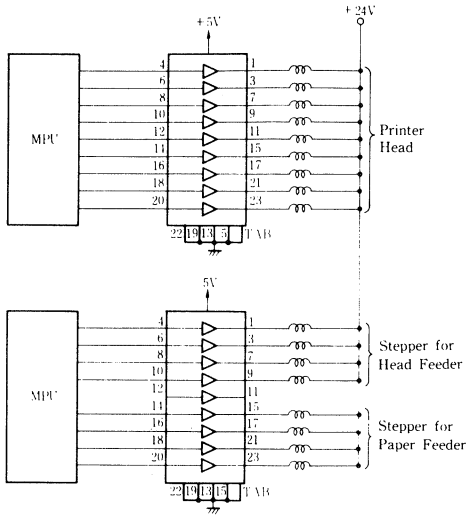
Where drive period is defined as T.

And power dissipation (P_T) when driving 9 channels at the same time;

$$P_T = \frac{9}{T} (P_{on} \cdot t_{on} + P_{sus} \cdot t_{sus}) \quad \cdots\cdots (6)$$

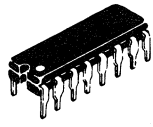
APPLICATION

- Dot Printer



HA13415 ● Quad. Solenoid Driver

The HA13415, a monolithic power IC, is a driver for inductive loads.
Packaged in Dual-in-Line 16 pin, contains four driving circuits of 0.6A.
Each driver has OCSD circuit to protect the IC from the short circuit of loads, and is best suited for drivers of solenoid, relay and stepping motors.



(DP-16C)

■ FUNCTIONS

- 0.6A Quad Driver
- With Clamp Diode
- With Chip Enable
- With OCSD (Over Current Shutdown)
- With Low Voltage Inhibit

■ FEATURES

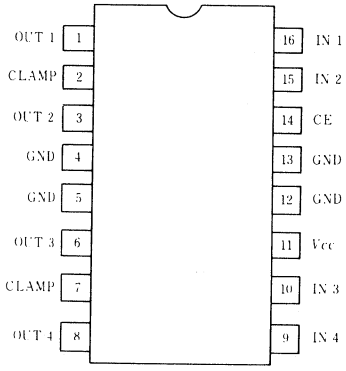
- High Sustaining Voltage (50V)
- Low Saturation Voltage
- Compatible with TTL
- Low Input Current

■ ABSOLUTE MAXIMUM RATINGS (Ta=25℃)

Item	Symbol	Ratings	Units	Note
Supply Voltage	V_{CC}	0.5 to 6	V	1
Input Voltage	V_{IN}	0.5 to 6	V	
Output Voltage	V_{out}	50	V	
Output Current	I_O	0.6	A	
Power Dissipation	P_T	2.0	W	2
Junction Temperature	T_j	150	℃	
Operating Junction Temperature Range	T_{opr}	40 to +125	℃	
Storage Temperature Range	T_{stg}	55 to +150	℃	

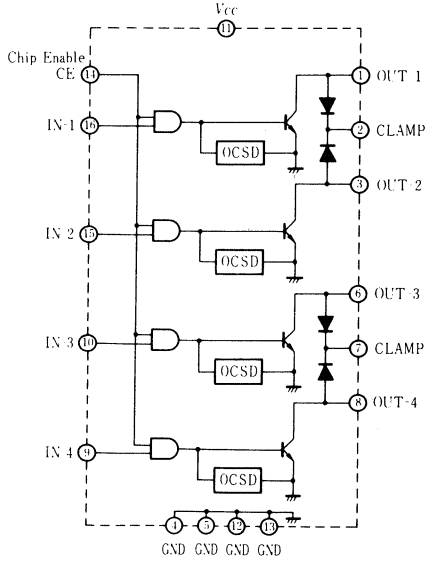
Notes 1. Recommended Operating Voltage
V_{CC} 5V ± 10% 4.5 to 5.5V
2. Thermal Resistances are follows.
$\theta_{j\text{-}a1} \leqq 60$℃/W (Soldered on a print circuit board.)
$\theta_{j\text{-}a2} \leqq 35$℃/W (Soldered on a print circuit convered with copper sufficiently.)
$\theta_{j\text{-}a3} \leqq 15$℃/W (Soldered on pin 4, 5, 12, and 13 with an infinity heat sink.)

■ PIN ARRANGEMENT



(Top View)

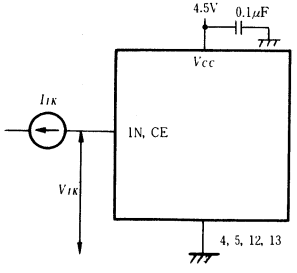
■ BLOCK DIAGRAM



■ ELECTRICAL CHARACTERISTICS (Ta=25℃, V_{CC}=5V)

Item	Symbol	Test Conditions		min	typ	max	Units	Note
Supply Current	I_{CC}	CE=0.8V		–	6	–	mA	
		CE=IN=2.0V		–	60	80	mA	
Low Level Input Voltage	V_{IL}			0	–	0.8	V	
High Level Input Voltage	V_{IH}			2.0	–	–	V	
Low Level Input Current	I_{IL}	V_I=0.8V		−10	–	10	μA	
High Level Input Current	I_{IH}	V_I=2.0 to 5V		−10	–	10	μA	
Input Clamp Voltage	V_{IK}	I_{IK}=−12mA		–	−1.0	−1.5	V	1
Low Level Output Voltage	V_{OL}	I_O=0.3A		–	0.20	0.4	V	
		I_O=0.6A			0.40	0.7		
Output Leakage Current	I_{CEX}	V_{CE}=50V				100	μA	
Clamp Diode Forward Voltage	V_F	I_F=0.4A			1.1		V	
		I_F=0.8A			1.3			
Clamp Diode Reverse Current	I_R	V_R=50V				100	μA	
Turn On & Turn Off Delay	t_{pHL}	V_L=17V, R_L=56Ω	for IN		0.2		μs	
			for CE		0.4			
	t_{pLH}	V_L=17V, R_L=56Ω	for IN		1.0		μs	
			for CE		1.5			
Negative Output Current Test		I_O=−100mA						2
Output Short Test		V_L=5.5V, R_L=3.5Ω						3
Capacitive Load Test		V_L=17V, R_L=27Ω, C_L=0.01μF						4
Solenoid Survival Test		V_L=32V, R_L=56Ω, L_L=250mH						5

Notes) 1. See Fig. 1.
2. Test Procedures are
(1) V_{CC}=5.5V
(2) Set all outputs "ON" with I_O=250mA per output, then set I_O=−100mA for one output. All remaining outputs shall remain "ON".
(3) Set all outputs "OFF" then set I_O=−100mA for one output. Each remaining Output shall not conduct more than 30mA.
(4) Perform test for each output.
3. See Fig. 2.
4. See Fig. 3.
5. See Fig. 4.



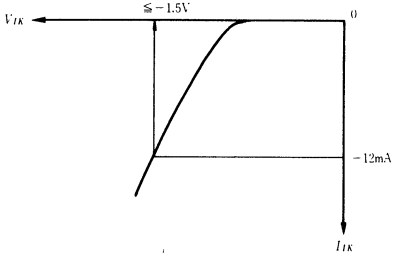
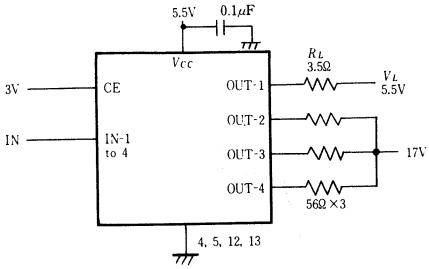


Fig. 1 Input Clamp Voltage

● Measure at pins 9, 10, 14, 15, 16.



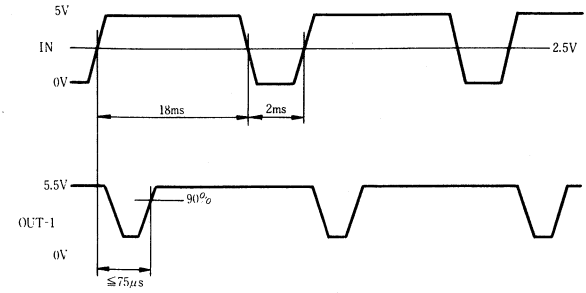
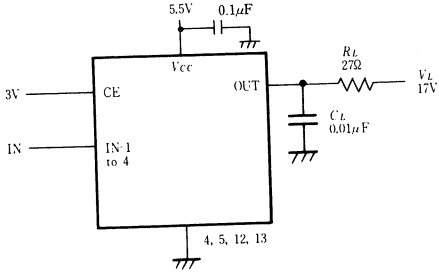


Fig. 2 Output Short Test

- Each unshorted output shall turn ON with IC = 300mA per channel.
- Perform test for each output.



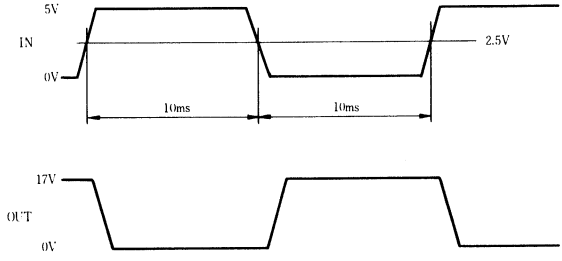
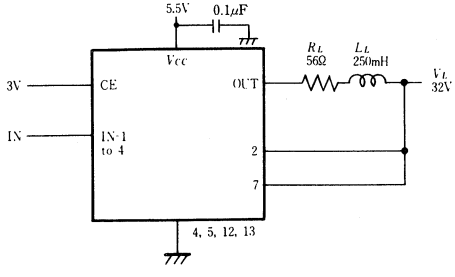


Fig. 3 Capacitive Load Test

- OCSD shall not become enabled and limit I_C or disable the output being tested during the cycling.
- Test each output, one ON at a time.



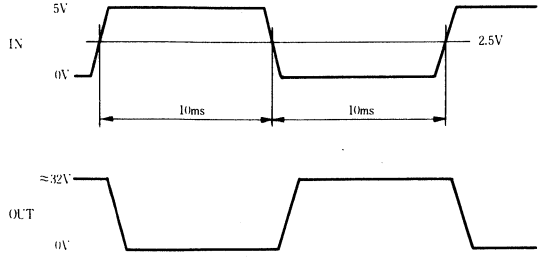


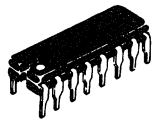
Fig. 4 Solenoid Survival Test

- Each output "ON" and "OFF"
- Test one output each time.

HA13421A,HA13421AMP ● Dual Bridge Drivers

HA13421A and HA1342AMP are monolithic power ICs, dual bridge drivers. The maximum driving current and voltage are 0.33A x 12V per bridge. Therefore, this value finds best use in the 2 phase bipolar stepping motor driving to head actuater of 3 to 5¼ inch FDD.

HA13421A



(DP-16A)

HA13421AMP

(MP-18)

■ FEATURES

- 330mA Output Current Capability
- Dual Bridge Included
- With Power Save
- Single – Input Direction Control
- Low Output Saturation Voltage
- Low Supply Current
- Low Input Current
- Compatible with TTL, LSTTL & 5V CMOS
- With Thermal Shutdown

■ ABSOLUTE MAXIMUM RATINGS (Ta=25°C)

Item	Symbol	HA13421A	HA13421AMP	Unit	Note
Logic Stage Supply Voltage	V_{CC}	7	7	V	1
Seeking Supply Voltage	V_{S1}	15	15	V	1
Holding Supply Voltage	V_{S2}	7	7	V	1
Input Voltage	V_I	0 to V_{CC}	0 to V_{CC}	V	
Peak Seeking Current	I_O (peak)	500	500	mA	2
Seeking Current(DC)	I_{OS}	330	330	mA	
Holding Current(DC)	I_{OH}	200	200	mA	
Power Dissipation	P_T	2.0	1.0	W	3
Junction Temperature	T_j	150	150	℃	
Operating Junction Temperature Range	T_{opr}	−20 to +125	−20 to +125	℃	
Storage Temperature Range	T_{stg}	−55 to +125	−55 to +125	℃	

Notes 1) Recommended Operating Voltage

	MIN	TYP	MAX	UNIT
V_{CC}	4.5	5.0	5.5	V
V_{S1}	10.2	12.0	13.8	V
V_{S2}	4.5	5.0	5.5	V

2) t≦5 ms

3) Thermal Resistances are as follows.

● HA13421A

θ_{j-a1}≦60°C/W (Soldered on a print circuit board)

θ_{j-a2}≦35°C/W (Soldered on a print cicuit covered with copper sufficiently)

θ_{j-a3}≦15°C/W (Soldered on pin 4,5, 12 and 13 with an infinity heatsink)

● HA13421AMP

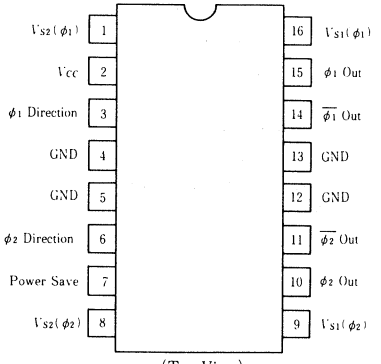
θ_{j-a1}≦120°C/W (Soldered on glass epoxy circuit board with 10% printing)

θ_{j-a2}≦100°C/W (Soldered on glass epoxy circuit board with 30% printing)

θ_{j-a3}≦80°C/W (Soldered on a metal based circuit board)

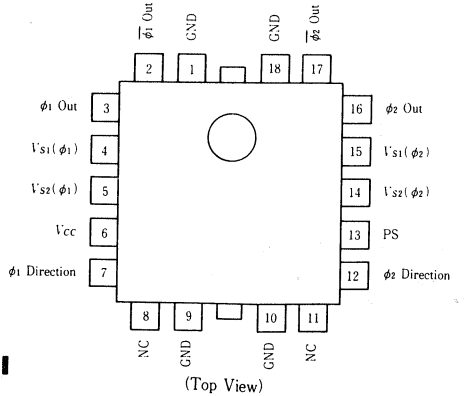
■ PIN ARRANGEMENT

● HA13421A



(Top View)

● HA13421AMP



(Top View)

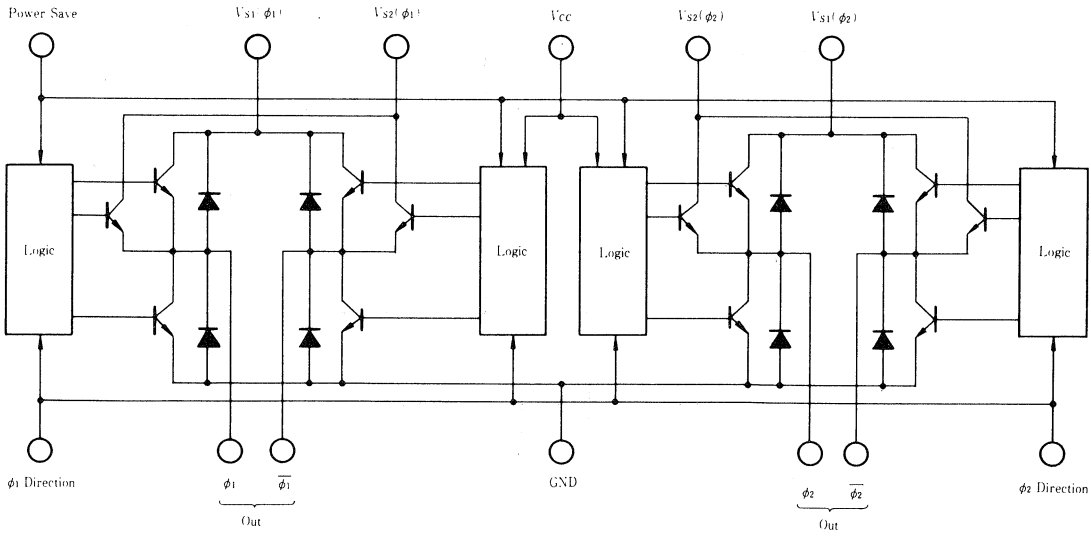
HITACHI

■ ELECTRICAL CHARACTERISTICS (Ta=25℃, V_{CC}=5V, V_{S2}=5V, V_{S1}=12V)

Item	Symbol	Test Condition		min	typ	max	Unit	Note
Input Low Voltage	V_{IL}			---	---	0.8	V	
Input High Voltage	V_{IH}			2.0	---	---	V	
Input Low Current	I_{IL}	V_I=0.8V		---	---	±10	μA	
Input High Current	I_{IH}	V_I=2V		---	1.0	±10	μA	
Input High Current	I_{IH}	V_I=5.5V		---	0.5	1.0	mA	
Supply Current		PS=0.8V, I_O=0	V_{CC}	---	25	33	mA	
			V_{S1}	---	10	20	mA	1
			V_{S2}	---	---	1.0	mA	2
		PS=2V, I_O=0	V_{CC}	---	25	33	mA	
			V_{S1}	---	3	5	mA	1
			V_{S2}	---	5	10	mA	2
Output TRS Breakdown Voltage	BV_{CER}	I_C=10mA		18	---	---	V	
V_{S1} Saturation Voltage	$V_{CE(sat)1}$	PS=0.8V, I_O=330mA		---	1.5	2.0	V	3
V_{S2} Saturation Voltage	$V_{CE(sat)2}$	PS=2.0V, I_O=130mA		---	1.5	2.0	V	3
Clamp Diode Forward Voltage	V_F	I_F=330mA	Upper	---	5	---	V	
			Lower	---	1.5		V	
Delay Time	t_{PLH}	I_O=330mA		---	1.0	5	μs	
Delay Time	t_{PHL}	I_O=330mA		---	1.0	5	μs	

Note 1 The specification indicates the sum of $V_{S1}(\phi_1)$ & $V_{S1}(\phi_2)$ current.
Note 2 The specification indicates the sum of $V_{S2}(\phi_1)$ & $V_{S2}(\phi_2)$ current.
Note 3 The specification indicates the sum of Upper & Lower saturation voltages.

■ BLOCK DIAGRAM



■ TRUTH TABLE

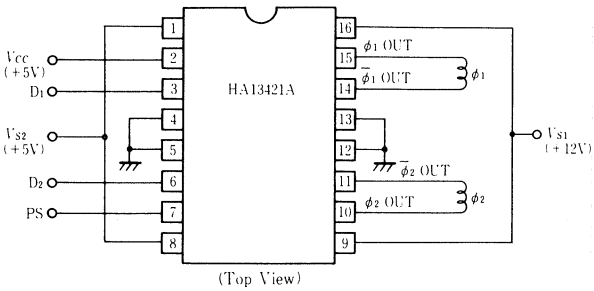
● For Each Bridge

Power Save	Direction	ϕ—Out	$\bar{\phi}$—Out
L	L	L	H^+
L	H	H^+	L
H	L	L	H^-
H	H	H^-	L

L =Low Voltage State
H^+=High Voltage State (Seeking TRS On)
H^-=High Voltage State (Holding TRS On)

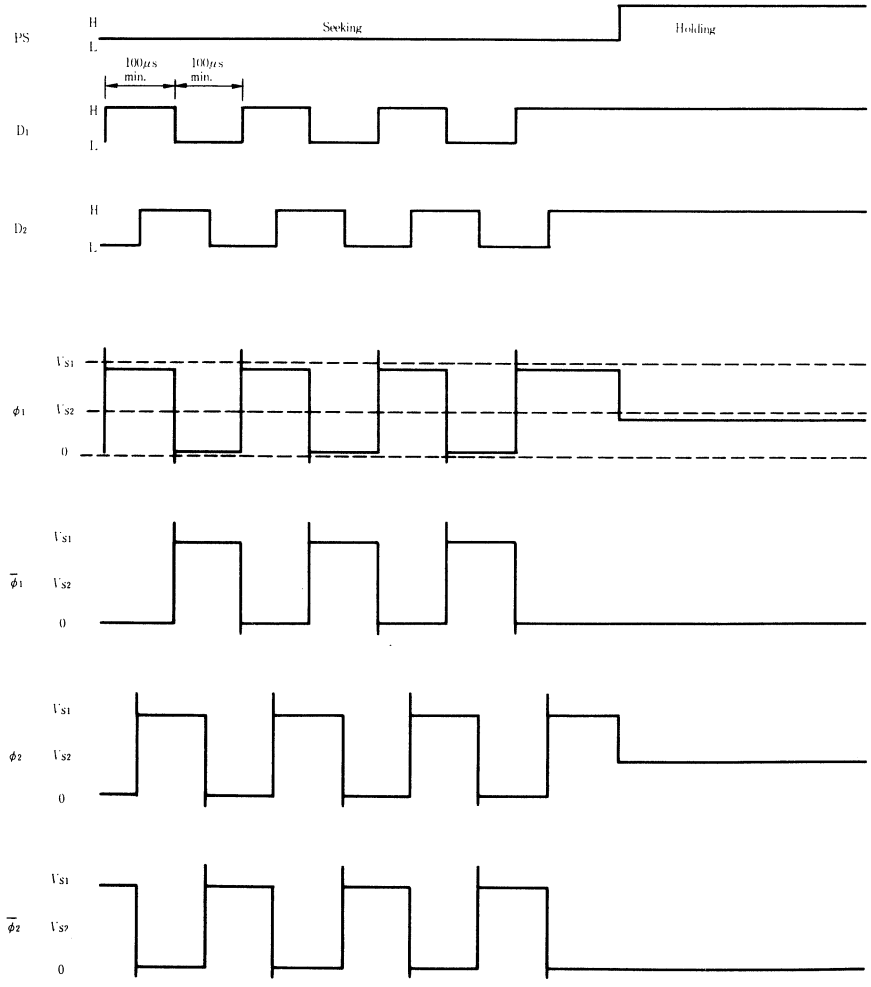
■ APPLICATION

2-phase Bipolar Stepping Motor Drive Circuit



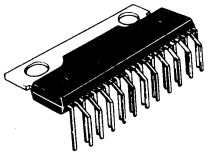
(Top View)

■ TIMING CHART



HA13426 ● Three-phase Motor Driver with Speed Discriminator

HA13426 is a power IC with a speed discriminator for the three-phase brushless motor driving of 5 ¼ inch-HDD (Hard Disk Drive). It is possible to construct a servo system with quartz resonator, requiring fewer external components. Especially EMI noise from motor driver is depressed because of a voltage drive system.

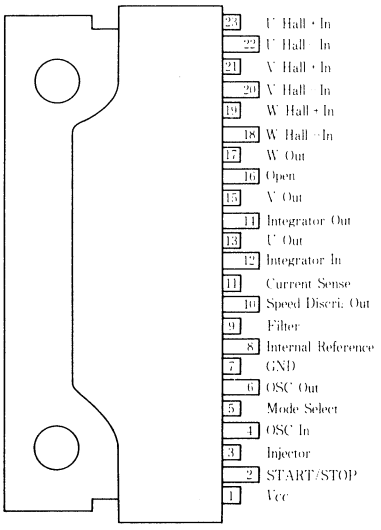


(SP-23TA)

■ FEATURES

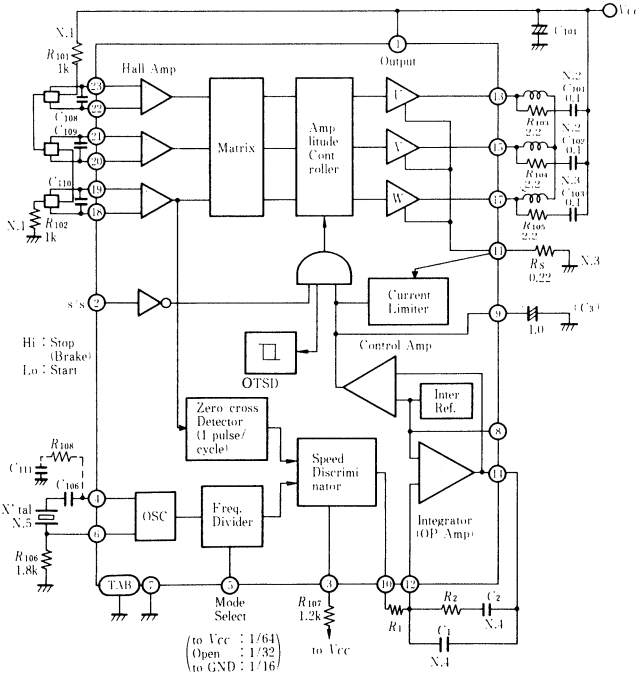
- Possible to construct a servo system on a single chip
- Large output current (3A)
- Require no adjustment because of digital servo system
- The voltage drive system (not supply voltage control) achieves almost no spike voltage at commutating, caused EMI (Electro-Magnetic Interference) conventionally.
- The START/STOP terminal of TTL level is attached.
- Load-short brake at STOP mode
- Maximum current at starting is depressed by the built-in current limiter.
- Wide selection for quarts resonator is permitted because of frequency divider.

■ PIN ARRANGEMENT



(Top View)

■ BLOCK DIAGRAM



■ ABSOLUTE MAXIMUM RATINGS (Ta=25℃)

Item	Symbol	Ratings	Unit	Note
Supply Voltage	V_{CC}	15	V	1
Input Voltage	V_{IN}	0 to V_{CC}	V	2
Output Current	I_O	3	A	
Power Dissipation	P_T	25	W	3
Junction Temperature	T_j	150	℃	
Operating Junction Temperature Range	T_{jop}	−20 to +125	℃	
Storage Temperature Range	T_{stg}	−55 to +125	℃	

Note) 1. Recommended operating voltage
V_{CC} = 12V ± 15% (10.2V to 13.8V)
2. Applied to Hall Amp, mode select input.
Maximum Input Voltage at start/stop is 6V.
3. Thermal Resistance
$\theta_{j\text{-}c} \leqq 3$℃/W
$\theta_{j\text{-}a} \leqq 40$℃/W

■ ELECTRICAL CHARACTERISTICS (Ta=25℃, V_{CC}=12V)

Item		Symbol	Test Condition	min	typ	max	Unit	Note
Total	Supply Current	I_{SO}	S/S=2.0V		50	70	mA	
		I_S	S/S=0.8V, R_L=Open		55	75	mA	
	Over Temperature Protection	T_{sd}	Shutdown		150		℃	
		T_{hys}	Hysteresis		20		℃	
Hall Amp	Input Bias Current	I_{HB}	V_H=6.0V		2	10	μA	
	Input Common Mode Voltage Range	V_H		2.0		10	V	
	Voltage Gain	G_{VH}			10		dB	
Output Stage	Quiescent Output Voltage	V_Q		5.3	5.9	6.5	V	
	Difference Between Phase	$\triangle V_Q$				±0.3	V	
	Saturation Voltage	$V_{CE(sat)}$	I_O=2A		2.4	3.2	V	1
	Output Impedance	R_O	I_O=0.4A		0.2		Ω	
Control Amp	Internal Ref. Voltage	V_{ref}		3.0	3.2	3.4	V	
	Voltage Gain (CTL Amp to Output)	G_{CTL}		21	24	27	dB	
	Difference of Gain	$\triangle G_{CTL}$				±2	dB	
Integrator	Input Bias Current	I_B				±0.1	μA	
	Output Voltage Swing	A	I_O=0.3mA		0.7		V	
		A	I_O=−0.3mA		0.7		V	

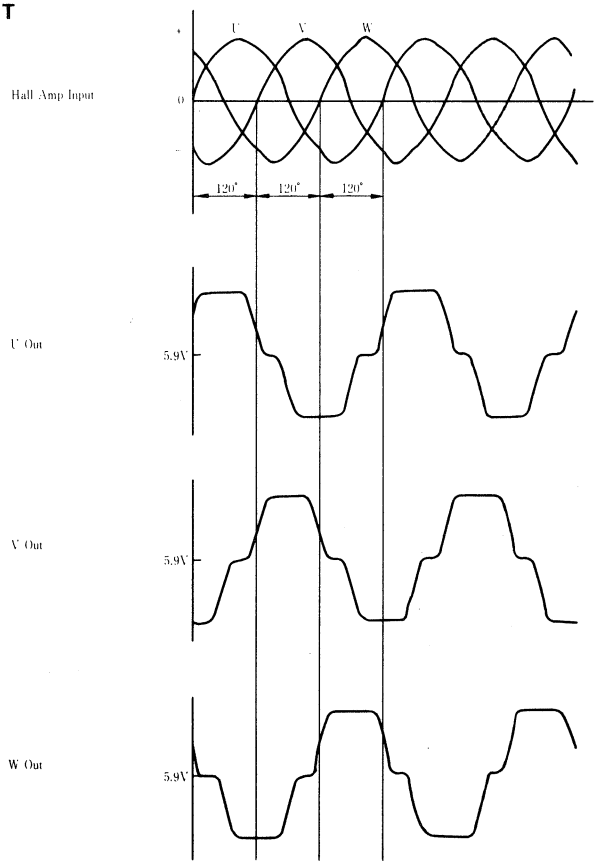
Note) 1. Sum of upper and lower TRS saturation voltages

to be continued

■ ELECTRICAL CHARACTERISTICS (Ta=25℃, V_{CC}=12V)

Item		Symbol	Test Condition	min	typ	max	Unit	Note
Speed Discriminator	Output Voltage Swing	V_{OH}	I_O=0.3mA	5.8	6.1	—	V	
		V_{OL}	I_O=−0.3mA	—	—	0.2	V	
	Cutoff Current	I_{off}	Charge Pump Off State	—	—	±0.1	μA	
	Operating Frequency	f_{CLK}		60	—	250	kHz	
	Count Number	N		—	1024	—		
Start Stop	Input High Voltage	V_{IH}	Stop	2.0	—	—	V	
	Input Low Voltage	V_{IL}	Start	—	—	0.8	V	
	Input High Current	I_{IH}	V_H=2.0V	—	−0.15	−0.5	mA	
	Input Low Current	I_{IL}	V_L=0.8V	—	−0.2	−0.5	mA	
Current Limiter	Reference Voltage			0.52	0.56	0.60	V	
Mode Select	1 16 Division Input Voltage	$V_{I\ 16}$		—	—	0.8	V	
	1 32 Division Input Voltage	$V_{I\ 32}$	Open	—	6.3	—	V	
	1 64 Division Input Voltage	$V_{I\ 64}$		11.2	—	—	V	
	1 16 Division Input Current	$I_{I\ 16}$	V_{IN}=0V	—	−0.63	−1.3	mA	
	1 64 Division Input Current	$I_{I\ 64}$	V_{IN}=12V	—	1.0	1.5	mA	
Oscillator	Operating Frequency	f_{osc}		—	—	8.0	MHz	

■ TIMING CHART



■ EXTERNAL COMPONENTS

Parts No.	Recommended Value	Function	Note
R_{101} R_{102}	1kΩ	Hall Elements Bias	1
R_{103} R_{104} R_{105}	2.2Ω (0.5W)	Stability	
R_{106}	1.8kΩ	OSC Bias	6
R_{107}	1.2kΩ	Speed Descri. bias	
R_{108}	470Ω	Stability	6
R_1, R_2	See Application	Integral Constant	
R_S	—	Current Sense	3
C_{101} C_{102} C_{103}	0.1μF	Stability	2
C_{104}	≧0.1μF	V_{CC} By-passing	
C_{106}	10pF	AC Coupling OSC	
C_{108}, C_{109} C_{110}	≧0.01μF	Stability	
C_{111}	4700pF	Stability	6
C_1, C_2	See Application	Integral Constant	4
C_3	See Application	Filter Constant	
X'tal	—	Resonator	5

Notes) 1. Set R_{101} and R_{102} at which output voltage of more than 50mVpp is applied to hall elements.

2. Use C_{101} to C_{103} which cause no 2nd resonance.
And connect the middle points of C_{101}, C_{102} and C_{103} to the most stable one of those of V_{CC}, GND the middle point of coil.
(Requring to use non-polar in case of connecting them to the middle point of coil.)

3. Output current is limited as shown below by RS valve.

$$I_{out} = \frac{0.56(V) \pm 10\%}{R_S(\Omega)}$$

For example, output current is limited to 2.55(A) ±10% at Rs 0.22Ω.

4. Need to use non-polar as to C_1 and C_2.

5. The relationship between Crystal Oscillation frequency, f_{OSC} and the number of rotation, N is as follows.

$$N = \frac{60}{512} \cdot \frac{m \cdot f_{OSC}}{P} \text{ (rpm)}$$

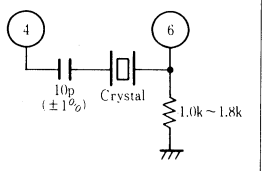
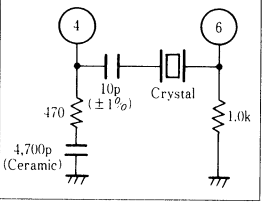
Where P is the number of pole of motor, and m is the division ratio of Frequency Divider and the latter is set at the following values by the voltage applied to Mode Select.

Mode Select	m
to GND	1/16
Open	1/32
to V_{CC}	1/64

For instance, the relationship between Mode Select and f_{OSC} to rotate a 4-pole motor at 3600 rpm as shown below.

Mode Select	f_{OSC} (MHz)
to GND	1.96608
Open	3.93216
to V_{CC}	7.86432

6. Determine external components of Oscillator as shown below in accordance with the frequency range.

1.0MHz≦f_{OSC}≦4.0MHz	4.0MHz≦f_{OSC}≦8.0MHz
	

■ HOW TO USE THE HA13426/431/432/432MP

1. Selection of Resonator

1.1 In HA13426

The oscillating frequency at synchronous, f_{OSC} and the number of motor rotation N have a relationship shown below.

$$N = \frac{60}{512} \cdot \frac{m \cdot f_{OSC}}{p} \text{ (rpm)} \quad \ldots\ldots\ldots\ldots\ldots\ldots \quad (1)$$

where, the p is the number of motor poles and m is the dividing ratio of a divider. For the m, one of the following values is selected according to applied voltage at the mode select pin.

Mode Select	m
to GND	1/16
Open	1/32
to V_{CC}	1/64

For example, the values of f_{OSC} to rotate 4-poles motor with 3600 rpm are;

Mode Select	f_{OSC} (MHz)
to GND	1.96608
Open	3.93216
to V_{CC}	7.86432

1.2 In HA13431/432/432MP

The oscillating frequency at synchronous, f_{OSC} and the FG frequency, f_{FG} have a relationship shown below.

$$f_{FG} = \frac{m \cdot f_{OSC}}{1024} \quad \ldots\ldots\ldots\ldots\ldots\ldots \quad (2)$$

where, m is the dividing ratio of a divider and takes one of the following values according to the applied voltage at the mode select pin.

Mode Select	m
to GND	1
Open	1/2
to V_{CC}	1/4

2. How to Determine the Integral Constants R_1, R_2, C_1 and C_2, and the Filter Constant C_3

2.1 Block Diagram

Fig. 1 is the block diagram showing motor speed control by the HA13426/431/432/432MP. The part enclosed by dotted lines denotes the IC, and the $G_1(S)$ and the $G_2(S)$ indicate the transfer functions of an integrator and from control amp to output, respectively. Since these IC's are driven by voltage, items of the motor coil impedance and the kick-back voltage are contained in the loop.

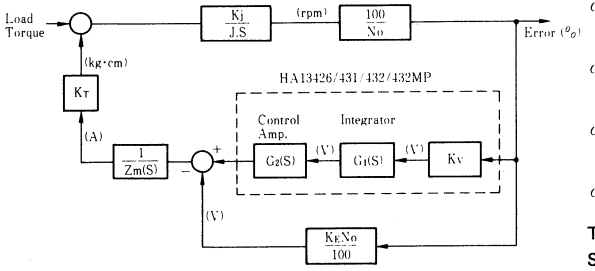


Fig. 1 Block Diagram

Kj = Transfer constant, 9.55
K_T = Torque constant (kg•cm/A)
K_E = Kick-back constant (V/rpm)
K_V = Speed discriminator gain (V/%)
J = Moment of inertia (kg•cm•sec^2)
Zm(S) = Motor coil impedance (Ω)
$G_1(S)$ = Transfer function of an integrator
$G_2(S)$ = Transfer function from control amp to output
No = Standard number of rotation

2.2 Resolution

In the Fig. 1, when

$$A(S)=\frac{K_j}{J\cdot S}\cdot\frac{100}{N_O} \quad \cdots\cdots(3)$$

$$\beta(S)=\frac{K_T}{Z_m(S)}\left(K_V\cdot G_1(S)\cdot G_2(S)-\frac{K_E\cdot N_O}{100}\right)\cdots(4)$$

the Fig. 1 can be shown as Fig. 2.

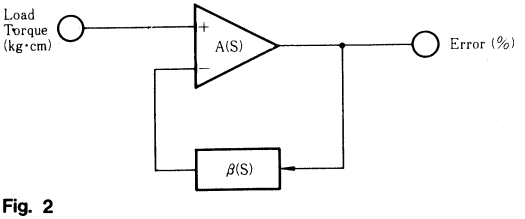


Fig. 2

On the other hand, the Zm(S), $G_1(S)$ and $G_2(S)$ are expressed as follows;

$$Z_m(S)=R_m(1+S/\omega_m) \quad \cdots\cdots(5)$$

$$G_1(S)=\frac{R_2}{R_1}\cdot\frac{1+\omega_2/S}{1+S/\omega_1} \quad \cdots\cdots(6)$$

$$G_2(S)=\frac{G_{CTL}}{1+S/\omega_3} \quad \cdots\cdots(7)$$

Then,

$$\omega_m=\frac{R_m}{L_m} \quad \cdots\cdots(8)$$

$$\omega_1=\frac{1}{C_1R_2} \quad \cdots\cdots(9)$$

$$\omega_2=\frac{1}{C_2R_2} \quad \cdots\cdots(10)$$

$$\omega_3=\frac{1}{C_3R_3} \quad \cdots\cdots(11)$$

The G_{CTL} and the R_3 are the internal constant of IC's. Substituting the equations (5) to (11), to the equation (4), $\beta(S)$ is;

$$\beta(S)=\frac{K_T}{R_m(1+S/\omega_m)}\left(\frac{R_2K_VG_{CTL}(1+\omega_2/S)}{R_1(1+S/\omega_1)(1+S/\omega_3)}-\frac{K_EN_O}{100}\right)$$

$$=\frac{R_2K_TK_VG_{CTL}}{R_1R_m}\cdot\frac{1+\omega_2/S}{(1+S/\omega_m)(1+S/\omega_1)(1+S/\omega_3)} \quad \cdots\cdots(12)$$

$$\left(\because\frac{R_2K_VG_{CTL}}{R_1}\gg\frac{K_EN_O}{100}\right)$$

To control speed with stability, A(S) and $\beta(S)$ are required to have a relationship shown in Fig. 3. That is, the angular frequency of the cross point of A(S) and $\beta(S)$, ω_0 should be put between the angular frequency of an integrator, ω_1 and ω_2.

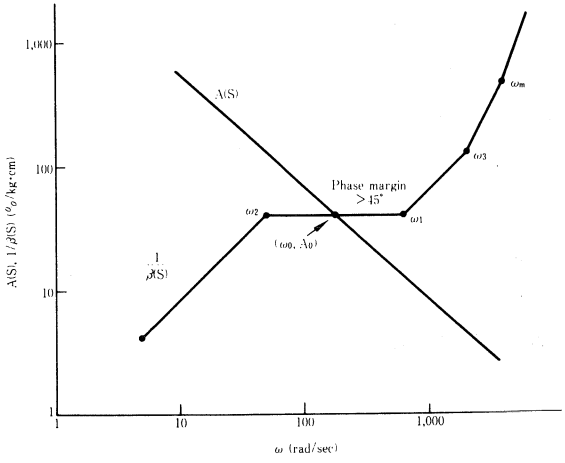


Fig. 3 Stable Relationship of A(S) and $\beta(S)$

2.3 Design Procesure of the R_1, R_2, C_1, C_2 and C_3

(1) Determining the ω_0

The ω_0 uses the value of 1/10 to 1/30 of the ω_m or the angular frequency of FG, ω_{fG} which is the lower. In HA13426, the angular frequency of the hall signal is used for ω_{fG}, and the ω_0 is the value of 1/30 to 1/100 of the ω_{FG}'.

(2) Calculating the Ao

From the equation (3)

$$A_O = \frac{K_j}{J \cdot \omega_0} \cdot \frac{100}{N_O} \quad \cdots\cdots (13)$$

(3) Designing R_1 and R_2

From the Fig. 3 and the equation (12),

$$\frac{R_2}{R_1} = \frac{R_m}{K_T \cdot K_V \cdot G_{CTL} \cdot A_O} \quad \cdots\cdots (14)$$

Each IC is designed to take the following Kv and G_{CTL}.

Type	Kv (V/%)	G_{CTL} (V/V)
HA13426	0.03	16 typ
HA13431	0.023	16 typ
HA13432/MP	0.023	8 typ

Small R_1 increases the C_1 and C_2 and large R_1 will cause speed error by the cutoff current of the speed discriminator and the input bias current of the integrator. Values of 10k ohms to 56k ohms are recommended.

(4) Determining ω_1, ω_2 and ω_3

Will be determined as follows

$$\omega_1 \geqq 3\,\omega_0$$
$$\omega_2 \leqq \omega_0/3$$
$$\omega_3 \geqq 3\,\omega_0$$

(5) Designing C_1, C_2, C_3

From the equations (9), (10), (11),

$$C_1 = 1/\omega_1 R_2$$
$$C_2 = 1/\omega_2 R_2$$
$$C_3 = 1/\omega_3 R_3$$

where the R_3 is designed to be 2.2k ohms.

3. When Using the External Clock

As shown in Fig. 4, external clock can be provided at the OSC input pin. But, applying too large input causes the miss-operation of IC's, the following resistor, Rs must be connected in series to control the current.

(1) In HA13426

$$R_S \geqq 2.5(V_{IH} - 1.4) - 1.5 \quad (k\Omega)$$
$$R_S \leqq 7.5(1.4 - V_{IL}) - 1.5 \quad (k\Omega)$$

A speeding-up capacitor parallel to Rs should be considered.

(2) In HA13431/432/432MP

$$R_S \geqq 3.7(V_{IH} - 1.7) - 2 \quad (k\Omega)$$
$$R_S \leqq 1.0(1.7 - V_{IL}) - 2 \quad (k\Omega)$$

Then, the input current I_{IH} and I_{IL} are restricted as follows and the external clock must have larger driving capacity.

$$I_{IH} = \frac{V_{IH} - 1.4}{R_s + R_i} \quad (mA)$$

$$I_{IL} = -\frac{1.4 - V_{IL}}{R_s + R_i} \quad (mA)$$

where, the Ri is the input resistance of the OSC and is 1.5k ohms in HA13426 or 2k ohms in the others.

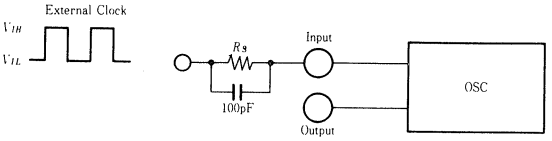


Fig. 4 Providing External Clock

4. Producing the Ready Signal

As shown in the Fig. 5, external comparator can produce the ready signal. Since the DC gain is extremely high (70dB or more), the rotation error, ΔN when the ready signal V_R becomes high is determined by the accuracy of the speed discriminator without the influence of the window of a comparator.

Open collector output type comparators are recommended.

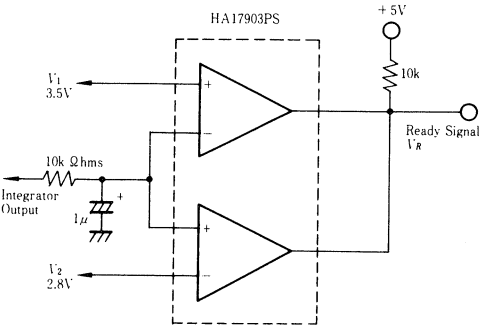
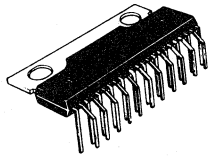


Fig. 5 Producing the Ready Signal

HA13431 ●Three-phase Motor Driver with Speed Discriminator

HA13431 is a monolithic power IC with a speed discriminator for the three-phase brushless DC motor driving of 5¼ inch FDD. It is possible to construct a servo system with quartz or ceramic resonator by fewer external components. Especially EMI noise from motor driver is depressed because of a voltage drive system.

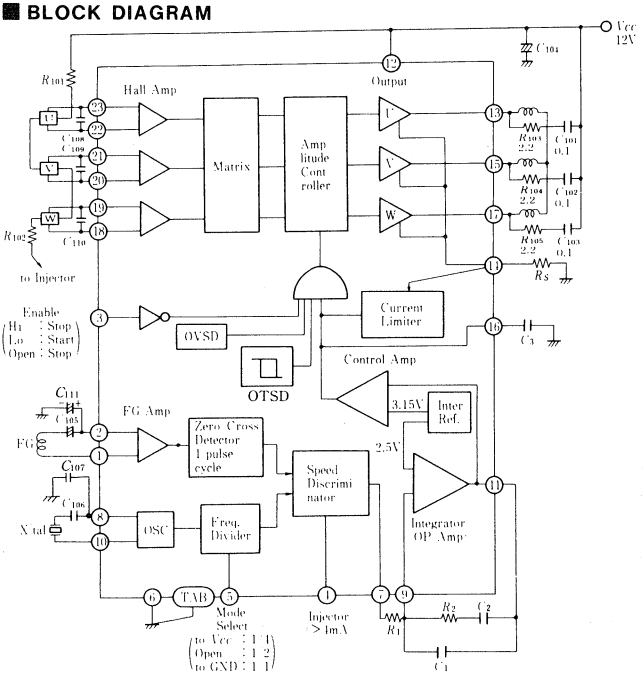


(SP-23T)

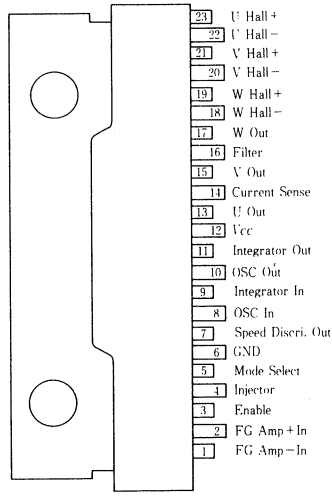
■ FEATURES

- Possible to construct a servo system on a single chip
- Require no adjustment because of digital servo system
- The voltage drive system (not supply voltage control) achieves almost no spike voltage at commutating, caused EMI conventionally.
- The Enable terminal of TTL level is attached, and the current at the stop mode is less than 0.5mA
- Maximum current at starting is depressed by the built-in current limiter.
- Wide selection for quartz & ceramic resonator is permitted because of frequency divider

■ BLOCK DIAGRAM



■ PIN ARRANGEMENT



(Top View)

■ ABSOLUTE MAXIMUM RATINGS (Ta=25℃)

Item	Symbol	Ratings	Unit	Note
Supply Voltage	V_{CC}	20	V	1
Input Voltage	V_{IN}	0 to V_{CC}	V	2
Output Peak Current	I_O (peak)	1.5	A	
Output Current	I_O	1.0	A	
Power Dissipation	P_T	10	W	3
Junction Temperature	T_j	150	℃	
Operating Junction Temperature Range	T_{opr}	−20 to +125	℃	
Storage Temperature Range	T_{stg}	−55 to +125	℃	

Notes) 1. Recommended operating voltage
V_{CC} = 12V±15% (10.2V to 13.8V)
2. Applied to Hall Amp, start stop and mode select input.
3. Thermal Resistances are as follows.
$\theta_{j-c} \leqq 3$℃/W
$\theta_{j-a} < 40$℃/W

■ ELECTRICAL CHARACTERISTICS (Ta=25℃, V_{CC}=12V)

Item		Symbol	Test Condition	min	typ	max	Unit	Note
Total	Quiescent Current	I_Q	Enable=2.0V	—	0.2	0.5	mA	
			Enable=0.8V, R_L : Open	—	24	31	mA	
	Over Voltage Shutdown	V_{sd}	Shutdown Voltage	15	16	17	V	
		V_{hys}	Hysteresis	0.5	0.8	1.2	V	
	Over Temperature Protection	T_{sd}	Shutdown	—	150	—	℃	
		T_{hys}	Hysteresis	—	25	—	℃	
Hall Amp	Input Bias Current	I_{HB}	V_H=6.0V	—	1.0	5	μA	
	Input Common Mode Voltage Range	V_H		1.5	—	10.5	V	
	Voltage Gain	G_{VH}		—	10	—	dB	
Output Stage	Quiescent Output Voltage	V_Q		5.1	5.7	6.3	V	
	Difference of Quiescent Voltage	$\triangle V_Q$		—	—	±0.3	V	
	Saturation Voltage	$V_{CE(sat)}$	I_O=0.7A	—	2.0	2.8	V	1
	Output Impedance	R_O	I_O=0.2A	—	0.3	—	Ω	
Control Amp	Internal Ref. Voltage	V_{REF1}		—	3.15	—	V	
	Voltage Gain (CTL Amp to Output)	G_{CTL}		—	24	—	dB	
	Difference of Gain	$\triangle G_{CTL}$		—	—	±2	dB	
Integrator	Internal Ref. Voltage	V_{REF2}		—	2.5	—	V	
	Input Bias Current	I_{BI}		—	—	±0.1	μA	
	Output Voltage Swing	A_+	I_O = +0.25mA	—	1.3	—	V	
		A_-	I_O = −0.25mA	—	−0.65	—	V	
	Unity Gain Band Width	BW	B_V =0dB	—	0.3	—	MHz	
Speed Discriminator	Injection Voltage	V_J	I_J=6mA	—	0.9	—	V	
	Output High Voltage	V_{OH}	I_O=0.25mA	4.4	4.7	—	V	
	Output Low Voltage	V_{OL}	I_O = −0.25mA	—	0.1	0.2	V	
	Cutoff Current	I_{off}	Charge Pump Off State	—	—	±0.1	μA	
	Count Number			—	1024	—		
Enable	Input High Voltage	V_{IH}	Stop	2.0	—	—	V	
	Input Low Voltage	V_{IL}	Start	—	—	0.8	V	
	Input High Current	I_{IH}	V_H=2.0V	—	—	±10	μA	
	Input Low Current	I_{IL}	V_L=0.8V	—	—	±10	μA	
Current Limiter	Reference Voltage	V_{REF3}		0.36	0.4	0.44	V	
FG Amp	Input Voltage	$V_{IN(FG)}$	f=200Hz	2.0	—	20	mVpp	
OSC	Oscillation Frequency	f_{osc}		0.1	—	1.0	MHz	
Mode Select	No Division Input Voltage	V_{I1}		—	—	0.8	V	
	1/2 Division Input Voltage	V_{I2}	Open	—	6.3	—	V	
	1/4 Division Input Voltage	V_{I4}		10	—	—	V	
	No Division Input Current	I_{I1}	V_{IN}=0V	—	—	−1.0	mA	
	1/4 Division Input Current	I_{I4}	V_{IN}=12V	—	—	1.0	mA	

Note 1) Sum of upper and lower TRS saturation voltages.

■ EXTERNAL COMPONENTS

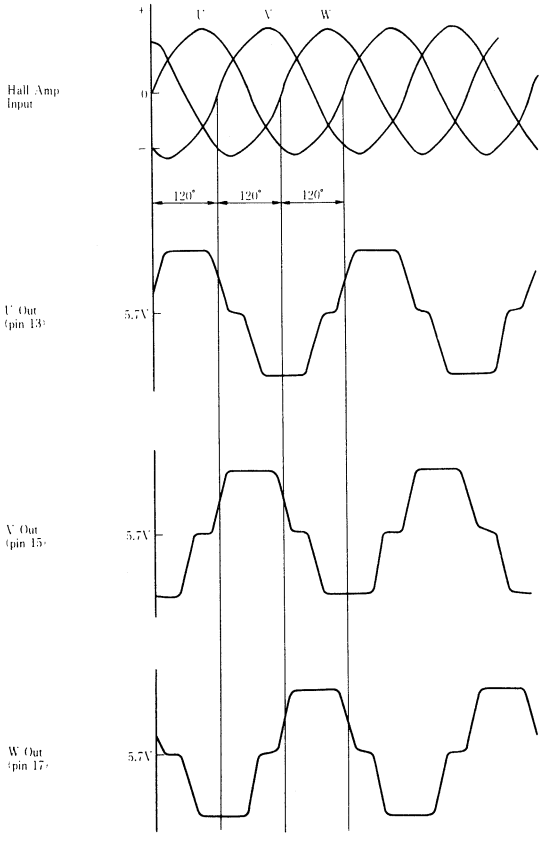
Parts No.	Recommended Value	Function	Note
R_{101}, R_{102}	—	Hall Elements Bias	1
R_{103}, R_{104}, R_{105}	2.2Ω	Stability	
R_S	—	Current Sense	3
R_1, R_2	See Application	Integral Constant	4
C_{101}, C_{102}, C_{103}	0.1μF	Stability	2
C_{104}	≧0.1μF	V_{CC} By−passing	
C_{105}	10μF	AC Coupling FG	
C_{106}	47pF	AC Coupling OSC	
C_{107}	56pF	Stability	
C_{108}, C_{109}, C_{110}	≧0.01μF	Stability	
C_{111}	10μF	Stability	
C_1, C_2	See Application	Integral Constant	4
C_3	See Application	Filter Constant	4
X'tal	See Application	Resonator	4

Notes 1) Set R_{101} and R_{102} at which output voltage of 30 to 100mVpp.
2) Use C_{101} to C_{103} which cause no 2nd resonance.
3) Output current is limited as shown below by Rs value.

$$I_{Out} = \frac{V_{REF3}}{R_S}$$

4) See HA13426.

■ TIMING CHART

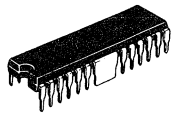


HA13432,HA13432MP

● Three-phase Motor Driver with Speed Discriminator

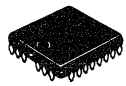
HA13432 and HA13432MP are monolithic power ICs with a speed discriminator for the three-phase brushless DC motor driving of micro or compact FDD. It is possible to construct a servo system with quartz or ceramic resonator, requiring fewer external components.
Especially EMI noise from motor driver is depressed because of a voltage drive system.

HA13432



(DP-24TS)

HA13432MP



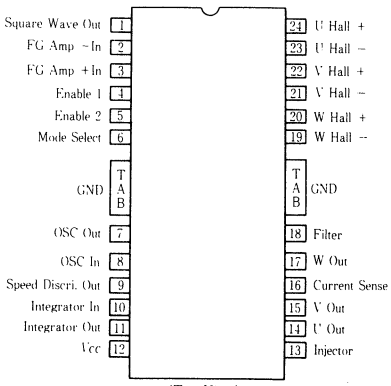
(MP-28)

FEATURES

- Possible to construct a servo system on a single chip
- Require no adjustment because of digital servo system
- The voltage drive system (not supply voltage control) achieves almost no spike voltage at commutating, caused EMI (Electro-Magnetic Interference) conventionally.
- The Enable terminal of TTL level is attached, and the current at the stop mode is less than 0.5mA.
- Maximum current at starting is depressed by the built-in current limiter
- Wide selection for quartz & ceramic resonator is permitted because of frequency divider.

PIN ARRANGEMENT

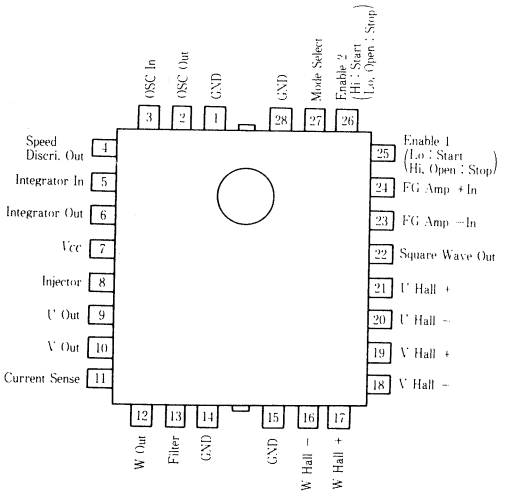
● HA13432



(Top View)

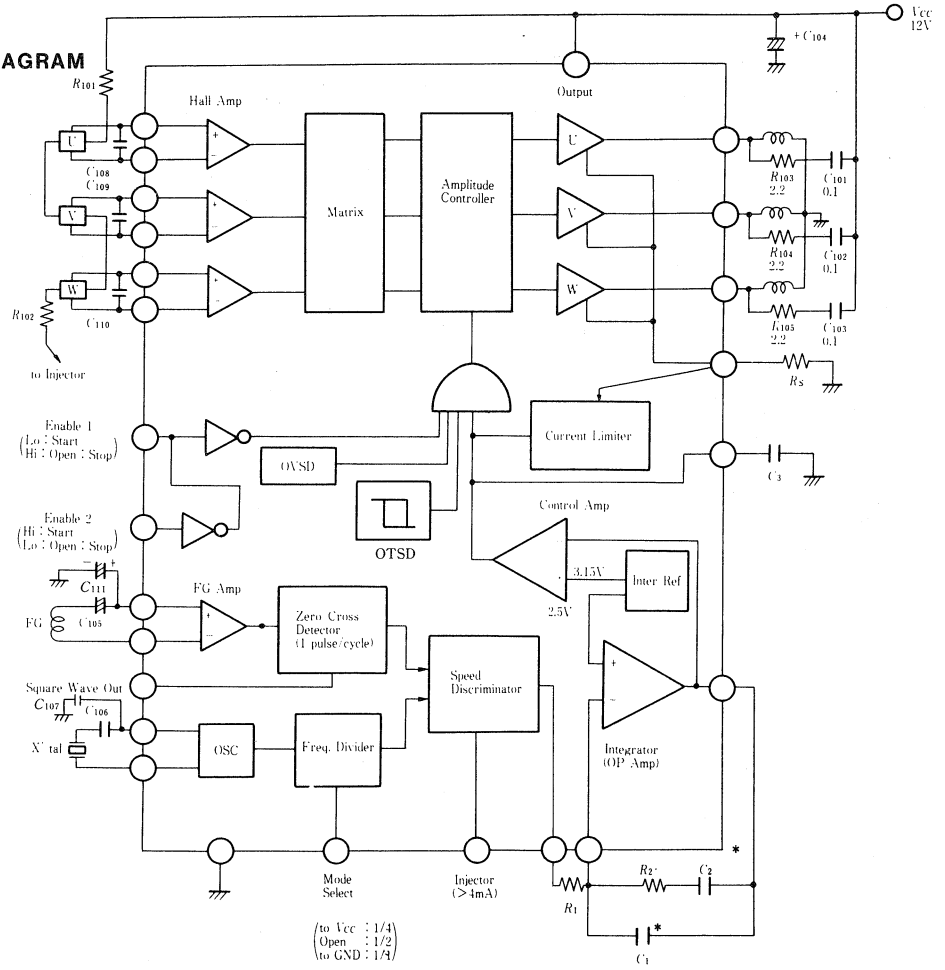
Enable	Hi	Open	Lo
1	Stop	Stop	Start
2	Start	Stop	Stop

● HA13432MP



(Top View)

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS (Ta=25℃)

Item	Symbol	HA13432	HA13432MP	Unit	Note
Supply Voltage	V_{CC}	20	20	V	1
Input Voltage	V_{IN}	0 to V_{CC}	0 to V_{CC}	V	2
Output Peak Current	$I_{O(peak)}$	0.75	0.75	A	
Output Current	I_O	0.5	0.5	A	
Power Dissipation	P_T	2.5	1.5	W	3
Junction Temperature	T_j	150	150	℃	
Operating Junction Temperature Range	T_{jop}	−20 to +125	−20 to +125	℃	
Storage Temperature Range	T_{stg}	−55 to +125	−55 to +125	℃	

Notes) 1. Recommended operating voltage V_{CC} = 12V ± 15% (10.2 to 13.8V)
2. Applied to Hall Amp, start stop and mode select input
3. Thermal Resistances are as follows.

HA13432 : $\theta_{j-c} \leqq 20$℃/W, $\theta_{j-a} \leqq 60$℃/W

HA13432MP : $\theta_{j-a} \leqq 80$℃/W (Soldered on a metal based circuit board)

■ ELECTRICAL CHARACTERISTICS (Ta=25℃, V_{CC}=12V)

Item		Symbol	Test Condition		min	typ	max	Unit	Note
Total	Quiescent Current	I_Q	Enable 1 & 2 Open		—	0.2	0.5	mA	
			Enable 1=0.8V R_L Open		—	19	24	mA	
	Over Voltage Shutdown	V_{sd}	Shutdown Voltage		15	16	17	V	
		V_{hys}	Hysteresis		0.5	0.8	1.2	V	
	Over Temperature Protection	T_{sd}	Shutdown		—	150	—	℃	
		T_{hys}	Hysteresis		—	25	—	℃	
Hall Amp	Input Bias Current	I_{HB}	V_H=6.0V		—	1.0	5	μA	
	Input Common Mode Voltage Range	V_H			1.5	—	10.5	V	
	Voltage Gain	G_{VH}			—	10	—	dB	
Output Stage	Quiescent Output Voltage	V_Q			5.1	5.7	6.3	V	
	Difference of Quiescent Voltage	$\triangle V_Q$			—	—	±0.3	V	
	Saturation Voltage	$V_{CE(sat)}$	I_O=0.35A		—	2.0	2.8	V	*
	Output Impedance	R_O	I_O=0.1A		—	0.45	—	Ω	
Control Amp	Internal Ref. Voltage	V_{REF1}			—	3.15	—	V	
	Voltage Gain (CTL Amp to Output)	G_V			15	18	21	dB	
	Difference of Gain	$\triangle G_V$			—	—	±2	dB	
Integrator	Internal Ref. Voltage	V_{REF2}			—	2.5	—	V	
	Input Bias Current	I_{BI}			—	—	±0.1	μA	
	Output Voltage Swing	A_+	I_O= +0.25mA		—	1.3	—	V	
		A_-	I_O= −0.25mA		—	−0.65	—		
	Unity Gain Band Width	BW	G_V=0dB		—	0.3	—	MHz	
Speed Discriminator	Injection Voltage	V_I	I_I=6mA		—	0.9	—	V	
	Output High Voltage	V_{OH}	I_O=0.25mA		4.4	4.7	—	V	
	Output Low Voltage	V_{OL}	I_O=−0.25mA		—	0.1	0.2	V	
	Cutoff Current	I_{off}	Charge Pump Off State		—	—	±0.1	μA	
	Count Number				—	1024	—		
Enable	Input High Voltage	V_{IH}			2.0	—	—	V	
	Input Low Voltage	V_{IL}			—	—	0.8	V	
	Input High Current	I_{IH}	V_H=2.0V	Enable 1	—	—	±10	μA	
				Enable 2	—	50	120	μA	
	Input Low Current	I_{IL}	V_L=0.8V	Enable 1	—	—	±10	μA	
				Enable 2	—	—	±40	μA	
Current Limiter	Reference Voltage	V_{REF3}			0.36	0.4	0.44	V	
FG Amp	Input Voltage	$V_{in(FG)}$	f=200Hz		2.0	—	20	mVpp	
OSC	Oscillation Frequency	f_{osc}			0.1	—	1.0	MHz	
Mode Select	No Division Input Voltage	V_{I1}			—	—	0.8	V	
	1/2 Division Input Voltage	V_{I2}	Open		—	6.3	—	V	
	1/4 Division Input Voltage	V_{I4}			10	—	—	V	
	No Division Input Current	I_{I1}	V_{IN}=0V		—	—	−1.0	mA	
	1/4 Division Input Current	I_{I4}	V_{IN}=12V		—	—	1.0	mA	

Note * : Sum of upper and lower TRS saturation voltages

■EXTERNAL COMPONENTS

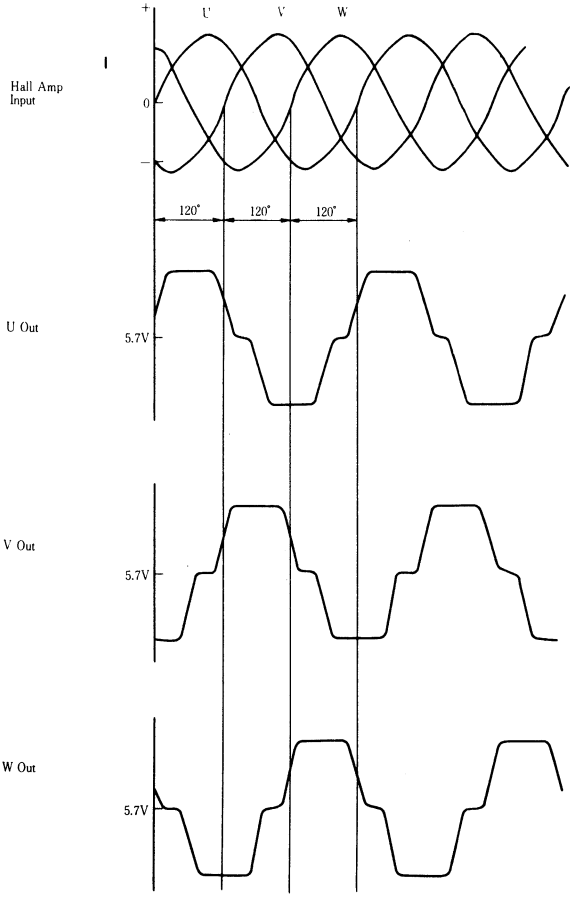
Parts No.	Recommended Value	Function	Note
R_{101}, R_{102}	—	Hall Elements Bias	1
R_{103}, R_{104}, R_{105}	2.2Ω	Stability	
Rs	—	Current Sense	3
R_1, R_2	See Application	Integral Constant	4
C_{101}, C_{102}, C_{103}	0.1μF	Stability	2
C_{104}	≧0,1μF	Vcc By-passing	
C_{105}	10μF	AC Coupling FG	
C_{106}	47pF	AC Coupling OSC	
C_{107}	56pF	Stability	
C_{108}, C_{109}, C_{110}	≧0.01μF	Stability	
C_{111}	10μF	Stability	
C_1, C_2	See Application	Integral Constant	4
C_3	See Application	Filter Constant	4
X' tal	See Application	Resonator	4

Note 1. Set R_{101} and R_{102} at which output voltage of 30 to 100 mVpp
Note 2. Use C_{101} to C_{103} which cause no 2nd resonance.
Note 3. Output current is limited as shown below by Rs value.

$$I\ limit = \frac{V_{REF3}}{Rs}$$

Note 4 See HA13426.

■TIMING CHART



HA13439MP ●2-phase Brushless DC Fan Motor Drive IC

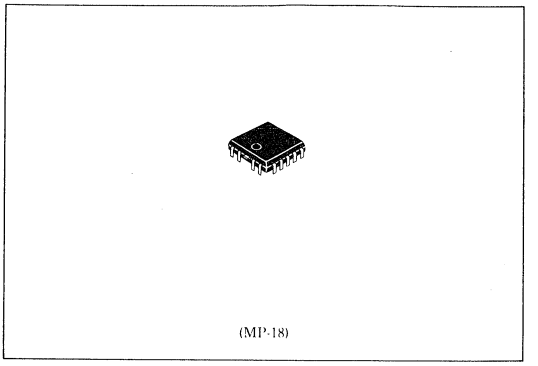
The HA13439MP is a monolithic IC designed to provide 2-phase brushless DC fan motor drive. It has the following functions.

■ FUNCTIONS

- 1.5A/80V output transistor.
- Hall Amp.
- Stuck rotar protection circuit (Auto Restart)
- Over temperature protection circuit OTSD.

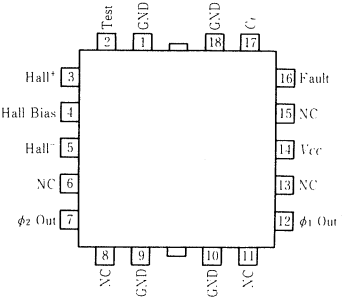
■ FEATURES

- High Current Capability, High Breakdown Voltage.
- Wide Supply Voltage Range (7.5 to 28V).
- Motor Coil Burning out Protection in the case of Rotar Stuck.
- Small, Surface-mount Technology Package.
- Stands Reverse Power Supply.



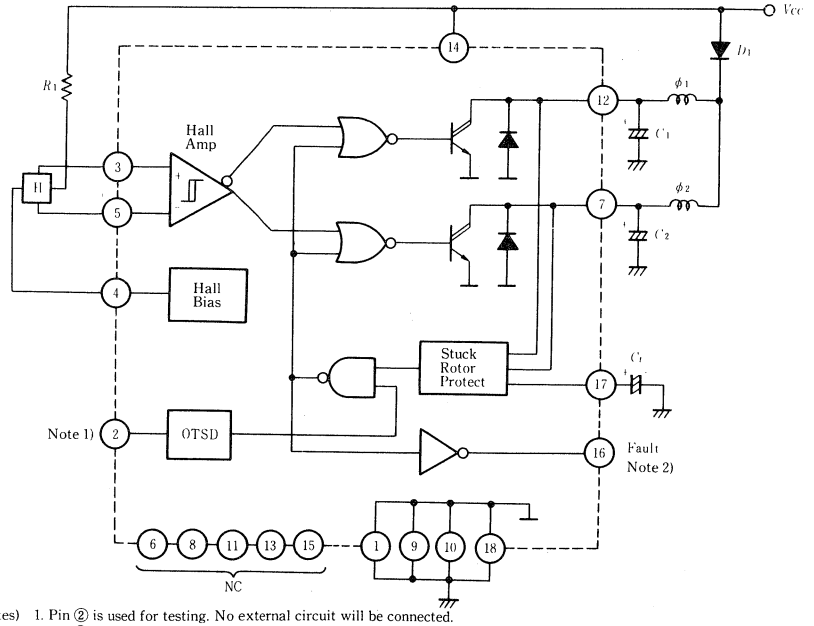
(MP-18)

■PIN ARRANGEMENT



(Top View)

■BLOCK DIAGRAM



Notes) 1. Pin ② is used for testing. No external circuit will be connected.
2. Pin ⑯ is open collector output. Internal transistor is "OFF" when the rotar is running.

HITACHI

■ABSOLUTE MAXIMUM RATINGS (T_a=25°C)

Item	Symbol	Ratings	Unit	Note
Supply Voltage	V_{CC}	−28 to +35	V	1
Output Voltage	BV_{CEX}	80	V	
Output Current (Peak)	I_{opeak}	1.5	A	2
Output Current (DC)	I_{odc}	1.0	A	
Input Voltage	V_{in}	0 to V_{CC}	V	3
Power Dissipation	P_T	1.25	W	4
Junction Temperature	T_j	150	°C	5
Storage Temperature Range	T_{stg}	−55 to +125	°C	

Notes) 1. Operating voltage range is shown below.
V_{CC}=7.5 to 28V
2. $t \leqq 1$ sec.
3. Apply to Hall Amp. input.
4. Value under $T_{a(u)}$=80°C. Thermal resistance of package is show below.
$\theta_{j\text{-}pin} \leqq 56$°C/W
$\theta_{j\text{-}a} \leqq 80$°C/W
(Heat sink with 1000mm^2 are adhered to IC surface by epoxy resin.)
5. Operating junction temperature range is shown below.
$T_{j(op)}$ −10 to +125°C

■ELECTRICAL CHARACTERISTICS (T_a=25°C, V_{CC}=7.5V to 28V)

	Item	Symbol	Test Condition	min	typ	max	Unit	Applicable Pin	Note
Quiescent Current		I_Q	R_F=OPEN, Pin 17=GND	−	6	12	mA	14	
Hall Amp	Common Mode Input Voltage Range	V_H		1.2	−	V_{CC} −4	V	3, 5	
	Input Current	I_{HI}	V_H=2V	−	−	±50	μA	3, 5	
	Hysteresis	ΔV_H	R_H=400Ω	7	12	20	mV	3, 5	1
	Bias Output Voltage	V_{HB}	I_H=5mA	1.2	1.4	1.6	V	4	
Output Transistor	Cut off Current	I_{CEX}	V_{CE}=28V, V_{CC}=28V	−	−	100	μA	7, 12	
			V_{CE}=80V, V_{CC}=28V	−	2.6	4	mA	7, 12	
	Saturation Voltage	V_{CE} (sat)	I_C=0.2A	−	0.80	1.1	V	7, 12	
			I_C=0.5A	−	0,95	1.4	V	7, 12	
			I_C=1.0A	−	1.25	2.0	V	7,12	
	Parasitic Diode Forward Voltage	V_{SD}	I_C=−1.0A	−	−1.7	−2.0	V	7, 12	2
Stuck Rotor Protection	Ct Chorge Current	I_{tf}	V_{pin17}=2.4V	40	65	100	μA	17	1
	Ct Discharge Current	I_{ts}	V_{pin17}=2.4V	1	3	5	μA	17	1
	Threshold Voltage	V_{TH1}	Cut-OFF	2.4	—	3.1	V	17	1
		V_{TH2}	Recovery	1.4	—	2.2	V	17	1
Fault	Low Level Voltage	V_{OL}	I_C=1mA	−	0.2	0.4	V	16	
	Cut Off Current	I_{CEX2}	V_{CE}=28V	−	−	±50	μA	16	
OSTD	Operating Temperature	T_{SD}		150	−	−	°C	7, 12	
	Hystesesis	T_{HYS}		−	25	−	°C	7, 12	

Notes) 1. See the Timing Chart.
2. See the Fig. 1

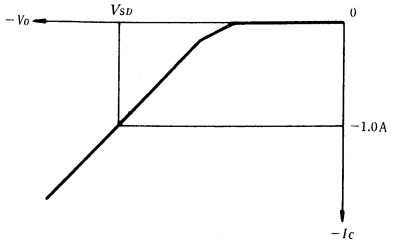


Fig. 1 Parasitic Diode Foward Voltage Characteristics

■EXTERNAL COMPONENTS

External Components No.	Reference Value	Purpose	Note
R_1	–	Hall Element Bias	
C_1, C_2	2.2μF		1
C_t	4.7μF	Time constant in protection circuit	2
D_1	–	Countermeasure for power supply reverse connection	3

Notes) 1. Use a high ripple type.
2. t_1 and t_2 is determined by the following equation in timing chart.

$$t_1 = \frac{C_t \cdot V_{TH1}}{I_{ct}}$$

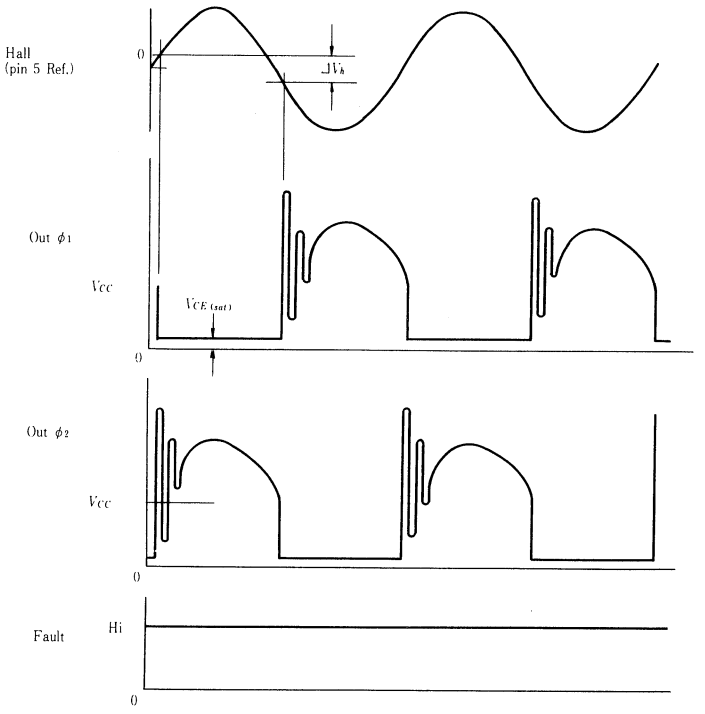
$$t_2 = \frac{C_t(V_{TH1} - V_{TH2})}{R_m}$$

3. Set t_1 for 1/5 to 1/1 of starting time.
3. In the case of no D_1, Current flowing to motor coil is determined when power supply reverse connection, where R_m (Ω) is coil resistance.

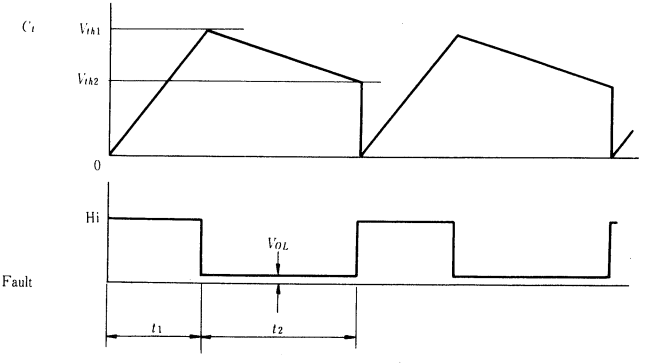
$$I_m = \frac{V_{CC} + V_{SD}}{R_m} \text{ (A Phase)}$$

■TIMING CHART

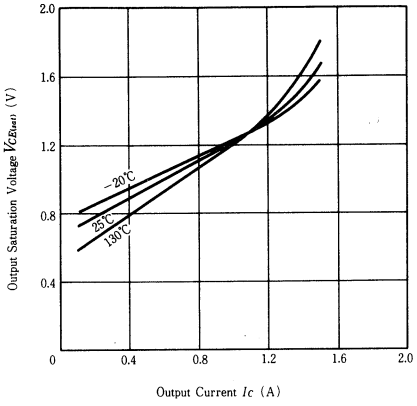
●Normal Operation



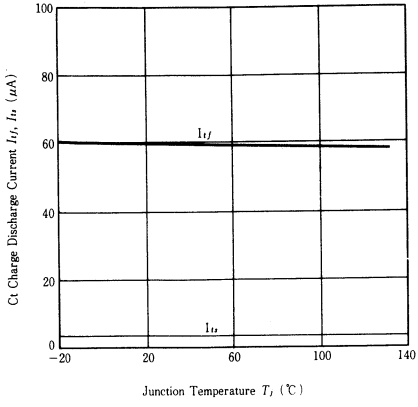
●In Rotor Stuck



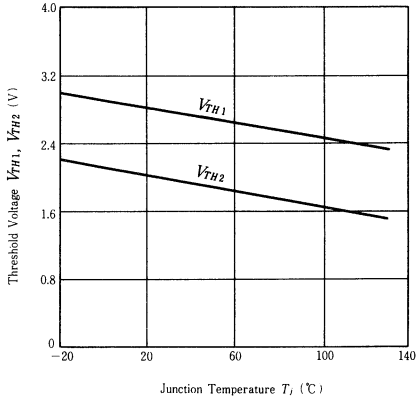
OUTPUT SATURATION VOLTAGE VS OUTPUT CURRENT



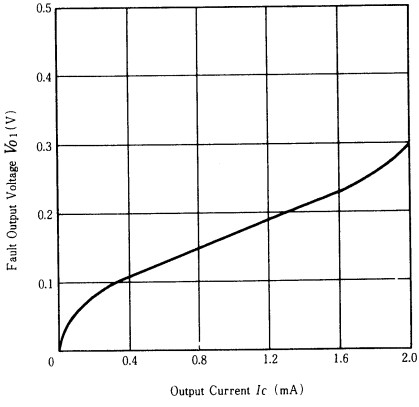
C_T CHARGE, DISCHARGE CURRENT VS TEMPERATURE



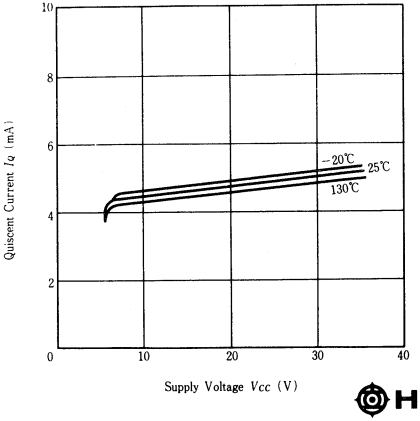
PROTECTION CIRCUIT THRESHOLD VOLTAGE VS TEMPERATURE



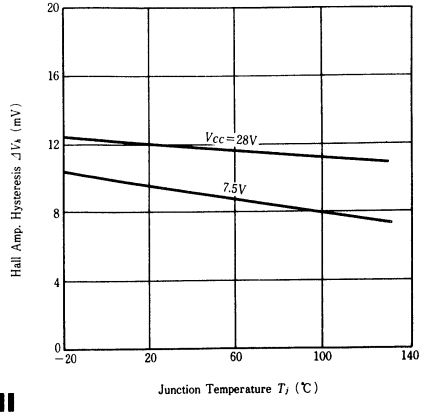
FAULT OUTPUT VOLTAGE VS OUTPUT CURRENT



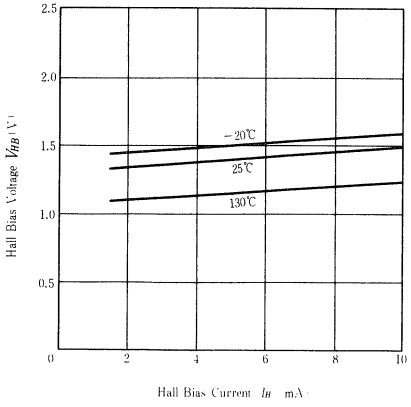
QUIESCENT CURRENT VS SUPPLY VOLTAGE



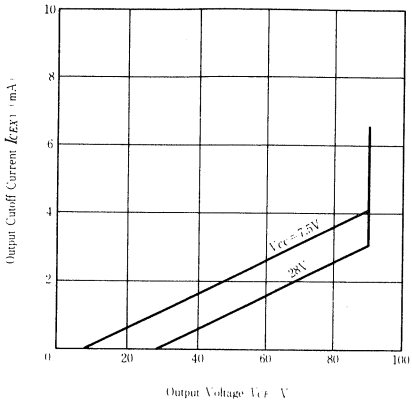
HALL AMP. HYSTERESIS VS TEMPERATURE



HALL BIAS VOLTAGE VS BIAS CURRENT

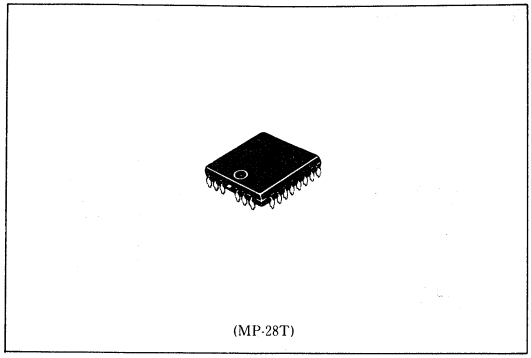


OUTPUT CUTOFF CURRENT VS OUTPUT VOLTAGE



HA13440MP ●3-phase Brushless DC Motor Drive IC —Preliminary—

The HA13440MP is a 3-phase brushless DC motor drive (output current; 1.0A/phase) designed for FDD spindle motor drive. Functions and features are shown as follows.



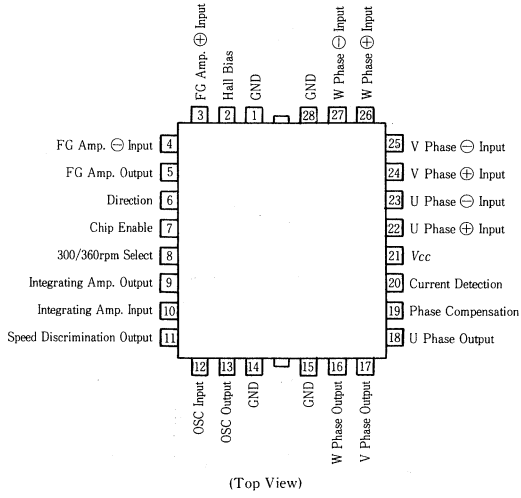
■FUNCTIONS

- 1.0A 3-phase Output Circuit.
- Hall Amp, Matrix.
- Control Amp. (Current Control).
- Direction.
- FG Amp, Zero Cross Detector.
- Oscillation Circuit.
- Speed Discriminator.
- 300/360 rpm Select.
- Integrating Amp.
- Current Limitter.
- Over Temperature Shut Down (OTSD).
- Chip Enable.

■FEATURES

- Possible to construct a servo system on a single chip.
- Require no adjustment because of digital control.
- Possible to use 5V (Operating Voltage Range: 4.25 to 13.8V).
- Low Power Dissipation.
- Small low thermal resistance surface-mount package.

■PIN ARRANGEMENT

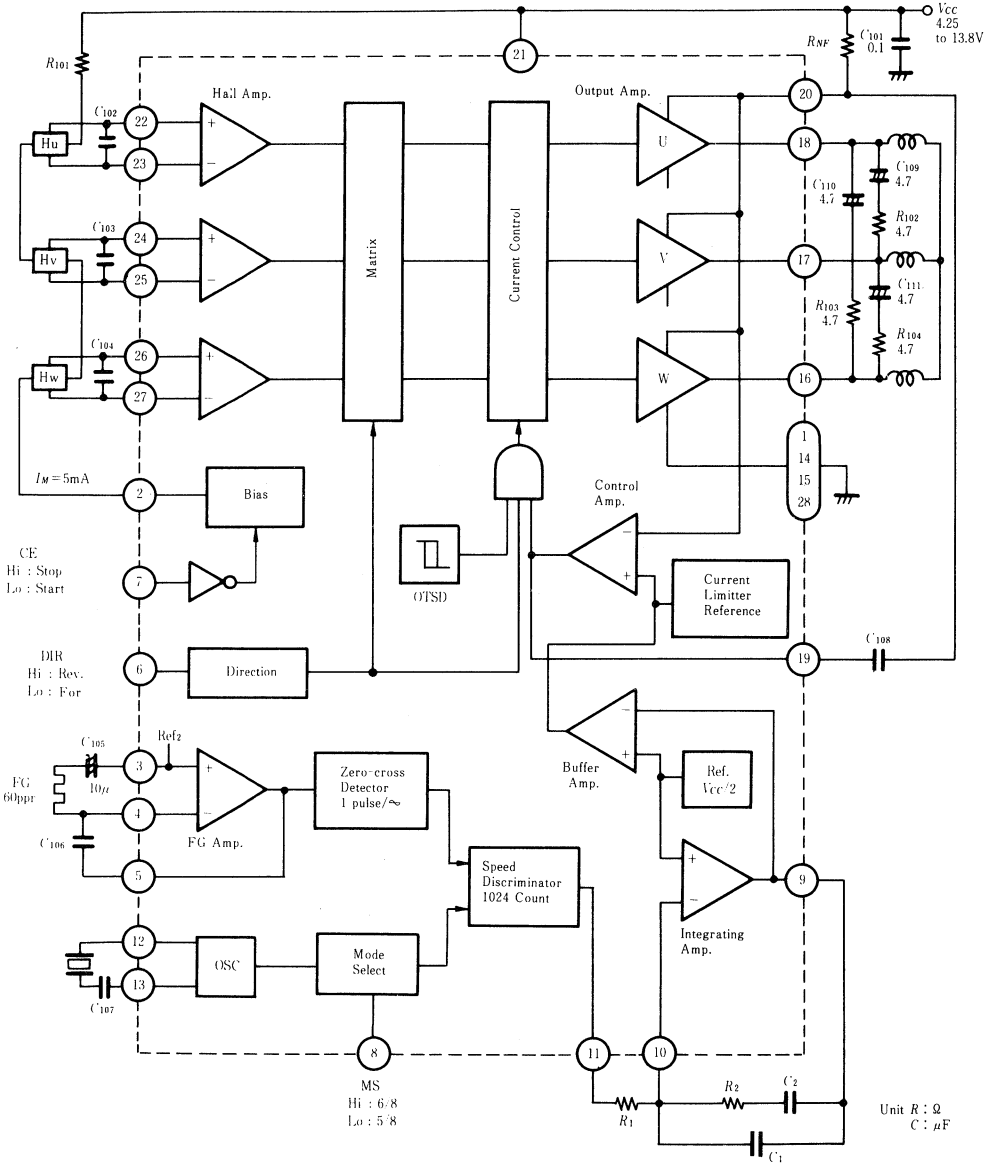


(Top View)

■TRUTH TABLE

Chip Enable CE	Direction DIR	Hall Amp. Input						Output		
		U+	U−	V+	V−	W+	W−	U	V	W
L	L	H	L	L	H	H	L	H	L	Open
		H	L	L	H	L	H	H	Open	L
		H	L	H	L	L	H	Open	H	L
		L	H	H	L	L	H	L	H	Open
		L	H	H	L	H	L	L	Open	H
		L	H	L	H	H	L	Open	L	H
	H	H	L	L	H	H	L	L	H	Open
		H	L	L	H	L	H	L	Open	H
		H	L	H	L	L	H	Open	L	H
		L	H	H	L	L	H	H	L	Open
		L	H	H	L	H	L	H	Open	L
		L	H	L	H	H	L	Open	H	L
H	×	×	×	×	×	×	×	Open	Open	Open

■BLOCK DIAGRAM



■ABSOLUTE MAXIMUM RATINGS (T_a=25°C)

Item	Symbol	Rating	Unit	Note
Supply Voltage	V_{CC}	+15	V	1
Instantaneous Output Current	I_{op}	1.0	A	2
Continuos Output Current	I_O	0.7	A	
Input Voltage	V_{in}	+7	V	3
Power Dissipation	P_T	2	W	4
Junction Temperature	T_j	150	°C	5
Storage Temperature Range	T_{stg}	−55 to +125	°C	

Notes) 1. Operating Voltage Range is shown below.
V_{CC}=4.25 to 13.8V
2. $t \leqq 0.5$sec.
3. Applicable to chip enable CE, direction DIR and mode select MS terminals
4. Value under Tpin1, 14, 15 & 28=100°C. Thermal resistance is shown below..
$\theta_{j\text{-}pin} \leqq 25$°C/W
$\theta_{j\text{-}a} \leqq 55$°C/W (In the case of metal base substrate)
$\theta_{j\text{-}a} \leqq 80$°C/W (In the case of glass-epoxy board)
5. Operating Junction Temperature is shown below.
T_{jopr}=0 to +125°C.

■ELECTRICAL CHARACTERISTICS (T_a=25°C, V_{CC}=4.25 to 13.8V)

Item		Symbol	Test Condition	min	typ	max	Unit	Applicable Terminal	Note
Quiscent Current		I_{Q1}	CE=2V	−	0.15	0.5	mA	20, 21	1
		I_{Q2}	CE=0.8V, R_L=OPEN	−	15	23	mA		1
Input Low Voltage		V_{IL}		−	−	0.8	V	6, 7, 8	
Input High Voltage		V_{IH}		2.0	−	V_{CC}	V		
Input Low Current		I_{IL}	V_{IL}=0V	−	−	±10	μA		
Input High Current		I_{IH}	V_{IH}=2V	−	−	±10	μA		
Hall Amp	Input Current	I_{HB}	V_H=2V	−	−	±10	μA	22 to 27	
	Common Mode Input Voltage	V_H		1.5	−	V_{CC}−1.0	V		
	Differential Input Voltage Range	U_H		70	−	200	mVpp		
Hall Bias	Output Voltage	V_{HB}	CE=0.8V, I_j=5mA	1.2	1.6	2.0	V	2	
	Leak Current	$I_{H\,off}$	CE=2V, V_{CE}=15V	−	−	±10	μA		
Output Amp	Leak Current	I_{CER}	CE=2V, V_{CE}=15V	−	−	100	μA	16, 17, 18	
	Saturation Voltage	V_{sat}	I_O=0.7A	−	1.3	1.8	V		2
			I_O=0.35A	−	1.0	1.2	V		2
Current Limitter Reference Voltage		V_{ref1}		0.225	0.25	0.275	V	20	3
Control Amp	Reference Voltage	V_{ref2}		0.9V_{CC}/2	V_{CC}/2	1.1V_{CC}/2	V	10	4
	Voltage Gain	G_{CTL}		−12	−10	−8	dB	16, 17, 18	
	Voltage Gain Difference	ΔG_{CTL}		−	−	±1.0	dB		
Integral Amp	Input Current	I_{B1}		−	−	±50	nA	10	
	Output Voltage Amplitude	$A+$	I⑨=0.5mA	0.62	0.72	0.82	V	9	5
		$A-$	I⑨=−0.5mA	−1.64	−1.44	−1.22	V		5
	Gain Band Width	BW_D	G_V=0dB	100	300	1000	kHz		
Speed Discrim-inator	Output High Voltage	V_{DOH}	I_O=0.5mA	V_{CC}−0.3	−	−	V	11	
	Output Low Voltage	V_{DOL}	I_O=−0.5mA	−	−	0.3	V		
	Cut-off Current	$I_{D\,off}$	V=2.5V	−	−	±50	nA		
	Operating Frequency	f_D		−	−	1000	kHz		
	Count Number	N_D		−	1024	−			
OSC	Oscillation Frequency Range	f_{OSC}		−	−	1000	kHz	13	
	Ocsillation Frequency Error	Δf_{OSC}	492kHz Ceramic Oscillation	−	−	±0.2	%		
FG Amp	Voltage Gain	G_{FG}	f=300Hz	39	41	43	dB	5	
	Gain Band Width	BW_2	C_{108}=0, G_{FG}=−3dB	5	10	20	kHz		
	Input Resistance	R_i		120	180	240	Ω	3	
	Distortionless Output Voltage	V_O	f=300Hz	1.0	−	−	V_{rms}	5	

(to be continued)

Item		Symbol	Test Condition	min	typ	max	Unit	Applicable Terminal	Note
Zerocross Detection	Hysteresis	V_{hys}		35	50	65	mV	5	
	Offset Voltage	V_{os}		–	–	±10	mV		
OTSD	Operating Temperature	T_{sd}		125	–	–	°C		
	Hysteresis	T_{hys}		–	25	–	°C		

Notes) 1. Sum of ⑳, ㉑ in current.
2. Sum of upper and lower transistor saturation voltage.
3. Measure from V_{CC} pin.
4. In the case of $V_{CC}>11.2V$, the value keeps 5.6V ± 10%.
5. Measure from V_{ref2}.

■EXTERNAL COMPONENT

Part No.	Recommended Value		Purpose	Note
	5V/3.5" FDD	12V/5.25" FDD		
R_{101}, R_{102}, R_{103}	4.7Ω	4.7Ω	For stability	
R_{104}	330	1.8k	Hall Element Bias	
R_1	56k	56k	Integral Constant	
R_2	150k	56k	Integral Constant	
R_{NF}	0.62	0.39	Current Detection	1
C_{101}, C_{102}, C_{103}	4.7μF	4.7μF	For stability	2
C_{104}	0.1μ	0.1μ	Supply Bypass	3
C_{105}	10μ	10μ	FG Amp AC Coupling	
C_{106}	4700p	4700p	FG Amp Band Setting	
C_{107}	47p	47p	Oscillation AC Coupling	
C_{108}	0.1μ	0.1μ	Control Amp Phase Compensation	
C_{109}, C_{110}, C_{111}	0.01μ	0.01μ	For stability	
C_1	0.022μ	0.047μ	Integral Constant	5
C_2	0.22μ	0.47μ	Integral Constant	5
X'tal	492kHz	492kHz		4

Notes) 1. Current limitter operates by the following equation.

$$I_{omax} = \frac{V_{ref1}}{R_{NF}}$$

2. Need to use non-polar type.
3. Put them as near the IC as possible.
4. Oscillation frequency ($fosc$) is determined by the following equation.
(1) When 300/360 selection is "H" level,

$$f_{OSC} = \frac{8192}{6} f_{FG} \quad \text{(Hz)}$$

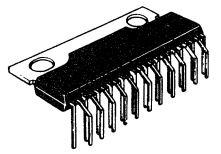
(2) When 300/360 selection is "L" level,

$$f_{OSC} = \frac{8192}{5} f_{FG} \quad \text{(Hz)}$$

5. Need to use small leak current

HA13441, HA13442 ●3-phase Brushless DC Motor Drive IC for HDD —Preliminary

HA13441 and HA13442 are three-phase brushless DC motor drive IC of 2A/phase, 4A/phase and have following functions and features.



(SP-23TA)

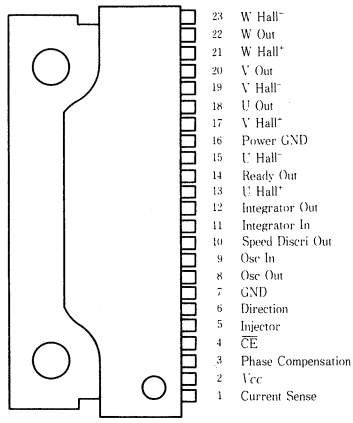
■ FUNCTIONS

- 2A/phase (4A/phase) three phase output circuit.
- Hall Amp., Matrix.
- Chip Enable.
- Buffer Amp.
- Control Amp.
- Speed Discriminator.
- Oscillation Circuit.
- Zero Cross Detector.
- Integrator.
- Current Limitter.
- Ready Circuit.
- Low Supply Voltage Inhibit.
- Over Temperature Shut Down

■ FEATURES

- Possible to construct a servo system on a single chip.
- Require no adjustment because of digital servo system.
- Large output current (2A/phase, 4A/phase).
- Output voltage noise is smaller.
- Speed error is small.
- Low Thermal Resistance package.

■ PIN ARRANGEMENT



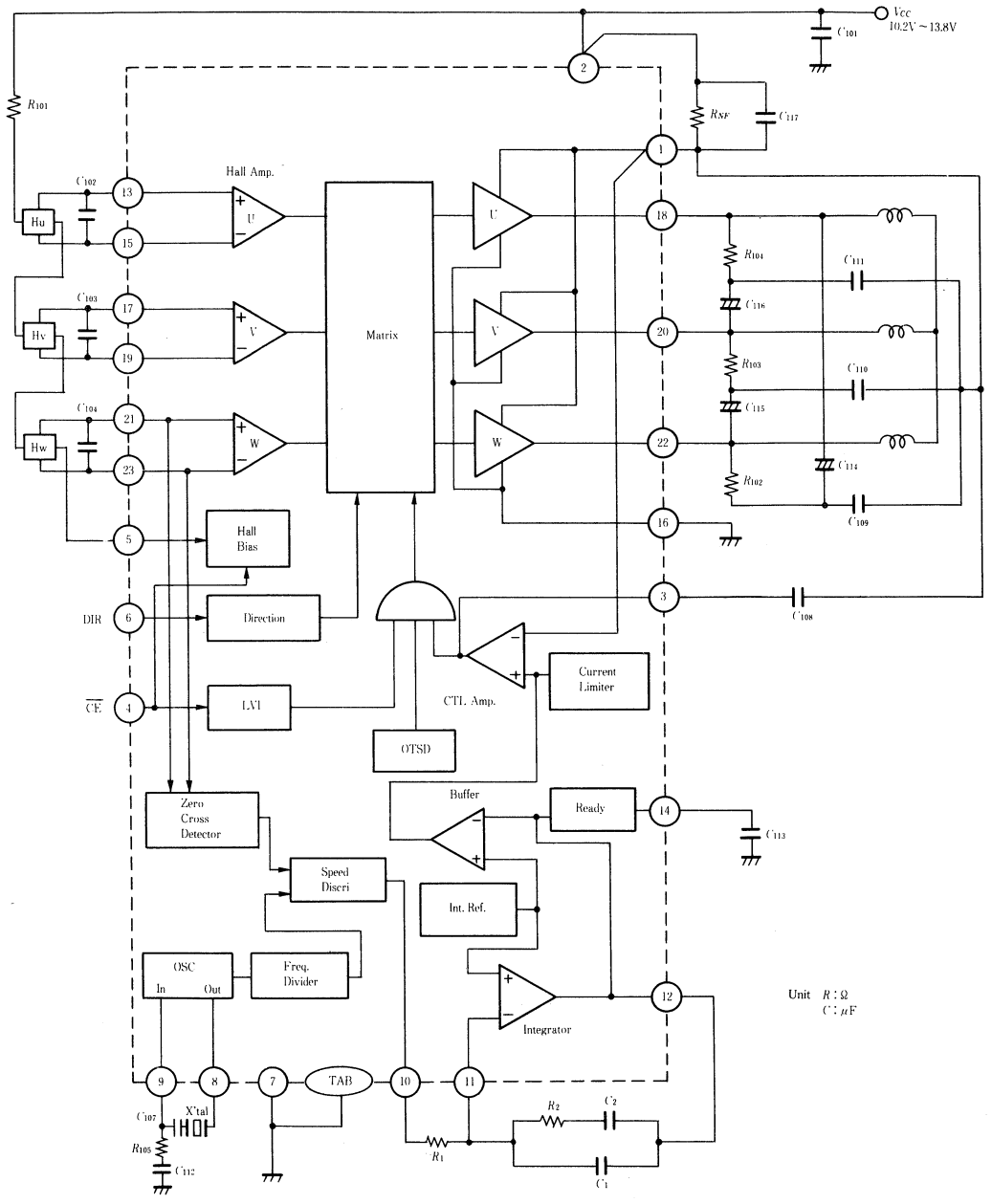
(Top View)

■ TRUTH TABLE

Chip Enbale CE	Hall Amp. Input			Output		
	U	V	W	U	V	W
L	H	L	H	H (L)	L (H)	OPEN (OPEN)
	H	L	L	H (L)	OPEN (OPEN)	L (H)
	H	H	L	OPEN (OPEN)	H (L)	L (H)
	L	H	L	L (H)	H (L)	OPEN (OPEN)
	L	H	H	L (H)	OPEN (OPEN)	H (L)
	L	L	H	OPEN (OPEN)	L (H)	H (L)
H	×	×	×	OPEN		

OPEN: High Impedance
× : Don't care

■BLOCK DIAGRAM



■ABSOLUTE MAXIMUM RATINGS (T_a=25°C)

Item	Symbol	Rating		Unit	Note
		HA13441	HA13442		
Supply Voltage	V_{CC}	+15	+15	V	1
Input Voltage	V_{in}	V_{CC}	V_{CC}	V	2
Output Current	I_O	2	4	A	
Power Dissipation	P_T	25	25	W	3
Junction Temperature	T_j	150	150	°C	4
Storage Temperature Range	T_{stg}	−55 to +125	−55 to +125	°C	

Notes) 1. The operating supply voltage range is 12V ± 15% (10.2V to 13.8V).
2. Applicable for Hall Amp. input, Direction input, Chip Enbale input.
3. The value is at T_C = 75°C. Thermal resistance shows as follows.
$\theta_{j-c} \leqq 3$°C
$\theta_{j-a} \leqq 40$°C
4. The operating junction temperature range is T_{opr} = 0°C to +125°C.

■ELECTRICAL CHARACTERISTICS (T_a=25°C, V_{CC}=12V)

Item		Symbol	Test Condition	min	typ	max	Unit	Applcable Terminal	Note
Quiescent Current		I_{CC1}	CE=2V	−	1.0	2	mA	1, 2	1
		I_{CC2}	CE=0.8V	−	24.0	36.0	mA		1
Hall Amp. to Bias	Input Current	I_{HB}	V_H=6.0V	−	2	10	μA		
	Input Common Mode Voltage Range	V_H		1.3	−	9.5	V		
	Bias Voltage	V_{HB}	I_H=5mA	1.3	−	1.8	V	5	
Output Amp.	Leak Current	I_{CER}	V_{CE}=15V	−	−	2	mA	18, 20,22	
	Saturation Voltage	V_{sat1}	I_O=3.0A (1.5A)	−	2.8	3.2	V		2
		V_{sat2}	I_O=0.6A (0.3A)	−	1.8	2.4	V		2
Reference Voltage Internal Current Limitter		V_{ref1}		0.48	0.56	0.63	V	1	3
Buffer Amp.	Internal Reference Voltage	V_{ref2}		2.95	3.15	3.35	V	11	
	Voltage Gain	G_V		8 (5)	6 (3)	4 (1)	dB	1	4
	Difference of Gain	ΔG_V		−	−	±1.0	dB		
Integrator	Input Current	I_B (ER)		−	−	±60	nA	11	
	Output Voltage Swing	$A+$	I_O=0.5mA	1.10	1.40	1.60	V	12	
		$A-$	I_O=−0.5mA	−0.55	−0.7	−0.85	V		
	Gain Bandwidth	BW	G=0dB	100	−	−	kHz		
Speed Discriminator	Output High Voltage	V_{OH}	I_O=0.5mA	5.8	6.1	−	V	10	5
	Output Low Voltage	V_{OL}	I_O=−0.5mA	−	−	0.2	V		5
	Cut Off Current	I_{off}		−	−	±60	nA		
	Count Number			−	2048	−			
Chip Enable	Input High Voltage	V_{IH}		2.0	−	−	V	4	
	Input Low Voltage	V_{IL}		−	−	0.8	V		
	Input High Current	I_{IH}	V_{IH}=5.5V	−	−	±10	μA		
	Input Low Current	I_{IL}	V_{IL}=0V	−	−	±10	μA		
OSC	Frequency Error	f_{osc}		−	−	0.1	%	8	
	Operating Frequency	f_{osc}		−	−	8	MHz		
Zero Cross Detection Sensitivity		V_Z		−	−	30	mVpp	21, 23	6
Ready Circuit	Output High Voltage	V_{OH}	I_{source}=0.1mA	4.8	5.0	−	V	14	
	Output Low Voltage	V_{OL}	I_{sink}=0.1mA	−	0.2	0.3	V		
	Output Current	I_{sink}	V=2.5V	0.1	0.2	0.3	mA		
		I_{fo}	V=2.5V	0.1	0.2	0.3	mA		

(to be continued)

Item		Symbol	Test Condition	min	typ	max	Unit	Applicable Terminal	Note
LVI Operating Voltage				—	—	9.0	V		
OTSD Operating Temperature		T_{sd}		125	—	—	°C		
Direction	Input High Voltage	V_{IH}		4.0	—	—	V	6	
	Input Low Voltage	V_{IL}		—	—	0.8	V		
	Input High Current	I_{IH}	V_{IH}=5.5V	—	—	±10	μA		
	Input Low Current	I_{IL}	V_{IL}=0V	—	—	±10	μA		

Notes) 1. Sum of ①, ② in pin.
2. Sum of upper and lower transistor saturation voltage. ( ) shows HA13441.
3. ( ) shows HA13441.
4. Measure from V_{CC} pin
5. Measure from V_{ref2}
6. Minimum input voltage necessary for producing trigger pulse.

■EXTERNAL COMPONENTS

Parts No.	Reference Value		Purpose	Note
	HA13441 3.5"×2disk HDD	HA13442 5.25"×6disk HDD		
R_{101}	1kΩ	1kΩ	Hall Element Bias	
R_{102}	470	470	For Oscillation Stability	1
R_{103}	330	330	For Stability	2
R_{104}, R_{105}, R_{106}	2.2	2.2	For Stability	2
R_1	22k	22k	Integral Constant	3
R_2	330k	330k	Integral Constant	3
R_{NF}	0.47	0.22	Current Sence	4
C_{101}	0.1μF	0.1μF	Power Supply By-pass	2
C_{102}	10p	10p	AC Coupling OSC	
C_{103}	0.047μ	0.047μ	For Oscillation Stability	1
C_{104}	0.1μ	0.1μ	For Ready Output Fillter	
C_{105}, C_{106}, C_{107}	3300p	3300p	For Stability	2
C_{108}	0.068μ	0.068μ	Control Amp. Phase Compensation	2
C_{109}, C_{110}, C_{111}	0.1μ	0.1μ	For Stability	2, 5
C_{112}, C_{113}, C_{114}	2.2μ to 10μ	2.2μ to 10μ	EMI Reduction	6
C_{115}	0.1μ	0.1μ	For Stability	5
C_1	0.022μ	0.1μ	Integral Constant	3
C_2	0.47μ	1.0μ	Integral Constant	3
X'_{tal}	3.932MHz	3.932MHz	Resonator	7

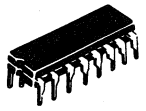
Notes) 1. Unnecessary in some output frequencies. Contact with the resonator maker please.
2. Put them as near the IC as possible. When attached at a distance, these parts lose the effect.
3. The optimum value depends on the motor specification (Inertia moment including load, torque constant, standard rotation number)
4. Output Current is limited as shown below. Use non-inductive type of R_{NF}.

$$I_{omax} = \frac{V_{ref1}}{R_{NF}}$$

5. Use these capacitors which have good frequency characteristics and cause no 2nd resonance.
6. Need to use non-polar type.
7. Use crystal oscillator.

HA16628P ●5-bit D/A Converter and Position Amplifier

The HA16628P is a monolithic integrated circuit designed for use with the HA16629P to DC motor positioning system for applications such as carriage/daisy-wheel position Control in Typewrites.



(DP-16)

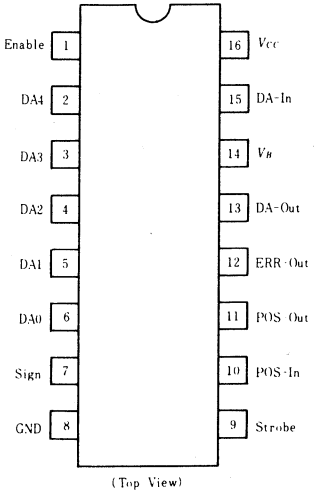
■FUNCTIONS

- 5 bit D/A Converter
- Error Amplifier
- Position Amplifier

■FEATURES

- Single Supply Voltage 10V DC to 20V DC
- Compatible with TTL, LSTTL & C-MOS
- Low Input Current (D/A Converter)

■PIN ARRANGEMENT



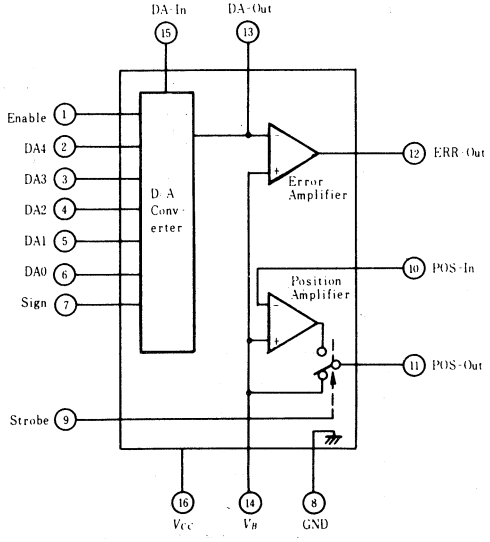
(Top View)

■ABSOLUTE MAXIMUM RATINGS (Ta=25°C)

Item	Symbol	Rating	Unit	Note
Supply Voltage	V_{CC}	20	V	
Common Voltage	V_B	0.55V_{CC}	V	
Power Dissipation	P_T	450	mW	
Input Voltage	V_I	6	V	1
Output Current	I_O	±5	mA	2
Operating Temperature Range	T_{opr}	0 to +70	°C	
Storage Temperature Range	T_{stg}	−50 to +125	°C	

Notes 1. Apply to DA_0~DA_4, Sign, ENABLE, STROBE
2. Apply to Pos-Out, ERR-Out

■BLOCK DIAGRAM



■ELECTRICAL CHARACTERISTICS (Ta=25℃, V_{CC}=12V, V_B=5V)

Item	Symbol	Test Conditions	min	typ	max	Unit
Supply Voltage	V_{CC}		10	—	20	V
Supply Current	I_{CC}	No Loads	—	—	10	mA
Supply Current of V_B (Pin 14)	I_B	No Loads	—	—	1	mA

●D/A Converter

Item	Symbol	Test Conditions	min	typ	max	Unit
Current Reference Input Range (Pin 15)	I_{DAIN}	all inputs "L"	0.3	—	1	mA
Current Reference Off-set Voltage (Pin 15 to 14)	V_{IO}	I_{DAIN}=0.3 to 0.7mA	−20	—	20	mV
Output Current	$I_{DAout(1)}$	I_{DAin}=0.516mA, Sign="H" Other input all"L"	0.96	0.98	1.00	mA
	$I_{DAout(2)}$	I_{DAin}=0.516mA, Sign="L" Other input all"L"	−1.00	−0.98	−0.96	mA
Output Current (Output Offset Current)	$I_{DAout(3)}$	Sign="L" Enable="L" Other input all"H"	−1	—	1	μA
	$I_{DAout(4)}$	Sign="H" Enable="L" Other input all"H"	−1	—	1	μA
Low Level Input Voltage (Digital Inputs)	V_{IL}		—	—	0.8	V
High Level Input Voltage (Digital Inputs)	V_{IH}		2.0	—	—	V
Low Level Input Current (Digital Inputs)	I_{IL}	V_{IL}=0V	−1	—	—	μA
High Level Input Current (Digital Inputs)	I_{IH}	V_{IH}=5V	—	—	20	μA

●Error Amplifier

Item	Symbol	Test Conditions	min	typ	max	Unit
Input Offset Voltage	V_{IO}	All inputs "H" DA-out to ERR-out	−5	—	5	mV
Output Voltage Swing	V_{out}	I_{ERRout}=1mA	V_B−3.3	—	V_B+3.3	V

●Position Amplifier

Item	Symbol	Test Conditions	min	typ	max	Unit
Low Level Input Voltage (Pin 9)	V_{IL}		—	—	0.8	V
High Level Input Voltage (Pin 9)	V_{IH}		2.0	—	—	V
Input Offset Voltage	$V_{IO(1)}$	Strobe="L" POS-IN to POS-out	−10	—	10	mV
	$V_{IO(2)}$	Strobe="H"	−10	—	10	mV
Input Bias Current (Pin 10)	I_{IB}	Strobe="L"	−1	—	—	μA
Output Voltage Swing	V_{out}	$I_{POS-out}$=1mA, Strobe="L"	V_B−3.3	—	V_B+3.3	V

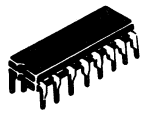
■D/A CONVERTER LOGIC FUNCTION

Digital word							Commands
Sign	DA4	DA3	DA2	DA1	DA0	ENABLE	
*	*	*	*	*	*	H	DAout=Zero
*	H	H	H	H	H	L	DAout=Zero
L	H	H	H	H	L	L	DAout=+min
L	L	L	L	L	L	L	DAout=+max
H	H	H	H	H	L	L	DAout=−min
H	L	L	L	L	L	L	DAout=−max

Notes: *=indifferent L=Low level H=High level
+min, +max=Source Current
−min, −max=Sink Current

HA16629P ● Tachometer Converter (F/V Converter)

The HA16629P is a monolithic integrated circuit designed for use with the HA16628P to DC motor positioning System for applications such as carriage/daisy-wheel position control in Typewrites.



(DP-16)

■ FUNCTIONS

- Tacho Voltage Generator (F/V converter)
- Reference Voltage Generator
- Position pulse Generator

■ FEATURES

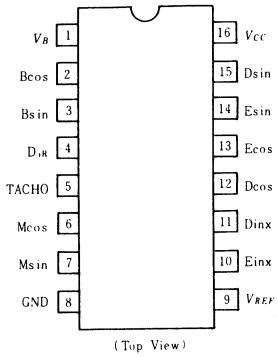
- Single Supply Voltage 10V DC to 20V DC
- Position pulse output is open collector

■ ABSOLUTE MAXIMUM RATINGS (Ta=25°C)

Item	Symbol	Rating	Note
Supply Voltage	V_{CC}	20	V
Common Voltage	V_B	0.55V_{CC}	V
Input Voltage (Pin 4, 10, 13, 14)	$V_{I(1)}$	V_{CC}	V
Input Voltage (Pin 6, 7)	$V_{I(2)}$	V_B±5*	V
Output Voltage (Pin 11, 12, 15)	V_{out}	20	V
Output Current (Pin 11, 12, 15)	$I_{out(1)}$	5	mA
Output Current (Pin 2, 3, 5)	$I_{out(2)}$	±1	mA
Output Current (Pin 9)	$I_{out(3)}$	−1.5	mA
Power Dissipation	P_T	450	mW
Operating Temperature Range	T_{opr}	0 to +70	°C
Storage Temperature Range	T_{stg}	−50 to +125	°C

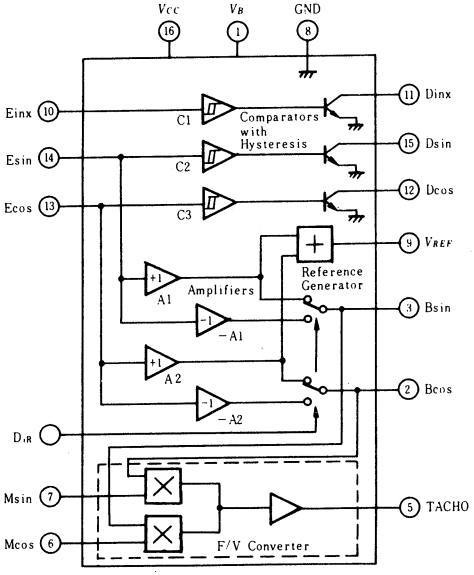
* $(V_B-5V)\geq 0V$, $(V_B+5V)\leq V_{CC}$

■ PIN ARRANGEMENT



(Top View)

■ BLOCK DIAGRAM



■ ELECTRICAL CHARACTERISTICS (Ta=25°C, V_{CC}=12V, V_B=5V)

Item	Symbol	Test Conditions	min	typ	min	Unit
Supply Voltage	V_{CC}		10	—	20	V
Supply Current	I_{CC}	no Loads	—	—	20	mA
Supply Current of V_B (Pin 1)	I_B	no Loads	−2	—	2	mA

●Comparators with Hysteresis (C_1, C_2 and C_3)

Item	Symbol	Test Conditions	min	typ	min	Unit
Input Bias Current	I_{IB}	$V_{E_{in}X}=V_{E_{sin}}=V_{ECOS}$=5V	−2	—	—	μA
Input "H" Level Threshold Voltage	V_{THH}	C_1 (Pin 10)	7.2	7.5	7.8	V
		C_2, C_3 (Pin 14, 13)	5.1	5.3	5.5	V
Input "L" Level Threshold Voltage	V_{THL}	C_1	5.7	6.0	6.3	V
		C_2, C_3	4.5	4.7	4.9	V
Output "L" Level Voltage	V_{OL}	I_{OL}=2.5mA	—	—	0.4	V
Output Leak Current	I_{OH}	V_{OH}=5V	—	—	2	μA

●Amplifiers (A_1, $-A_1$, A_2 and $-A_2$)

Item	Symbol	Test Conditions	min	typ	max	Unit
Input "L" Level Voltage (Pin 4)	V_{IL}		—	—	0.8	V
Input "H" Level Voltage (Pin 4)	V_{IH}		2.0	—	—	V
Common Mode Input Voltage Range	V_{CM}		V_B±2.5	—	V_B±3.5	V
Output Offset Voltage (A_1 and A_2)	$V_{OS(+)}$	$D_{in}R$=L	−30	—	30	mV
Output Offset Voltage ($-A_1$ and $-A_2$)	$V_{OS(-)}$	$D_{in}R$=H	−50	—	50	mV
Voltage gain (A_1 and A_2)	$A_{VD(+)}$	$D_{in}R$=L	—	1	—	V/V
Voltage gain ($-A_1$ and $-A_2$)	$A_{VD(-)}$	$D_{in}R$=H	—	−1	—	V/V
Output Voltage Swing	V_{out}		V_B−3.3	—	V_B+3.3	V

●Reference Generator

Item	Symbol	Test Conditions	min	typ	max	Unit
DC Reference Voltage (Pin 9)	V_{REF1}	I_{REF}=−0.5mA, Note (1)	7.5	8.0	8.5	V
	V_{REF2}	I_{REF}=−0.5mA Note (2)	6.7	7.5	8.3	V

Note (1)

No.	Test Conditions		Unit
	E sin	E cos	
1	$V_B+\frac{3}{\sqrt{2}}$	$V_B+\frac{3}{\sqrt{2}}$	V_{DC}
2	$V_B+\frac{3}{\sqrt{2}}$	$V_B-\frac{3}{\sqrt{2}}$	V_{DC}
3	$V_B-\frac{3}{\sqrt{2}}$	$V_B+\frac{3}{\sqrt{2}}$	V_{DC}
4	$V_B-\frac{3}{\sqrt{2}}$	$V_B-\frac{3}{\sqrt{2}}$	V_{DC}

V_B=5 V

Note (2)

No.	Test Conditions		Unit
	E sin	E cos	
1	V_B+3	V_B	V_{DC}
2	V_B	V_B+3	V_{DC}

V_B=5 V

●F/V Converter

Item	Symbol	Test Conditions	min	typ	max	Unit
Input Bias Current	I_{IB}	$V_{M\,sin}=V_{M\,cos}=5V$	—	5	15	μA
DC Output Voltage (Pin 5)	V_{TACHO1}	Note (1)	1.5	—	2.0	V_{DC}
	V_{TACHO2}	Note (2)	8.0	—	8.5	V_{DC}
Output Voltage Swing	V_{out}		$V_B-3.3$	—	$V_B+3.3$	V
Output Offset Voltage (Pin 5)	V_{IO}	$M_{sin}=M_{cos}=V_B$	−80	—	80	mV

	No. / Cond.	E sin	E cos	M sin	M cos
Note (1)	1	V_H	V_H	V_+	V_-
	2	V_H	V_L	V_-	V_-
	3	V_L	V_L	V_-	V_+
	4	V_L	V_H	V_+	V_+
Note (2)	5	V_H	V_H	V_-	V_+
	6	V_H	V_L	V_+	V_+
	7	V_L	V_L	V_+	V_-
	8	V_L	V_H	V_-	V_-

$V_H = V_B + 1$ (V)

$V_L = V_B - 1$ (V)

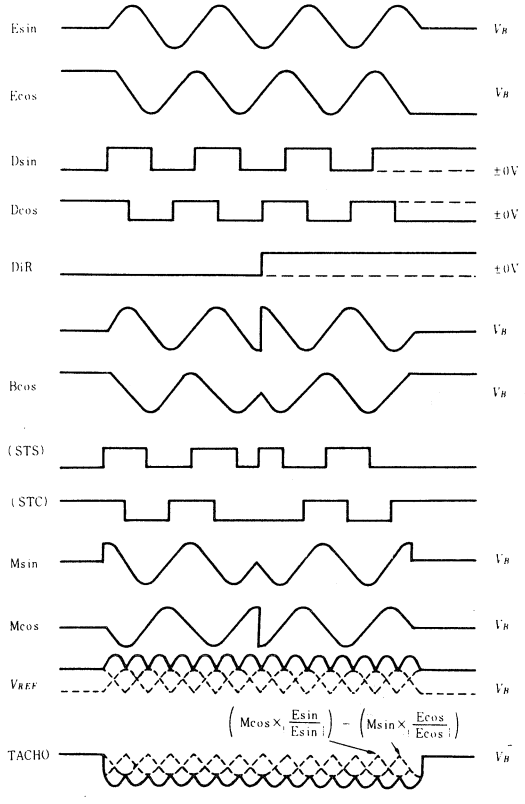
$V_+ = V_B + \frac{1.6}{\sqrt{2}}$ (V)

$V_- = V_B - \frac{1.6}{\sqrt{2}}$ (V)

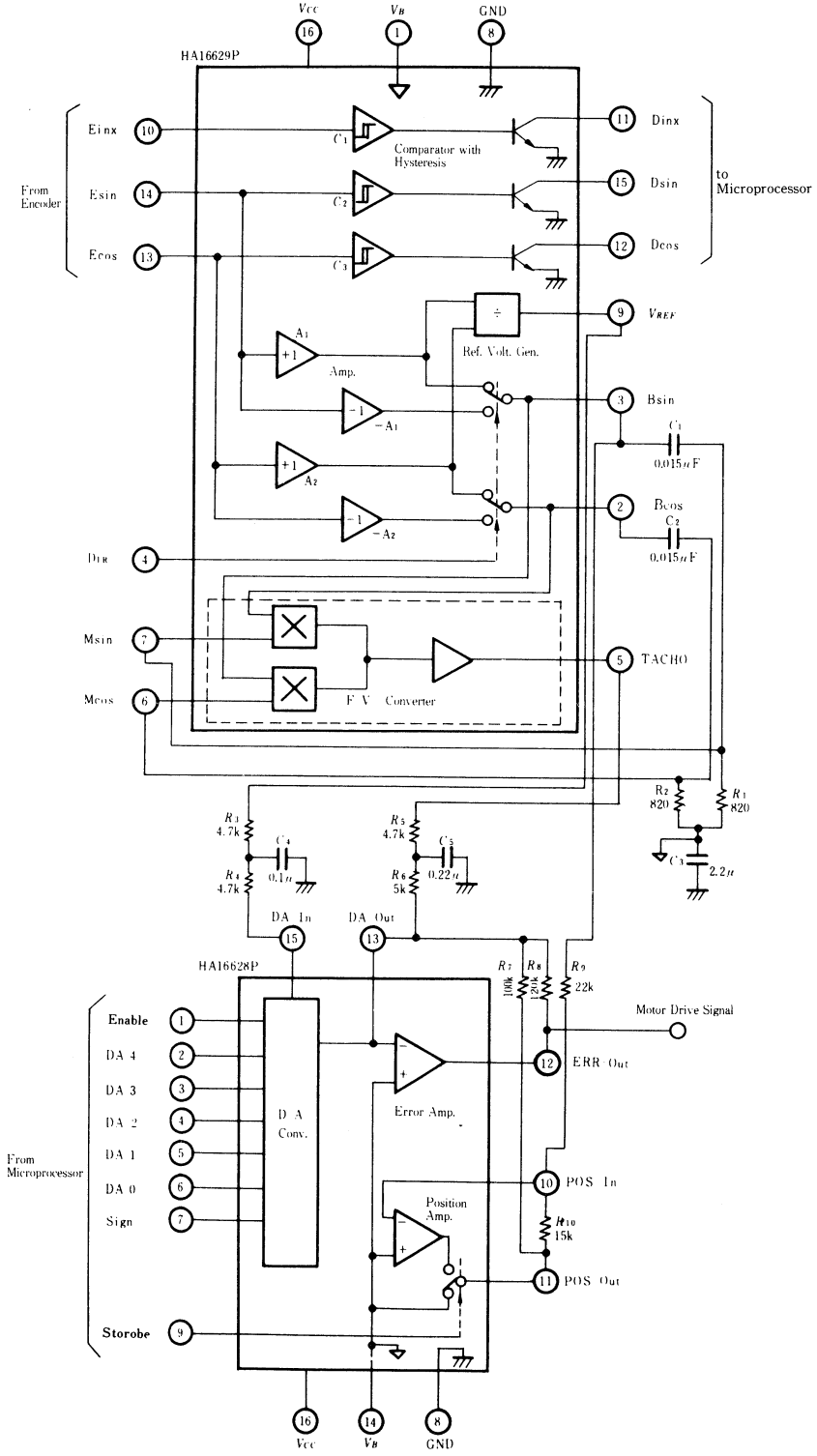
$V_B = 5$ (V)

■ WAVEFORMS

●Clock Wise Direction



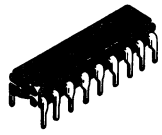
APPLICATION



HA16631P, HA16631MP ●Flexible Disk Read Amplifier

The HA16631P and the HA16631MP are monolithic read amplifiers for flexible disk drive, and provide wave-shaped output signals. The amplified signals from the magnetic head generate data pulses by differentiator, zero-volt comparator and waveform shaper section.

HA16631P



(DP-18)

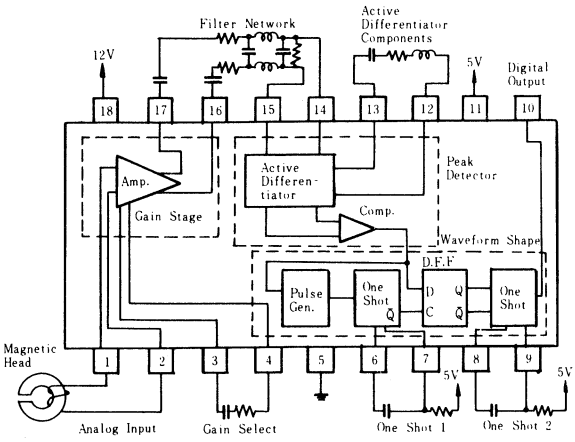
HA16631MP

(MP-18)

■FEATURES

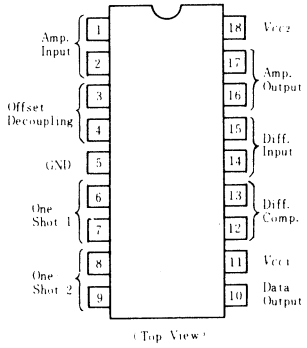
- Combined all the active circuit to perform the flexible disk read amplifier function in one chip.
- Direct connection with TTL's.

■BLOCK DIAGRAM

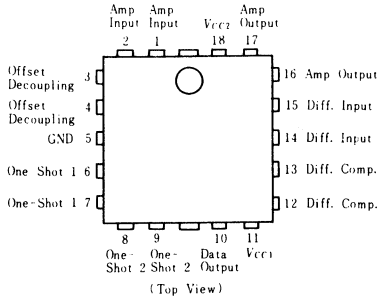


■PIN ARRANGEMENT

●HA16631P



●HA16631MP



■ MAXIMUM RATINGS (Ta=25℃)

Item	Symbol	Rating	Unit
Power Supply Voltage (Pin 11)	V_{CC1}	7.0	V
Power Supply Voltage (Pin 18)	V_{CC2}	16	V
Input Voltage (Pins 1 and 2)	V_{IN}	−0.2 to +7.0	V
Output Voltage (Pin 10)	V_O	−0.2 to +7.0	V
Differential Input Voltage (Pins 1 and 2)	$V_{IN(diff)}$	0 to +5.0	V
Operating Temperature	T_{opr}	0 to +70	℃
Storage Temperature	T_{stg}	−55 to +125	℃

■ ELECTRICAL CHARACTERISTICS

● Operating Power Supply Voltage Range (Ta=25℃)

Item	Symbol	Test Condition	min	typ	max	Unit	Test Circuit
Power Supply Voltage Range	V_{CC1R}		4.75	5.00	5.25	V	
Power Supply Voltage Raoge	V_{CC2R}		10.0	12.0	14.0	V	

● Amplifier Section (Ta=25℃, V_{CC1}=5.0V, V_{CC2}=12.0V: unless otherwise specified)

Item	Symbol	Test Condition	min	typ	max	Unit	Test Circuit
Differential Voltage Gain	A_{VD}	f=250kHz, V_{IN}=5mVrms V_{CC1R} V_{CC2R}	80	110	140	V/V	2
Input Bias Current	I_{IB}	V_{CC2}=12V, V_{CM}=4V	—	1	9	μA	4
Common Mode Voltage Range	V_{CM}		1.85	—	6.2	V	2
Output Distortion Ratio	THD	f=1kHz, V_{IN}=25mVp-p V_{CC1R} V_{CC2R}	—	1.5	5	%	2
Differential Output Voltage Swing	V_{OD}	V_{CC1R} V_{CC2R}	3.0	4.2	—	Vp-p	2
Output Source Current	I_O		—	8.0	—	mA	8
Output Sink Current (Pins 16 and 17)	I_{OS}	V_{CC1R} V_{CC2R}	2.8	4	—	mA	9
Input Resistance	r_{IN}		30	120	—	kΩ	5
Output Resistance	r_o		—	15	—	Ω	6
Common Mode Rejection Ratio	$CMRR$	f=100kHz, V_{IN}=200mVp-p	50	—	—	dB	11
Power Supply Rejection Ratio V_{CC1}	$PSRR_1$	V_{CC}=12.0V 4.75V≦V_{CC1}≦5.25V	50	—	—	dB	10
Power Supply Rejection Ratio V_{CC2}	$PSRR_2$	V_{CC1}=5.0V 10.0V≦V_{CC2}≦14.0V	60	—	—	dB	10
Differential Output Offset Voltage	V_{DO}		—	—	0.4	V	7
Common Mode Output Voltage	V_{CO}		—	3.1	—	V	7
Effective Differential Emitter Resistance (Pins 3 and 4)	R_{EFF}		370	570	770	Ω	3

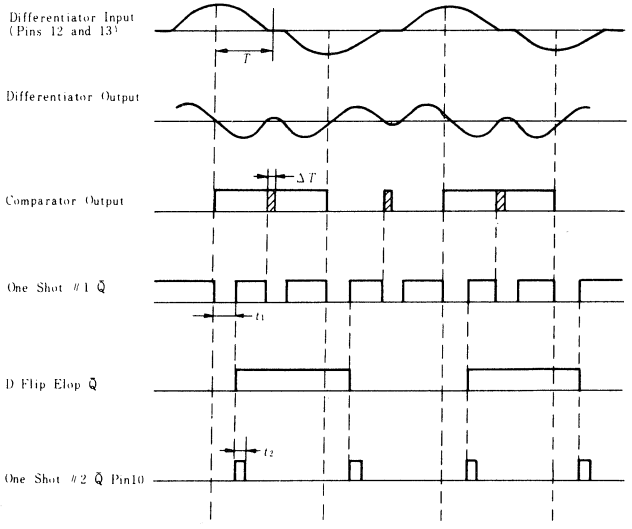
● Peak Detector Section (Ta=25℃, V_{CC1}=5.0V, V_{CC2}=12.0V: unless otherwise specified)

Item	Symbol	Test Condition	min	typ	max	Unit	Test Circuit
Sink Current (Pins 12 and 13)	I_{SD}		1.0	1.5	—	mA	12
Peak Shift	P_S	f=250kHz, V_{IN}=1.0Vp-p	—	—	5	%	13
Input Resistance	r_{ID}		—	30	—	kΩ	17
Output Resistance	r_{OP}		—	40	—	Ω	

●Waveform Shaper Section (Ta=25°C, V_{CC1R}, V_{CC2R}: unless otherwise specified)

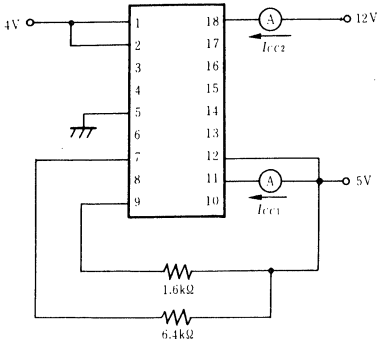
Item	Symbol	Test Condition	min	typ	max	Unit	Test Circuit
Output Voltage H (Pin 10)	V_{OH}	V_{CC1}=4.75V V_{CC2}=12.0V, I_{OH}=−0.4mA	2.7	—	—	V	15
Output Voltage L (Pin 10)	V_{OL}	V_{CC1}=4.75V V_{CC2}=12.0V, I_{OL}=8mA	—	—	0.5	V	16
Rising Time (Pin 10)	t_{TLH}	V_{CC1}=5.0V, V_{CC2}=12.0V V_{out}=0.5V→2.7V	—	—	25	ns	14
Falling Time (Pin 10)	t_{THL}	V_{CC1}=5.0V, V_{CC2}=12.0V V_{out}=2.7V→0.5V	—	—	25	ns	14
Timing Range #1	$t_{1A,B}$	f=125kHz	600	—	2000	ns	
		f=250kHz	600	—	1000	ns	
Timing Accuracy #1	t_1	t_1=0.625C_1R_1+150 C_1=200pF, R_1=6.8kΩ	850	1000	1150	ns	14
Timing Capacitance #1	C_1		150	—	680	pF	14
Timing Resistance #1	R_1		1.5	—	10	kΩ	14
Timing Range #2	$t_{2A,B}$	f=125kHz	150	—	1000	ns	
		f=250kHz	150	—	750	ns	
Timing Accuracy #2	t_2	t_1=0.625C_1R_1 C_1=200pF, R_1=1.6kΩ	170	200	230	ns	14
Timing Capacitance #2	C_2		100	—	800	pF	14
Timing Resistance #2	R_2		1.5	—	10	kΩ	14

■TIMING CHART

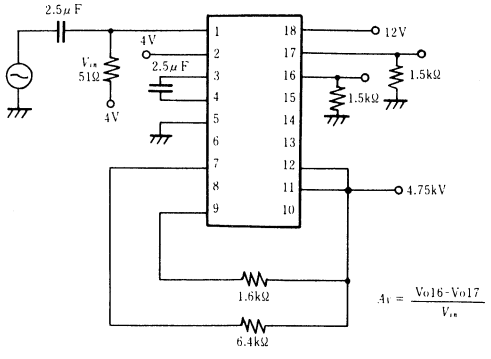


■ TEST CIRCUITS

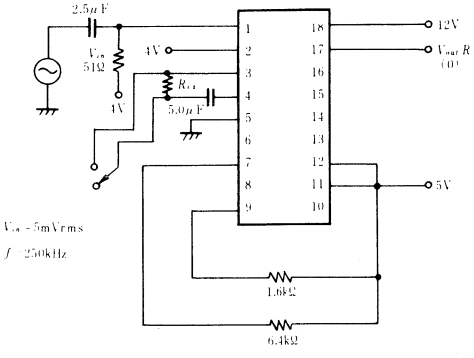
1. Power Supply Current



2. Voltage Gain, Band-width, Output Voltage Swing, Output Distortion Ratio



3. Pre-Amplifier Section Effective Emitter Resistance (Pins 3 and 4)



V_{in} = 5mVrms
f = 250kHz

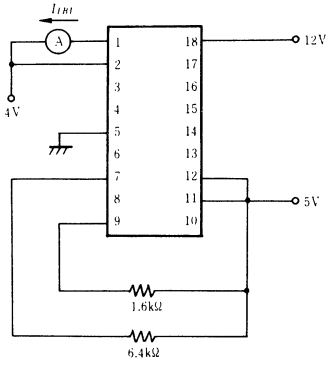
$$\frac{A_V}{2} = \frac{V_{out}}{V_{in}}$$

$$r_e + R_{e1} = \frac{R_{e1}}{\frac{A_{vo}}{A_{vf}} - 1}$$

$$= \frac{500}{\frac{V_{out}O}{V_{out}R} - 1}$$

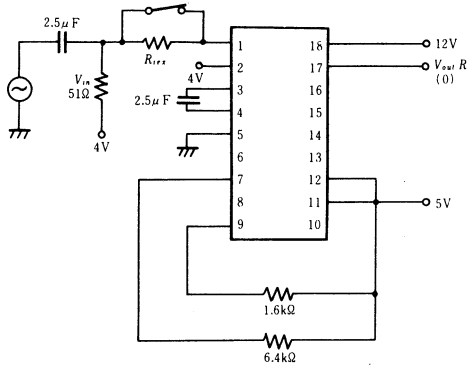
R_{e1} = 500Ω

4. Input Bias Current



Measure I_{IB2} in the same way.

5. Input Resistance

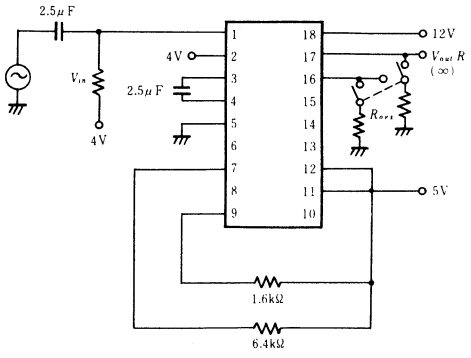


$$V_{IN} = \frac{V_{out}R \cdot R_{ref}}{V_{out}O - V_{out}R}$$

$$= \frac{R_{ref}}{\frac{V_{out}O}{V_{out}R} - 1}$$

$R_{ref} = 100k\Omega$

6. Output Resistance

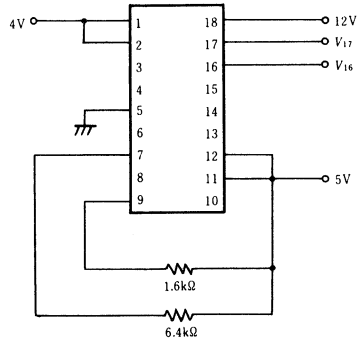


$$V_{out} = \frac{V_{out} - V_{out}R}{V_{out}R} \cdot R_{ref}$$

$$= R_{ref}(V_{out}^{\infty}/V_{out}R - 1)$$

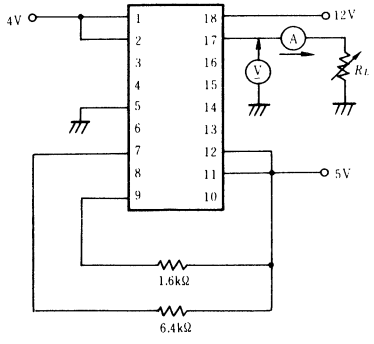
$R_{ref} = 500\Omega$

7. Differential Output Offset Voltage, Common Mode Output Voltage



$V_{DO} = |V_{17} - V_{16}|$

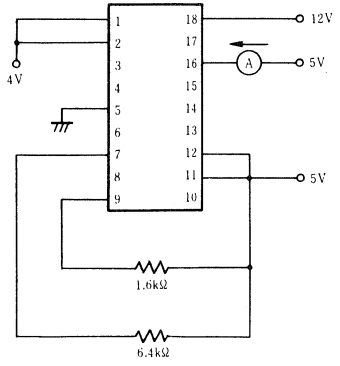
8. Output Source Current



Measure Pin16 in the same way. $R_{CO}: V_{17}^{(\infty)}$

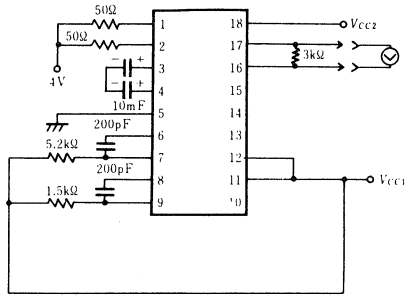
$|V_{17}^{(\infty)} - V_{17}^{(R)}| \leq 0.1V$

9. Output Sink Current



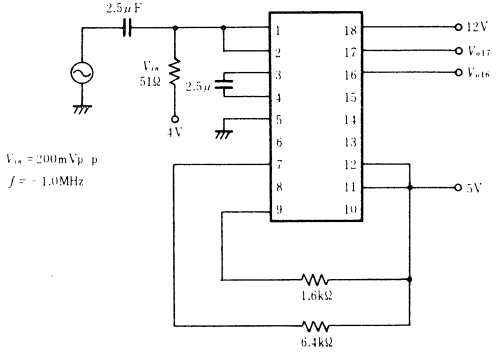
Measure Pin12 in the same way.

10. Power Supply Rejection Ratio



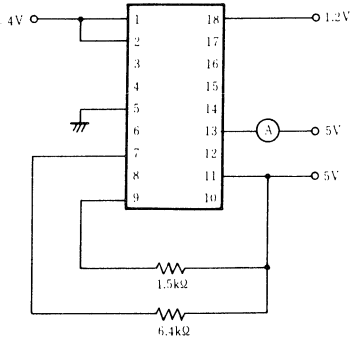
Fluke 8375A
Digital Multimeter

11. Common Mode Rejection Ratio



$$CMRR = 20\log_{10}\frac{100V_{in}}{V_{o16} - V_{o17}}$$

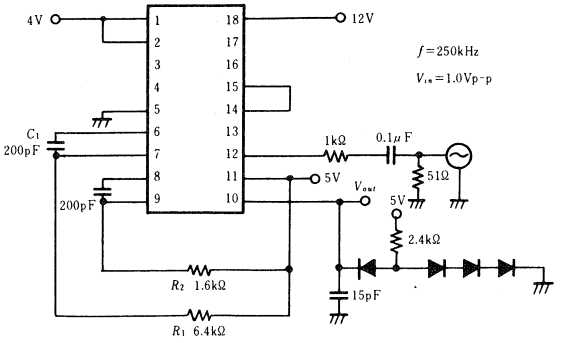
12. Differentiator Output Sink Current

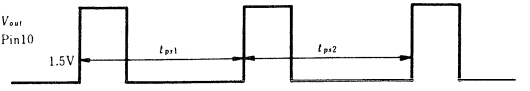


Measure Pin12 in the same way.

Measurement is performed using Vector Voltmeter hp8405A, or equivalent.

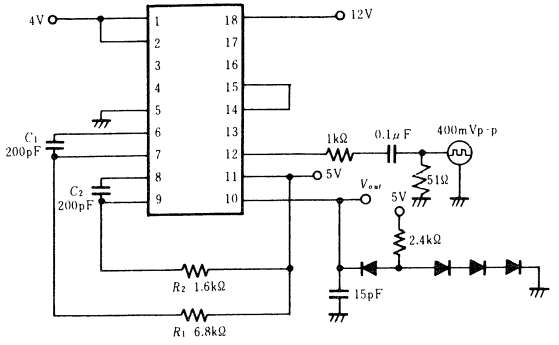
13. Peak Shift





$$PS = 1/2 \cdot \frac{t_{ps1} - t_{ps2}}{t_{ps1} + t_{ps2}} \times 100\%$$

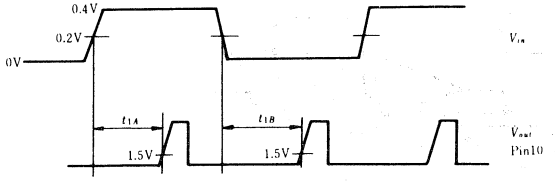
14. Timing Accuracy, Rising Time, Falling Time

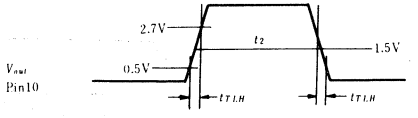


$t_{TLH} = t_{THL}$ 10ns

f=250kHz

50% Duty



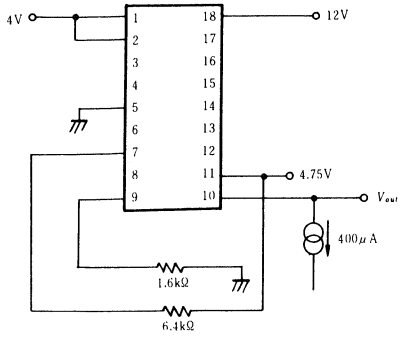


$$Et_{1A} = \frac{t_{1A}}{1{,}000\text{ns}} \times 100\%$$

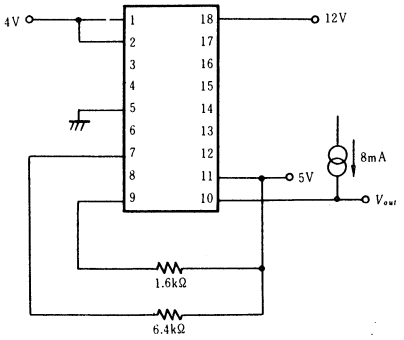
$$Et_{1B} = \frac{t_{1B}}{1{,}000\text{ns}} \times 100\%$$

$$ET2 = \frac{t_2}{200\text{ns}} \times 100\%$$

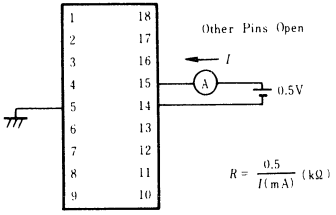
15. Output Voltage H (Pin 10)



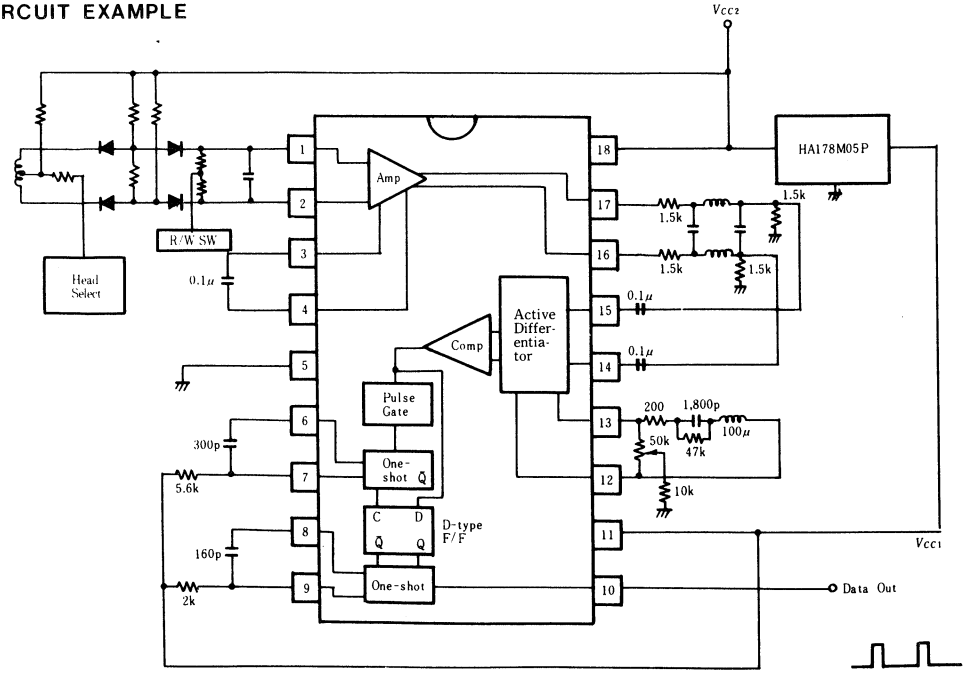
16. Output Voltage L (Pin 10)



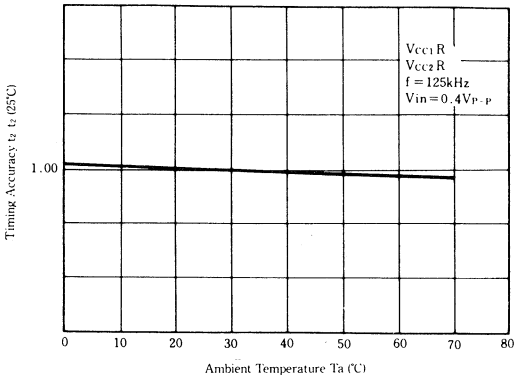
17. Input Resistance



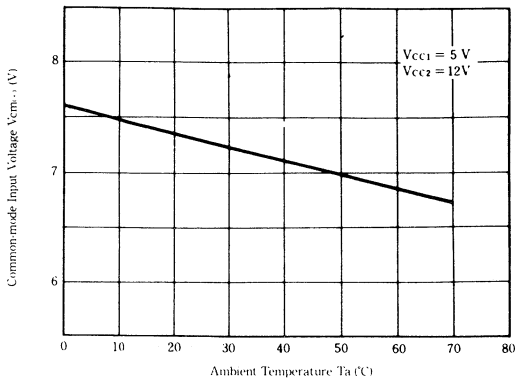
■ CIRCUIT EXAMPLE



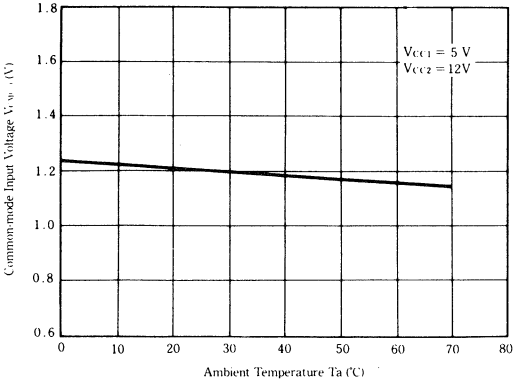
TIMING ACCURACY VS. AMBIENT TEMPERATURE



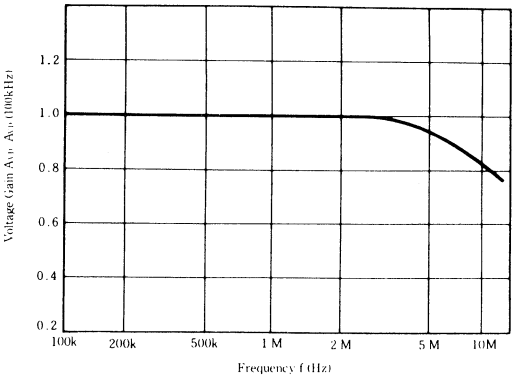
COMMON-MODE INPUT VOLTAGE VS. AMBIENT TEMPERATURE



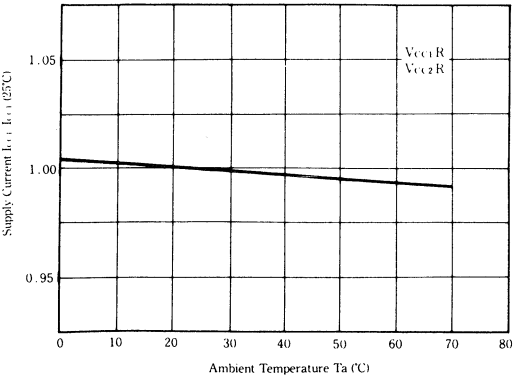
COMMON-MODE INPUT VOLTAGE VS. AMBIENT TEMPERATURE



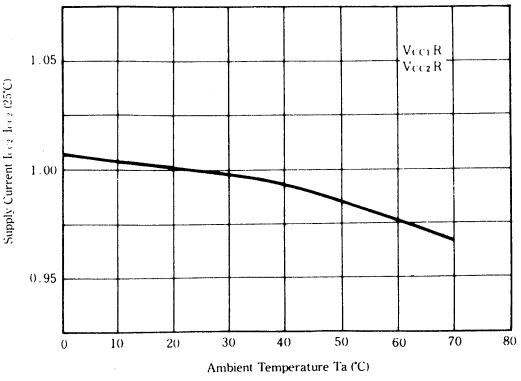
VOLTAGE GAIN VS. FREQUENCY



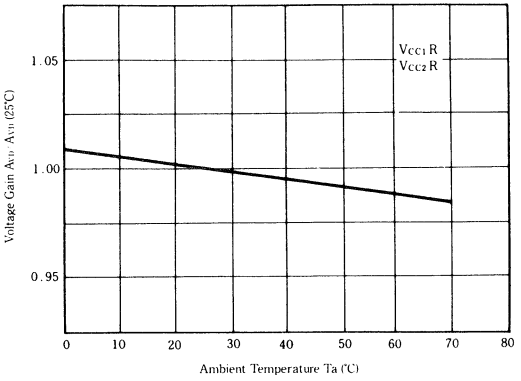
SUPPLY CURRENT VS. AMBIENT TEMPERATURE (1)



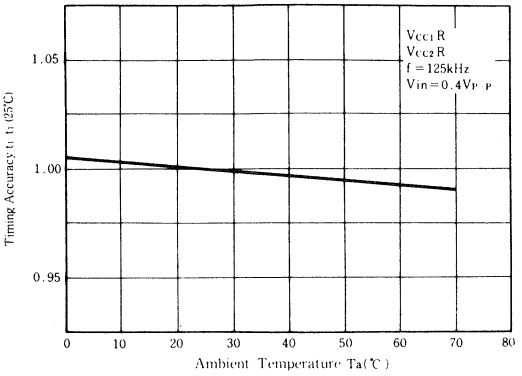
SUPPLY CURRENT VS. AMBIENT TEMPERATURE (2)



VOLTAGE GAIN VS. AMBIENT TEMPERATURE

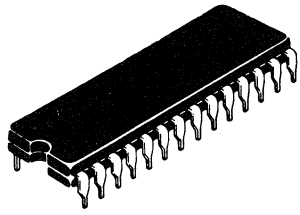


TIMING ACCURACY VS. AMBIENT TEMPERATURE



HA16632AP ● VOF IC for Floppy Disk Drive

The HA16632AP is a monolithic VFO IC for floppy disk interface. It is designed to accept the read out data from floppy disk drive, which includes jitter caused by the wow and flutter of the disk revolution, or peak shift by the magnetic effect on the disk. And it generates "Window" signals which are necessary to separate data pulse from clock pulse.



(DP-28)

■ FEATURES

- Applicable to both the 8 inch disk and the 5.25 inch disk by changing the voltage level "high" or "low" on the control pin.
- Applicable to both the single density record format and the double density record format by changing the voltage level "high" or "low" on the control pin.
- Applicable to various floppy disk controllers such as FD1791, μPD765 by changing the voltage level "high" or "low" on the control pin.
- Gate units in the IC chip are constructed by Low power schottky TTL circuits.

■ MAXIMUM RATINGS ($Ta=25°C$)

Item	Symbol	Rating	Unit
Power Supply Voltage 1	V_{CC}	7	V
Power Supply Voltage 2	V_{LNR}	7	V
Power Dissipation	P_T	750	mW
Operating Temperature Range	$Ta\text{-}op$	0 to +60	°C
Storage Temperature Range	T_{stg}	−55 to +125	°C

■ ELECTRICAL CHARACTERISTICS ($Ta=25°C$)

Item	Symbol	Test Conditions	min	typ	max	Unit	Application Terminal	Note
Operating Power Supply Voltage	$V_{CC(op)}$		4.75	5.00	5.25	V	V_{CC}, V_{LNR}	
Quiescent Current 1	I_{CC}	$V_{CC}=5.25V$	—	80	105	mA	V_{CC}	
Quiescent Current 2	I_{LNR}	$V_{CC}=5.25V$	—	28	37	mA	V_{LNR}	
Input High Current 1	I_{IH1}	$V_{CC}=5.25V$, $V_{IH}=2.7V$	—	—	20	μA	−RAW DATA −VFO SYNC −MFM	
Input High Current 2	I_{IH2}	$V_{CC}=5.25V$, $V_{IH}=5.25V$, −IRS=3.0V	—	—	50	μA	−8 INCHI −FSHA	
Input High Current 3	I_{IH3}	$V_{CC}=5.25V$, $V_{IH}=5.25V$	—	—	260	μA	−IRS	
Input Low Current 1	I_{IL1}	$V_{CC}=5.25V$, $V_{IL}=0.4V$	−0.4	—	—	mA	−RAW DATA −VFO SYNC −MFM	
Input Low Current 2	I_{IL2}	$V_{CC}=5.25V$, $V_{IL}=0.4V$, −IRS=3.0V	−1.8	—	—	mA	−8 INCHI −FSHA	
Input Low Current 3	I_{IL3}	$V_{CC}=5.25V$, $V_{IL}=0.4V$	−4.0	—	—	mA	−IRS	
Input Bias Current	I_{IB}	$V_{LNR}=5.25V$, $V_{IN}=2.4V$	—	—	20	μA	V_{IN}	
Output High Voltage 1	V_{OH1}	$V_{CC}=4.75V$, $I_{OH}=-280\mu A$	2.7	—	—	V	+WIND −RD DATA	1
Output High Voltage 2	V_{OH2}	$V_{CC}=4.75V$, $I_{OH}=-400\mu A$	2.7	—	—	V	−PDL, −PDH	1
Output High Voltage 3	V_{OH3}	$V_{CC}=4.75V$, $I_{OH}=-100\mu A$	3.4	4.0	—	V	+PUL	1

Note: 1. When setting the last output tap gate "High"

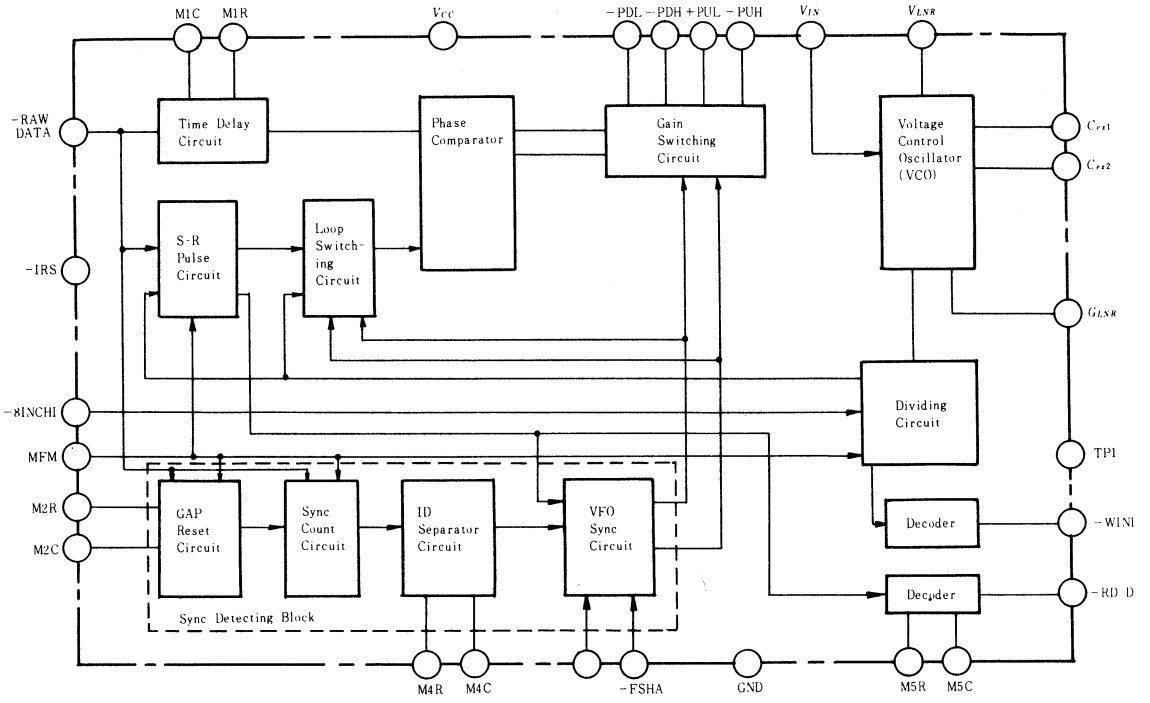
(to be continued)

■ELECTRICAL CHARACTERISTICS (Continued) (Ta=25°C)

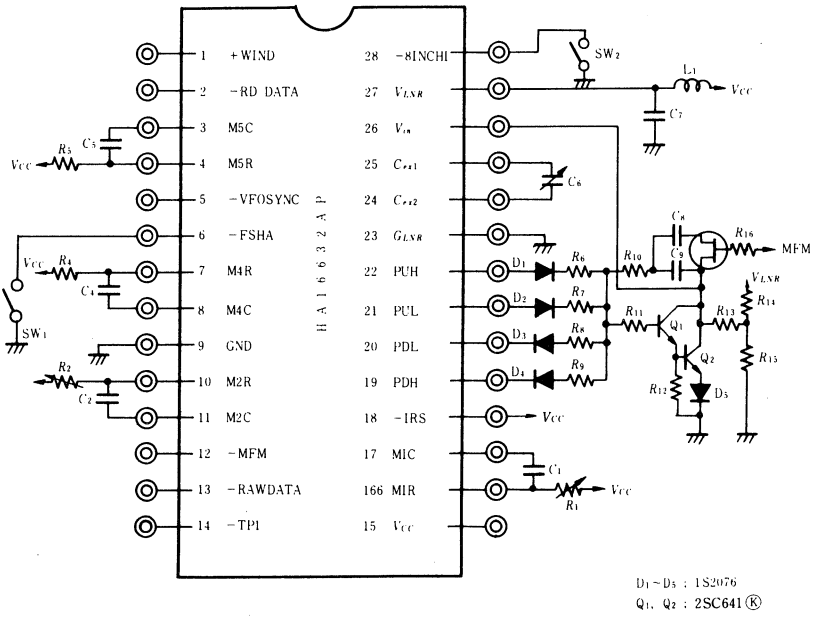
Item	Symbol	Test Conditions	min	typ	max	Unit	Application Terminal	Note
Output Low Voltage 1	V_{OL1}	V_{CC}=4.75V, I_{OL}=1mA	—	—	0.45	V	+WIND −RD DATA	2
Output Low Voltage 2	V_{OL2}	V_{CC}=4.75V, I_{OL}=1mA	—	—	0.45	V	−PDL	2
Output Low Voltage 3	V_{OL3}	V_{CC}=4.75V, I_{OL}=100μA	—	—	0.6	V	+PUL	2
Output Low Voltage 4	V_{OL4}	V_{CC}=4.75V, I_{OL}=100μA	—	—	0.6	V	+PUH	2
Output High Voltage 4	V_{OH4}	V_{CC}=4.75V, I_{OH}=−4mA	3.15	3.65	—	V	+PUH	1
Output Low Voltage 5	V_{OL5}	V_{CC}=4.75V, I_{OL}=4mA	—	—	0.55	V	−PDH	2
Output Short-circuit Current 1	I_{OS1}	V_{CC}=5.25V, +WIND, −RD DATA=GND	−70	—	−14	mA	+WIND −RD DATA	3
Output Short-circuit Current 2	I_{OS2}	V_{CC}=5.25V, −PDL, −PDH=GND	−100	—	−20	mA	−PDL −PDH	3
Output Short-circuit Current 3	I_{OS3}	V_{CC}=5.25V, +PUL, +PUH=GND	−100	—	−20	mA	+PUL +PUH	3
VCO Oscillation Frequency	f_{VCO}	V_{LNR}=5V, Cex=91pF V_{IN}=2.4V, −IRS=GND	—	4.0	—	MHz	−8 INCHII	
Maximum VCO Oscillation Frequency	$f$max	V_{LNR}=5V, Cex=30pF V_{IN}=4.0V, −IRS=GND	10	—	—	MHz	−8 INCHI	
M1 Output Pulse Width 1	$t_{W1\ 8}$	V_{CC}=5V, C_1=50pF VR 1=15kΩ, −IRS=GND	—	500	—	ns	+WIND	
M1 Output Pulse Width 2	$t_{W1\ 5}$	V_{CC}=5V, C_1=62pF VR 1=30kΩ, −IRS=GND	—	1000	—	ns	+WIND	
M2 Output Pulse Width 1	$t_{W2\ 8}$	V_{CC}=5V, C_2=240pF VR 2=25kΩ, −IRS=GND	—	2.50	—	μs	−RD DATA	
M2 Output Pulse Width 2	$t_{W2\ 5}$	V_{CC}=5V, C_2=500pF VR 2=25kΩ, −IRS=GND	—	5.0	—	μs	−RD DATA	
M4 Output Pulse Width 1	$t_{W4\ 8}$	V_{CC}=5V, C_4=34000pF VR 4=47kΩ, −IRS=GND	—	0.50	—	ms	TP 1	
M4 Output Pulse Width 2	$t_{W4\ 5}$	V_{CC}=5V, C_4=68000pF VR 4=47kΩ, −IRS=GND	—	1.0	—	ms	TP 1	
M5 Output Pulse Width	t_{W5}	V_{CC}=5V, C_5=12pF VR 5=15kΩ, −IRS=3.0V	—	200	—	ns	−RD DATA	

Notes 1. When setting the last output tap gate "High"
2. When setting the last output tap gate "Low"
3. When setting the last output tap gate "High"

■ BLOCK DIAGRAM

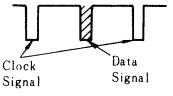


■ PIN ARRANGEMENT



$D_1 \sim D_5$: 1S2076
Q_1, Q_2 : 2SC641Ⓚ

PIN EXPLANATION

Item	Pin Name	Signal	Remarks
Pin for Power Supply	V_{CC}	Power Supply for every block except VCO block	
	GND	GND for every block except VCO block	
	V_{LNR}	Power Supply for VCO block	
	G_{LNR}	GND for VCO block	
Pin for Input Signal	−RAW DATA	Raw read data signal from flexible disk drive, including signal components of clock signal and data signal.	
	−VFO SYNC	Input signal which shows detection of SYNC Byte (periodic signal). When −FSHA="Low", this signal switches gain to lead-in loop. −VFO SYNC="Low"→ SYNC Byte detected −VFO SYNC="High"→ SYNC Byte undetected	
	−MFM	Mode select pin for MFM or FM -MFM="Low"→ MFM mode (double density) -MFM="High"→ FM mode (single density)	
	−8 INCHI/(−VCO)	1. Select pin for 8 inchi FDD or 5inchi FDD (−IRS="High") -8 INCHI="Low"→8 inchi FDD −8 INCHI="High"→5 inchi FDD 2. VCO oscillation output monitor pin (−IRS="Low")	
	−FSHA	Select pin for the kinds of Flexible Disk Controller (FDC) −FSHA="Low"→FD1791, MB8876, 8877 −FSHA="High"→μPD765AC	

■ PIN EXPLANATION (Continued)

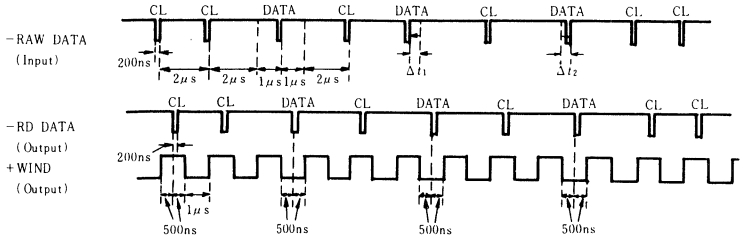
Item	Pin Name	Signal	Remarks
Pin for Input Signal	−IRS	Pin for testing IC's at using the packaged IC → −IRS = "High" at testing IC → −IRS = "Low"	
Input Pin	VIN	Control voltage input pin for VCO	
Pin for Output Signal	+WIND/(+M1Q)	1. Window signal output pin to distinguish data signal from signal which are included in −RAW DATA signal. +WIND = "High" → for distinguishing clock signal +WIND = "Low" → for distinguishing data signal (−IRS = "High") 2. Monostable Multivibrator Output Pulse Monitor pin for M1 (−IRS = "Low")	
	−RD DATA/(+M2Q)	1. Adjusted Read data output signal pin (−IRS = "High") 2. Monostable Multivibrator Output Pulse Monitor pin for M2 (−IRS = "Low")	
	−PDL	Output signal for charge pump down at Low Gain	
	−PDH	Output signal for charge pump down at High Gain	
	+PUL	Output signal for charge pump up at Low Gain	
	+PUH	Output signal for charge pump up at High Gain	
	TP1	IC test monitor pin	

■ PIN EXPLANATION

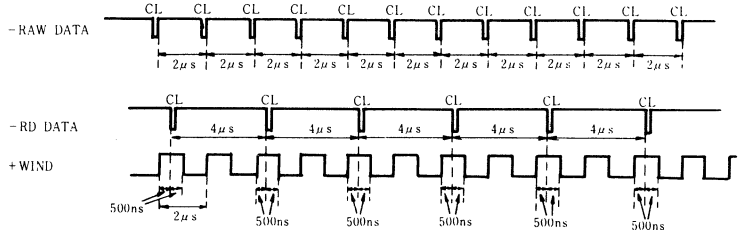
Item	Pin Name	Signal	Remarks
Resistor Capacitor	M1R	Ready access pin to capacitor and resistor M1	
	M1C	Ready access pin to capacitor for monostable multivibrator M1	
Ready Access Pin	M2R	Ready access pin to capacitor and resistor M2	
	M2C	Ready access pin to capacitor for monostable multivibrator M2	
	M4R	Ready access pin to capacitor and resistor M4	
	M4C	Ready access pin to capacitor for monostable multivibrator M4	
	M5R	Ready access pin to capacitor and resistor M5	
	M5C	Ready access pin to capacitor for monostable multivibrator M5	
	CEX1	Ready access pin to capacitor for VCO	
	CEX2	Ready access pin to capacitor for VCO	

■ TIME CHART

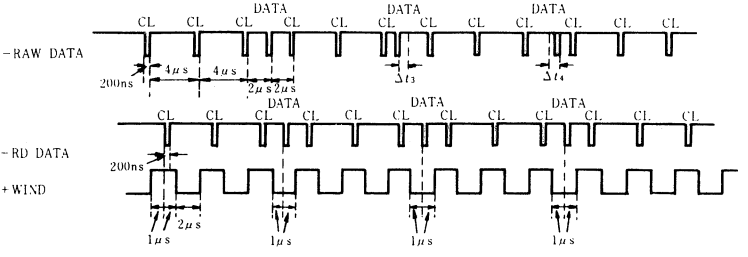
●Case 1 (8inchi, MFM, LOW Gain)



●Case 2 (8inchi, MFM, High Gain)····· SYNC Sig.

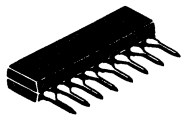


●Case 3 (8inchi, FM, LOW Gain)



HA16636P ●Ground Fault Interrupter

The HA16636P is a monolithic circuit designed for ground fault protection. It's applied for amplifier section of ground fault interrupter, and consists of differential amplifier and mono-stable multivibrator.



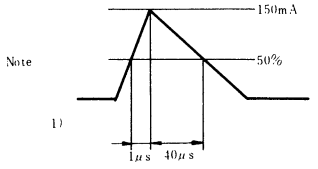
(SP-8)

■FEATURES

- Minimum external parts.
- Wide temperature range . . . . . −20°C ~ +85°C
- High packing density for SIP-8 package.
- Output pulse from mono-stable multivibrator . . . . . tow = 55ms typ, C = 0.68μF
- Temperature compensated for sensitivity of leakage current.
- High surge voltage and wide noise compensated.

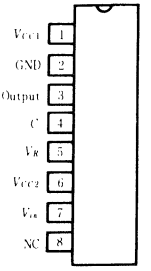
■ABSOLUTE MAXIMUM RATINGS ($Ta = 25°C$)

Item	Symbol	Rating	Unit	Note
Supply Current	I_{CC}	10	mA	
Excess Supply Current	I_Z	150	mA	1
Power Dissipation	P_T	100	mW	2
Operating Temperature Range	T_{opr}	−20 to +85	°C	
Storage Temperature Range	T_{stg}	−55 to +125	°C	



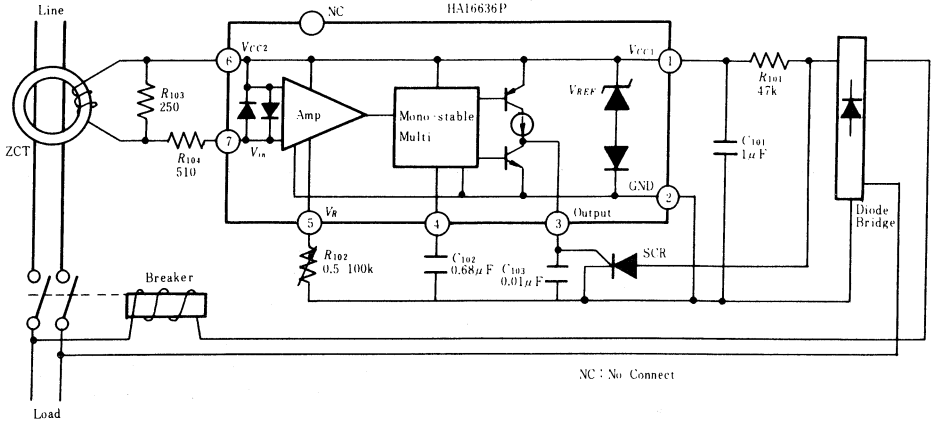
2. Temperature range ····· Topr

■PIN ARRANGEMENT



(Top View)

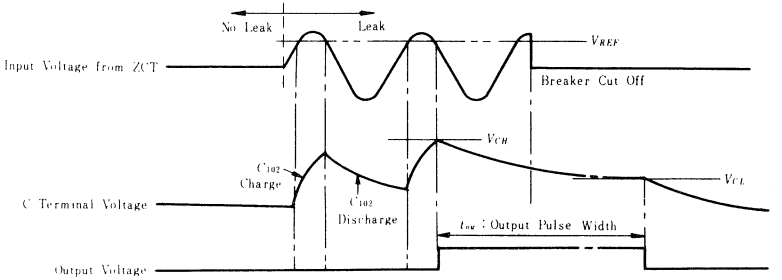
■BLOCK DIAGRAM AND APPLICATION CIRCUIT



●Outline of the Function

1. Both input terminal "Vcc2" (6) and "Vin" (7) of a differential amplifier connected the secondary coil of the Zero-phase Current Transformer (ZCT) that detect a leakage current. And further, "Vcc1" (1)and "Vcc2" (6)connected to each other inner this IC.
   So, if the appointed current are supplied, the terminal voltage of "Vcc1" (1) could fix the constant voltage by the zener diode.
2. Sensitivity of a leakage detection can adjusted by the external variable resistance (R102) that connected to the terminal "V_R". (5)
3. The signal that amplified by the differential amplifier integrated by the capacitor (R102) that connected to the terminal "C". (4)
   If the terminal voltage of "C" (4) amounted to the threshold voltage of the mono-stable multivibrator, a output pulse would generate with the capacitor C102 and the internal resistance and so, this pulse drive SCR that connected to the output terminal. (3)

●Operating Time Chart

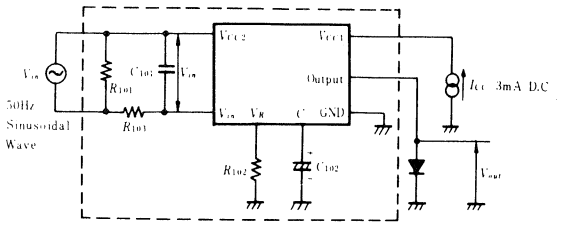


■ELECTRICAL CHARACTERISTICS ($Ta = 25°C$)

Item	Symbol	Test Conditions	min	typ	max	Unit
Operating Supply Current Range	I_{CC}		1.3	—	10	mA
Refference Voltage	V_{REF}	I_{CC} = 1.3mA, V_C = 2V, V_{OH} = 0.8V	5.6	6.3	6.8	V
Output Source Current	$I_{SOURCE1}$	I_{CC} = 1.3mA, V_{OH} = 0.8V	245	400	—	μA
	$I_{SOURCE2}$	Ta = −20°C, I_{CC} = 1.3mA, V_{OH} = 0.9V	290	500	—	μA
Output Voltage	V_{OL1}	I_{CC} = 1.3mA, I_{sink} = 2mA	—	0.1	0.2	V
	V_{OL2}	I_{CC} = 3V, I_{sink} = 300μA	—	0.05	0.2	V
	V_{OH}	I_{CC} = 1.3mA, No-Load	3.5	—	—	V
Output Pulse Width	t_{OW}	I_{CC} = 1.3mA, C = 0.68μF	30	55	100	ms
Temperature Characteristic	V_{in} Ta 1	Ta = −20°C, I_{CC} = 3mA*	−12	—	12	%
	V_{in} Ta 2	Ta = 70°C, I_{CC} = 3mA*	−12	—	12	%
	V_{in} Ta 3	Ta = 85°C, I_{CC} = 3mA*	−18	—	18	%

* refer to measuring circuit

■MEASURING CIRCUIT



●External Parts Constant

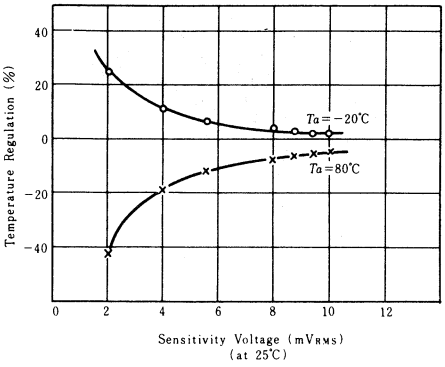
R101 = 250Ω ± 1% (Carbon Film Resistor)
R102 = Adjusted Resistance ±5% (Carbon Film Resistor)
R103 = 510Ω ±1% (Carbon Film Resistor)
C101 = 0.47μF ± 1% (Tantalum Electrolytic Capacitor)
C102 = 0.68μF ± 1% (Tantalum Electrolytic Capacitor)

●Temperature Coefficient

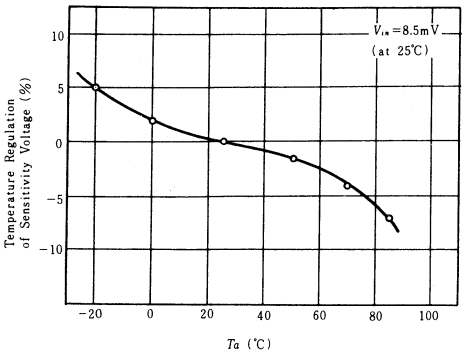
$$= \frac{Vin(Ta) - Vin(25°C)}{Vin(25°C)} \times 100[\%]$$

(Ta = −20°C, 70°C, 85°C)

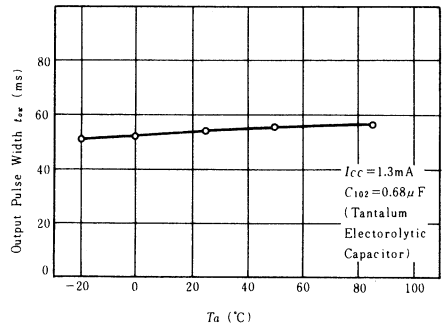
SENSITIVITY VOLTAGE CHARACTERISTICS



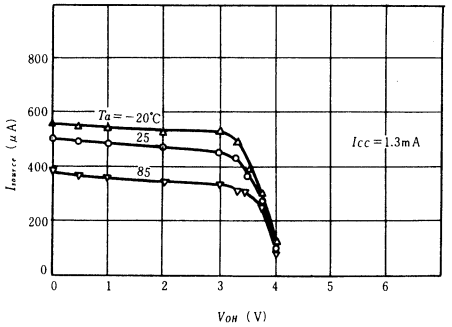
TEMPERATURE REGULATION OF SENSITIVITY VOLTAGE CHARACTERISTICS



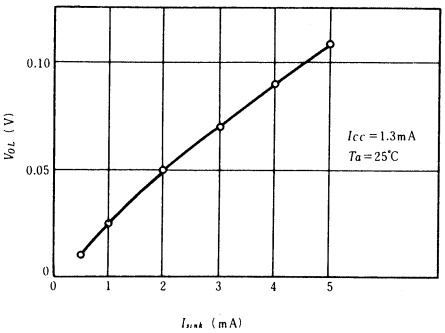
Tow-Ta CHARACTERISTICS



OUTPUT CHARACTERISTICS



OUTPUT CHARACTERISTICS

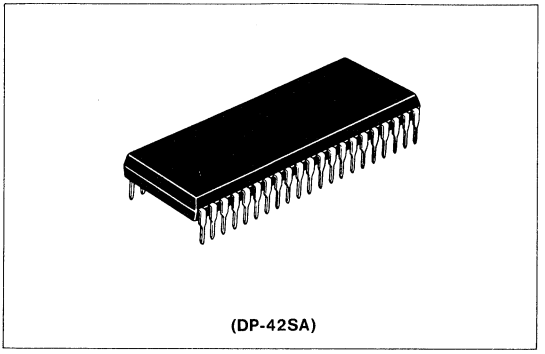


HA16640NT ● Write/Mechanism Controller for Floppy Disk Drive

This IC can provide WRITE + MECHANISM CONTROL function in one chip for FLOPPY DISK DRIVE

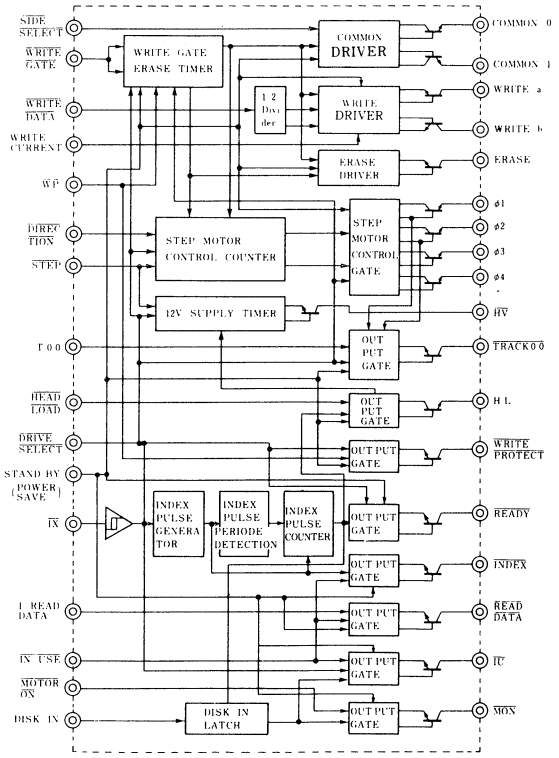
■ FEATURES

- WRITE Circuit includes COMMON, WRITE, ERASE drivers, and has capability of application for many kind of FDDs.
- WRITE Circuit also includes tripple power supply monitor circuits, so can protect the Disk from abnormal writing or erasing at ON, OFF of supply voltage.
- The delay time between write gate and erase gate timing is generated by internal MONO MULTI Circuit, so this IC is able to apply for many kind of FDDs and HEAD components.
- The function of MECHANISM CONTROL circuit conforms to the standard FDD's interface.
- MECHANISM CONTROL Circuit has a power save function, and at the stand-by mode in operation, power save circuit protects the equipment from internal temperature increasing by inhibiting the load current in external components, and also reduces the power dissipation in IC chip.
- The output interface has capability of large drive current, and internal logic circuit has low power consumption by means of Bi-CMOS technology. Especially, in the output interface circuit, it is not necessary to have any external TTL ICs because of including line drivers into IC chip.
- With this device, it is able to design the print circuit board without TTL ICs, and to reduce many external components, also to shrink an area of print circuit board.
- Signal processing and control circuit in FDD are able to be constructed with only two ICs and some external discrete devices by connecting with FDD READ IC, HA16631P/MP.



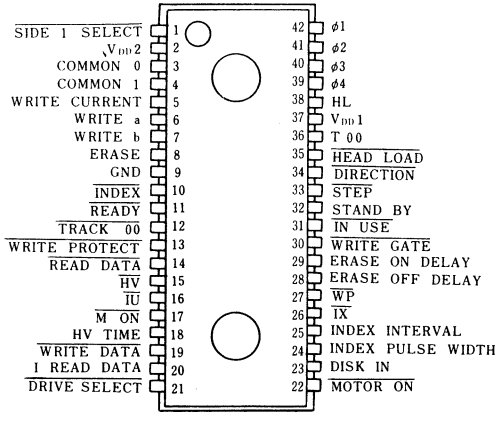
(DP-42SA)

■ BLOCK DIAGRAM



* In the WRITE CIRCUIT, power supply monitor circuits are included to watch the line voltage of 5V and 12V. When the line voltage goes down to abnormal value, the COMMON, WRITE, ERASE drivers are all inhibited rapidly.

■ PIN ARRANGEMENT



(Top View)

■ ABSOLUTE MAXIMUM RATINGS (T_a = 25°C)

Item	Symbol	Ratings	Unit	Applicable Terminal
Supply Voltage	V_{DD1}	−0.3, +7.0	V	V_{DD1}
Supply Voltage	V_{DD2}	−0.3, +14.0	V	V_{DD2}
Interface Input Voltage	V_{IN1}	−0.3 to V_{DD1}	V	Note 1
Interface Input Voltage	V_{IN2}	−0.3 to V_{DD2}	V	Note 2
Interface Output Current	I_{OL1}	50	mA	Note 3
$\overline{IU}$ Terminal Output Current	I_{OL2}	20	mA	$\overline{IU}$
$\overline{HV}$ Terminal Output Current	I_{OL3}	15	mA	$\overline{HV}$
$\overline{MON}$ Terminal Output Current	I_{OL4}	5	mA	$\overline{MON}$
HL Terminal Output Current	I_{OH5}	10	mA	HL
STEP Terminal Output Current	I_{OH6}	5	mA	$\phi1$ $\phi2$ $\phi3$ $\phi4$
COMMON Drive Current (WRITE MODE)	I_{OCW}	100	mA	COMMON 0, 1
COMMON Drive Current (READ MODE)	I_{OCR}	5	mA	COMMON 0, 1
WRITE Drive Current	I_{OWW}	10	mA	WRITE a,b
ERASE Drive Current	I_{OEW}	85	mA	ERASE
Input Current on the WRITE Current Set Terminal	I_{WC}	2.5	mA	WRITE CURRENT
Power Dissipation	P_D	850 (0 to 50°C)	mW	
Operating Temperature Range	T_{OP}	0 to +70	°C	
Storage Temperature Range	T_{stg}	−55 to +125	°C	

Notes 1. Applicable Terminal: $\overline{\text{SIDE SELECT}}$, $\overline{\text{WRITE DATA}}$, $\overline{\text{STEP}}$, $\overline{\text{DIRECTION}}$, $\overline{\text{IN USE}}$, $\overline{\text{MOTOR ON}}$, $\overline{\text{HEAD LOAD}}$, $\overline{\text{STAND BY}}$, $\overline{\text{WRITE GATE}}$, $\overline{\text{DRIVE SELECT}}$, $\overline{\text{I READ DATA}}$

2. Applicable Terminal: T00, DISK IN, $\overline{WP}$, $\overline{IX}$ and also Terminals from MM circuit connecting with the external C,R time constant.

3. Except for $\overline{IU}$, $\overline{HV}$, $\overline{MON}$, HL, $\phi1$ $\phi2$ $\phi3$ $\phi4$.

■ ELECTRICAL CHARACTERISTICS (T_a = 25°C)

Circuit Block		Item	Symbol	Test Condition	min	typ	max	Unit
WRITE Circuit	Supply Voltage	Supply Voltage Range	V_{DD1}		4.5	5.0	5.5	V
		Supply Voltage Range	V_{DD2}		10.8	12.0	13.2	V
	COMMON Driver	Output Voltage at Selected WRITE Mode	V_{OCW}	V_{DD2} = 12V I_{OCW} = −100mA	–	10.7	–	V
		Output Voltage at Unselected WRITE Mode	V_{OCWU}	V_{DD2} = 12V Unselected	–	–	0.7	V
		Output Voltage at Selected READ Mode	V_{OCR}	V_{DD2} = 12V I_{COR} = −5mA	–	4.7	–	V
		Output Voltage at Unselected READ Mode	V_{OCRU}	V_{DD2} = 12V Unselected	–	–	0.7	V
		Output Current Range	I_{COM}		–	–	100	mA
	WRITE Driver	Input Current Range on the WRITE Current Set Terminal	I_{WC}		0	–	2.5	mA
		WRITE Current Accuracy	I_{OWW}	WRITE Driver output voltage = 10V I_{WC} = 1mA	3.6	4.0	4.4	mA
		WRITE Current Temperature Coefficient	TCI_{OW}	I_{WC} = 1mA T_a = 0 to 70°C	–	±0.05	–	%/°C
		WRITE Current Symmetry	ΔI_{OW}	V_{DD1} = 5V, V_{DD2} = 12V I_{owa}-I_{owb}	−1	–	+1	%
		Output Leak Current	I_{LKW}	V_{DD1} = 5V, V_{DD2} = 12V V_{OW} = 20V	–	–	100	μA
	ERASE Driver	Output Low Voltage	V_{OLER}	V_{DD1} = 4.5V I_{OE} = 80mA	–	–	0.6	V
		Output Leak Current	I_{LKER}	V_{DD1} = 5.5V V_{OER} = 20V	–	–	200	μA
	Lower Line Voltage Protector	12V Detection Voltage	V_{PRV12}		–	8.1	–	V
		5V Detection Voltage	V_{PRV5}		–	3.8	–	V

(to be continued)

	Circuit Block	Item	Test Condition	Symbol	min	typ	max	Unit
Mechanism Control Circuit	Signal Interface (Note 1)	High Level Input Voltage	V_{DD1} = 5.0V	V_{IHI}	2.4	–	–	V
		Low Level Input Voltage	V_{DD1} = 5.0V	V_{ILI}	–	–	0.8	V
	Signal Interface (Note 1)	High Level Input Current	V_{DD1} = 5.5V V_{IH} = 5.5V	I_{HI}	–	–	10	μA
		Low Level Input Current	V_{DD1} = 5.5V V_{IL} = 0V	I_{ILI}	−10	–	–	μA
	Sensor Interface (Note 2)	High Level Input Voltage	V_{DD1} = 5.0V	V_{IHS}	3.3	–	–	V
		Low Level Input Voltage	V_{DD1} = 5.0V	V_{ILS}	–	–	1.7	V
		High Level Input Current	V_{DD1} = 5.5V V_{IH} = 5.5V	I_{IHS}	–	–	10	μA
		Low Level Input Current	V_{DD1} = 5.5V V_{IL} =0V	I_{ILS}	−10	–	–	μA
	Index Input Interface	Higher Threshold Voltage	V_{DD1} = 5V	V_{TH+IX}	–	3.5	–	V
		Lower Threshold Voltage	V_{DD1} = 5V	V_{TH-IX}	–	2.0	–	V
		Hysterisis	V_{DD1} = 5V	V_{HYS}	–	1.5	–	V
		Input Current	V_{DD1} = 4.5V V_{IH} = 2.6V	I_{IHIX}	−50	–	80	μA
	Signal Output Interface	Low Level Output Voltage	V_{DD1} = 4.5V I_{OL} = 48mA	V_{OLI}	–	-	0.4	V
		High Level Output Current	V_{DD1} = 5.5V V_{OH} = 5.5V	I_{OHI}	–	–	250	μA
	$\overline{IU}$ Output	Low Level Output Voltage	V_{DD1} = 4.5V I_{OL} = 10mA	V_{OLIU}	–	–	0.5	V
		High Level Output Current	V_{DD1} = 5.5V V_{OH} = 5.5V	I_{OHIU}	–	–	100	μA
	$\overline{HV}$ Output	Low Level Output Voltage	V_{DD1} = 4.5V I_{OL} = 15mA	V_{OLHV}	–	–	0.5	V
		High Level Output Current	V_{DD1} = 5.5V V_{OH} = 13.2V	I_{OHHV}	–	–	100	μA
	$\overline{MON}$ Output	Low Level Output Voltage	V_{DD1} = 4.5V I_{OL} = 5mA	V_{OLMN}	–	–	0.4	V
		High Level Output Current	V_{DD1} = 5.5V V_{OH} = 5.5V	I_{OHMN}	–	–	50	μA
	HL Output	High Level Output Voltage	V_{DD1} = 5V I_{OH} = −10mA	V_{OHHL}	3.6	–	–	V
		Low Level Output Current	V_{DD1} = 5.5V V_{OL} = 0V	I_{OLHL}	−20	–	–	μA
	STEP Output	High Level Output Voltage	V_{DD1} = 5V I_{OH} = −5mA	V_{OHSTP}	3.6	–	–	V
		Low Level Output Current	V_{DD1} = 5.5V V_{OL} =0V	I_{OLSTP}	−20	–	–	μA
	ERASE Timer	ERASE ON DELAY	Cex = 0.033μF Rex = 33kΩ	t_{EN}	0.44	0.52	0.60	ms
		ERASE OFF DELAY	Cex = 0.069μF Rex = 33kΩ	t_{EF}	0.91	1.07	1.23	ms
	INDEX, READY Circuit	Index Output Pulse Width	Cex = 0.033μF Rex = 220kΩ	t_{IXW}	2.61	3.08	3.55	ms
		Index Detection Period	Cex = 0.22μF Rex = 390kΩ	t_{IXI}	31.1	36.6	42.1	ms
	12V Hold Timer	Hold Period at 12V	Cex = 2.3μF Rex = 56kΩ	t_{HV}	47.1	55.5	63.9	ms
	Dissipation Current	Supply Current 1	V_{DD1} = 5.5V, V_{DD2} = 13.2V No Load	I_{DD1}	–	–	65	mA
		Supply Current 2	V_{DD1} = 5.5V, V_{DD2} = 13.2V No Load	I_{DD2}	–	–	10	mA

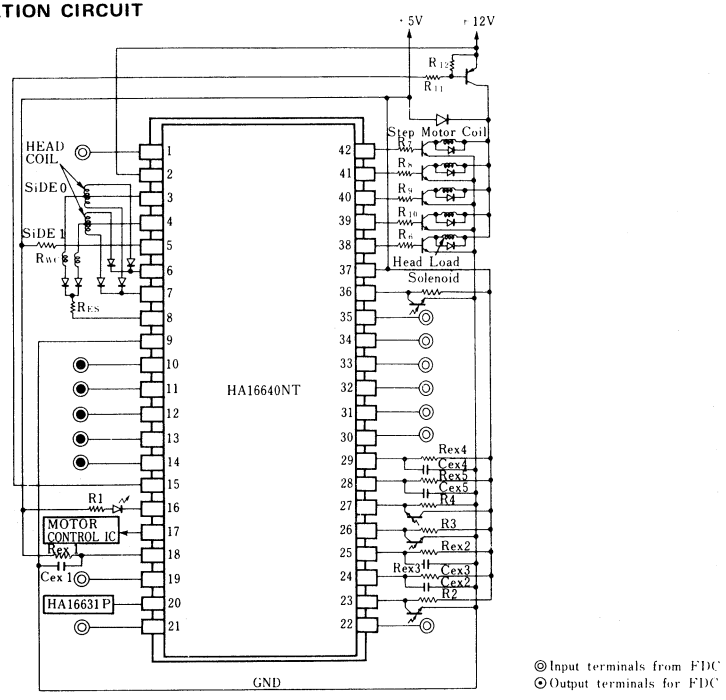
■ PIN DESCRIPTION

Symbol	Name	Description
COM 0	Common Driver 0	Output terminal of Common Driver (SIDE 0). During the Head Select signal is selecting SIDE 0, a common voltage appears on this terminal. The voltage value at WRITE Mode and that READ Mode are shown in the Electrical Characteristics. This terminal supplies a current which equals to write current + erase current. When the SIDE 0 is unselected, a common voltage doesn't appear, and this terminal is pulled down to ground by a internal resistor with high resistance.
COM 1	Common Driver 1	Output terminal of Common Driver. (SIDE 1). The function is as same as that of SIDE 0.
$\overline{\text{SIDE SELECT}}$	Side Select	Input terminal for Head Select signal. This signal selects the SIDE 0 or SIDE 1 of the common driver.
WRITE a, b	Write Driver a, b	Output terminal of Write Driver. The current multiplied by 4 with the determined current at the WRITE CURRENT terminal is sinked. WRITE a and WRITE b turn on alternately according to the Write Data "1" or "0".
ERASE	Erase Driver	Output terminal of Erase Driver. The drive transistor turns on during the period of Erase Gate signal keeping low, and the Erase Gate timing is generated by write Gate signal in IC circuit. This terminal has open collector NPN transistor, and erase current must be determined by an external resistor.
WRITE CURRENT	Write Current	The terminal to determine the Write Current. The Write current is determined with connecting an external resistor to +5V supply. The Write Current on the WRITE a, b terminals is multiplied by 4 with the current on the WRITE CURRENT terminal, as follow equation. $I_{OWW} = \frac{3.38}{Rex} \times 4$ (mA) where, I_{OWW}: WRITE CURRENT on the WRITE a, b terminals. Rex: External pull up resistor on the WRITE CURRENT terminal, and use the value in kΩ unit.
$\overline{\text{WRITE DATA}}$	Write Data Input	Write Data input terminal. The signal is devided through the F/F circuit in IC, and drives the Write Driver.
$\overline{\text{WRITE GATE}}$	Write Gate	Input terminal for Write Gate signal. The write gate is enable at input Low, and allows data writing. Erase Gate signal is generated with the determined delay from the negative and positive edge of Write Gate signal, and drives an erase driver.
$\overline{\text{WP}}$	Write Protect Input	Input terminal for the detected write protect signal from the Disk. Common, Write, Erase drivers are all inhibited at input low, and $\overline{\text{WRITE PROTECT}}$ driver turns ON.
ERASE ON DELAY	Erase ON Timer	Terminal for connecting the external time contact Cex, Rex of internal Mono Multi circuit to determine the delay time between the both negative edge of write Gate and Erase Gate signal. It is necessary to determine the delay time for the fittest value according to the kind of FDD and HEAD component.
ERASE OFF DELAY	Erase OFF Timer	As same as above, but the delay time is determined between the both positive edge of Write Gate signal and Erase Gate signal.
$\overline{\text{STEP}}$	Step Signal Input	Terminal for step pulse input to drive the stepping motor to seek tracks. With each one step pulse input, the driver outputs ϕ_1, ϕ_2, ϕ_3, ϕ_4 change sequentialy.
$\overline{\text{DIRECTION}}$	Direction Input	Input terminal for Direction signal to determine the direction of stepping motor revolution. Output drivers change with the direction of $\phi_1 \rightarrow \phi_2 \rightarrow \phi_3 \rightarrow \phi_4$ at the input low, and $\phi_1 \rightarrow \phi_4 \rightarrow \phi_3 \rightarrow \phi_2 \rightarrow \phi_1$ at the input High.
ϕ_1, ϕ_2, ϕ_3 ϕ_4	4 Phase Stepper Drive Output	Output terminals to drive the stepping motor coil. With each step pulse input, outputs change with the direction determined by Direction signal. Output driver has emitter follower construction, but the driver cannot drive the stepping motor coil directly. It is necessary to have external driver devices such as discrete transistors.
$\overline{\text{HV}}$	Voltage Change Timer	Timer output terminal to drive an external transistors which switches supply voltage 12V to 5V each other for stepping motor coil. With each step pulse input or each head load execution, the output turns ON during the determined period. It is enable to switch supply voltage 12V to 5V alternately and to supply 12V for the stepping motor coil during the period of Low level on this terminal.
HV TIME	HV Timer	Terminal for connecting the external time constant of internal Mono Multi circuit to determine the period of keeping the $\overline{\text{HV}}$ output Low level.
$\overline{\text{WRITE PROTECT}}$	Write Protect Output	When the input level of $\overline{\text{WP}}$ turns Low and the drive select is executed, this output turns ON.

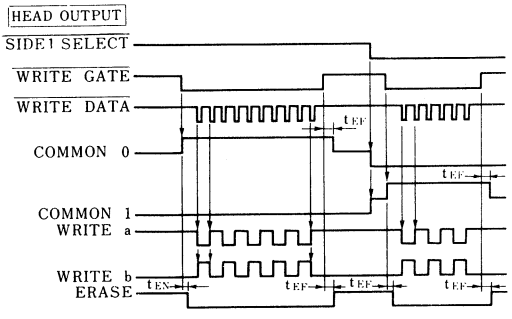
(to be continued)

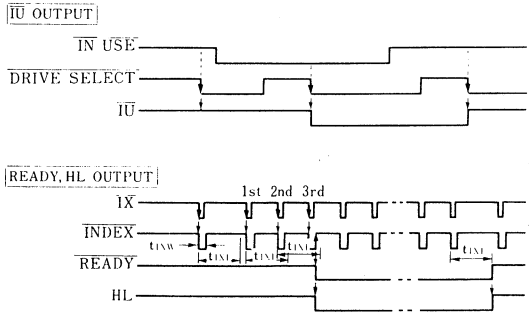
Symbol	Name	Description
T00	Track 00 Input	Input terminal for 00 track detection. High level input makes the 00 track detection.
$\overline{\text{TRACK 00}}$	Track 00 Output	Output terminal for 00 track detection. When the input level of T00 is High, and the both output ϕ_1, ϕ_2 are High, this output turns ON.
$\overline{\text{IX}}$	Index Input	Input terminal for the detected Index hole signal from the DISK. Input Low shows the hole detection.
$\overline{\text{INDEX}}$	Index Output	Output for the Index pulse. With each input of the detected Index pulse at the $\overline{\text{IX}}$ terminal, the width formed pulse appears on this terminal as a Index pulse.
INDEX PULSE WIDTH	Index Pulse Width Set	Terminal for connecting the external time constant of the internal Mono Multi circuit to determine the output pulse width on $\overline{\text{INDEX}}$. It is enable to adjust the pulse width independently to the diameter of the DISK hole.
$\overline{\text{READY}}$	Ready Output	Output of the Ready signal. When the disk revolution gets to the normal, after counting three index pulses, the output on this terminal turns ON, and shows FDD has gone into READY state. If the revolution goes down under the normal value, the output turns OFF rapidly and shows NOT READY state. And also the output shows High level continuously when Drive unit is not selected.
INDEX INTERVAL	Index Interval	Terminal for connecting the external time constant of the internal Mono Multi circuit to determine the reference index period corresponding to the standard revolution number of the DISK. In case of the FDD equipment having another revolution number, it is easier to adjust reference period by changing the time constant.
$\overline{\text{DRIVE SELECT}}$	Drive Select Input	Input terminal for Drive select signal. Input low makes the selected operation, and Write function, output interface, $\overline{\text{IU}}$ output are all enable.
STAND BY	Stand by Input	Input terminal for Power Save Signal to reduce the power consumption in FDD equipment and LSI. Input high inhibits all output terminals in Write and Mechanism control circuit except common driver, so power consumption in external circuit is reduced and this LSI makes itself into sleep mode. At the same time, common driver turns the READ mode.
$\overline{\text{HEAD LOAD}}$	Head Load	Input terminal for Head Load signal. When $\overline{\text{READY}}$ is low and operation is under the not stand-by mode, head load is enable at the input low.
HL	Head Load Output	Terminal for Head Load output. Circuit has a emitter follower construction. But this terminal cannot drive the coil of head load solenoid directly. It is necessary to have an external driving transistor.
$\overline{\text{IN USE}}$	In Use Input	Input terminal for IN USE signal. When the DISK is charged and the DRIVE equipment is selected, and also the operation is under the not stand-by mode, $\overline{\text{IU}}$ output is enable with the input low.
$\overline{\text{IU}}$	In Use Output	In Use Output. Circuit has a open collector NPN transistor, and can drive LED directly.
I READ DATA	Read Data Input	Input terminal for Read Data from READ circuit such as HA16631P/MP. When both $\overline{\text{DRIVE SELECT}}$ and STAND BY are Low, inverted read data pulses appear on the $\overline{\text{READ DATA}}$ terminal.
$\overline{\text{READ DATA}}$	Read Data Output	Output terminal for Read Data. Circuit has an open collector driver, and negative data pulses appear on this terminal.
DISK IN	Disk in Input	Input terminal for Disk charge detection signal. Input High shows the charged state. When the charged Disk is detected, $\overline{\text{MON}}$ output turns ON and the motor starts, and also $\overline{\text{IU}}$ output turns ON too. This function does not depend on the input level of $\overline{\text{MOTOR ON}}$ and $\overline{\text{IN USE}}$. When the Disk revolution gets to normal state, after counting eight Index pulses, both $\overline{\text{MON}}$ and $\overline{\text{IU}}$ outputs turns OFF, so the motor stops and IN USE LED turns OFF. After this operation, both $\overline{\text{MON}}$ and $\overline{\text{IU}}$ outputs depend on the input level of $\overline{\text{MOTOR ON}}$ and $\overline{\text{IN USE}}$. If the Disk is discharged, the motor stops and $\overline{\text{IU}}$ output is inhibited rapidly.
$\overline{\text{MOTOR ON}}$	Motor On	Input terminal for the motor ON, OFF, control signal. $\overline{\text{MON}}$ is enable at the input Low. Under the condition of the charged Disk and not-stand by, $\overline{\text{MON}}$ output turns ON with the $\overline{\text{MOTOR ON}}$ input Low.
$\overline{\text{MON}}$	Motor On Output	Output terminal for the motor ON, OFF, control signal. Circuit has an open collector NPN driving transistor. Output Low makes the motor ON and High makes OFF. Also this terminal is able to connect to the motor control IC, such as HA13431 and HA13432/MP.
V_{DD1}	5V Power Supply	5V Power Supply.
V_{DD2}	12V Power Supply	12V Power Supply.
GND	Ground	System ground

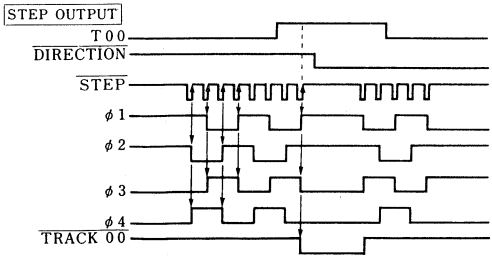
■ EXAMPLE OF APPLICATION CIRCUIT

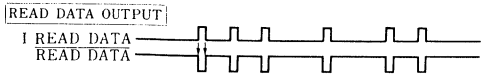


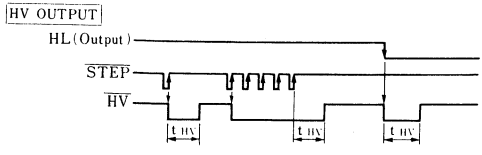
■ TIME CHART

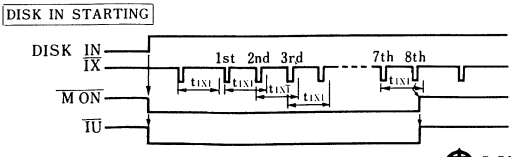








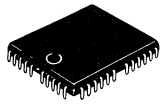




HA16642MP, HA16642NT ● Read/Write Functions for Floppy Disk Drive

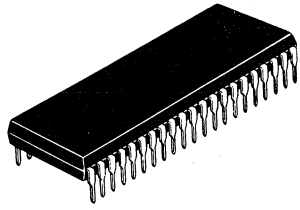
This IC can provide READ and WRITE functions in one chip for Floppy Disk Drive.

HA16642MP



(MP-44)

HA16642NT



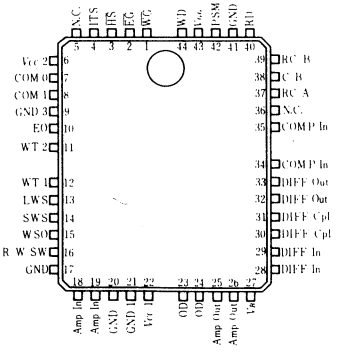
(DP-42SA)

■ FEATURES

- Read Amplifier has a differential voltage gain of 200 typ., which is avairable to adjust by gain select terminal.
- READ Circuit can be applied for the signal amplitude of 0.5mVpp to 10mVpp which is read out from HEAD COIL, so that this IC has superior capability to apply for a FDD less than 5 inches.
- In the read circuit, the peak shift is less than 1% for the signal amplitude, 0.5mVpp to 10mVpp, at the Amp input.
- In the WRITE circuit, the COMMON DRIVER, the WRITE DRIVER, and the ERASE DRIVER can provide a large current capability, so that can be applied to various kinds of FDD's.
- Write current can be established at any value according to the external resistor. The write current is independent of the supply voltage drift and temperature drift, with the built-in stabilizing circuit.
- This IC provides a function to reduce the write current at the inner track on the disk with a external switching signal. The reduce ratio of the write current can be established at any value with the external resistor.
- The WRITE GATE signal and the ERASE GATE signal can be applied independently each other.
- A dual-mode supply voltage monitor circuit is built-in, to inhibit a miss writing and a miss erasing at the power supply timing, ON and OFF, and the abnormal supply voltage.
- READ and WRITE functions are integrated in one chip, resulting in broad reduction of external components.

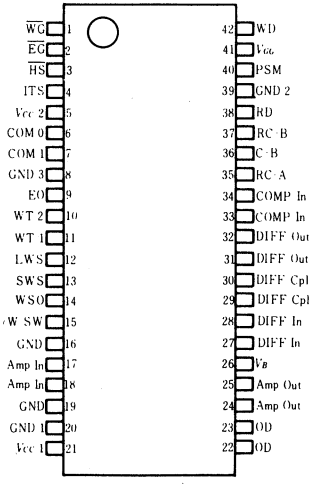
■ PIN ARRANGEMENT

● HA16642MP



(Top View)

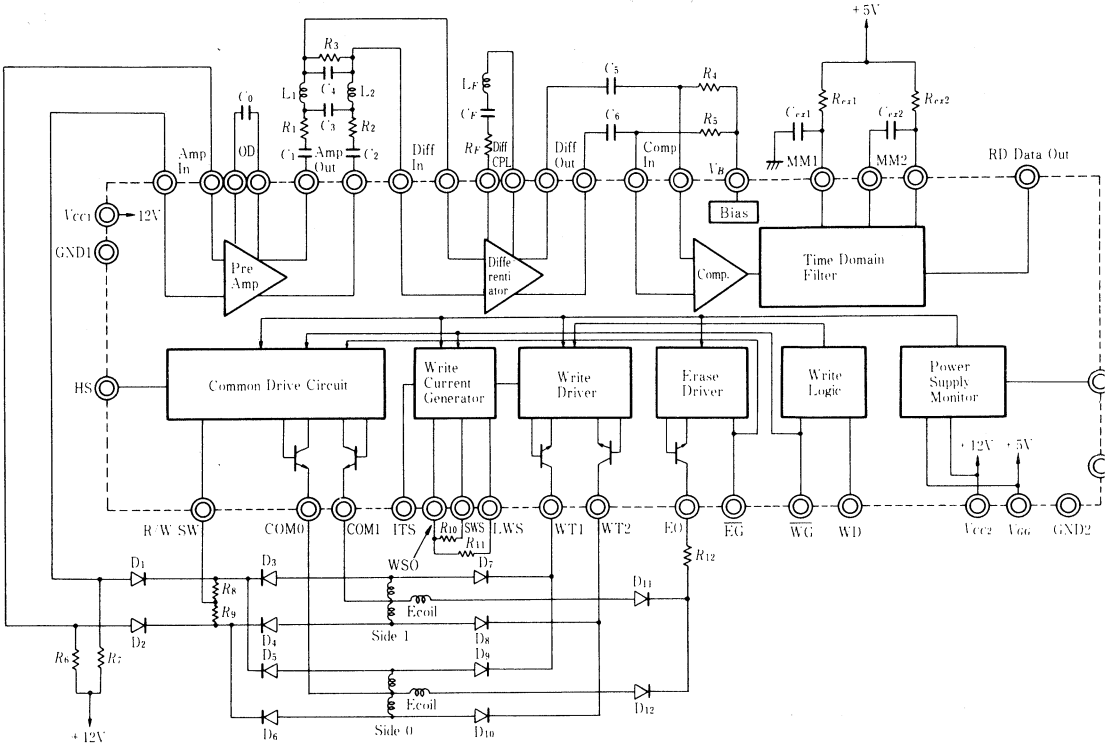
● HA16642NT



(Top View)

HITACHI

■BLOCK DIAGRAM AND APPLICATION CIRCUIT



: Integrated Blocks

R_8, R_9 : To determine a bias current for read mode

R_{10} : To determine the increase ratio of a write current at the inner track.

R_{11} : To determine a write current at the outer track.

(Write current at the inner track is a summation of the currents determined by R_{10} and R_{11} respectively.)

■ABSOLUTE MAXIMUM RATINGS (Ta=25℃)

Item	Symbol	Ratings	Unit	Applicable Terminal
Supply Voltage	V_{CC1}	7.0	V	V_{CC1}
Supply Voltage	V_{CC2}	16.0	V	V_{CC2}
Input Voltage	V_{IN}	−0.2 to +7.0	V	AMP IN
Differential Input Voltage	$V_{IN(diff)}$	0 to +5.0	V	AMP IN
Output Voltage	V_{out}	−0.2 to +7.0	V	RD DATA OUT
Common Drive Current	I_{COM}	150	mA	COM 0, COM 1
Write Drive Current	I_{WT}	15	mA	WT 1, WT 2
Erase Drive Current	I_{ER}	120	mA	EO
Power Dissipation	P_T	800	mW	V_{CC1}, V_{CC2}, V_{GG}
Operating Temperature Range	T_{opr}	0 to +70	℃	
Storage Temperature Range	T_{stg}	−55 to +125	℃	

■ELECTRICAL CHARACTERISTICS (Ta=25℃)

Circuit Block	Item	Symbol	Test Condition	min	typ	max	Unit
	Supply Voltage Range	V_{GG}		4.5	5.0	5.5	V
		$V_{CC1,2}$		10.5	12.0	13.5	V
Pre Amp.	Differential Voltage Gain	A_{VD}	f=250kHz, V_{in}=5mVrms		200		V V
	Input Bias Current	I_{IB}				15	μA
	Common Mode Input Voltage Range	V_{CM}		2.0	2.7	3.4	V
	Output Harmonic Distortion	THD	f=1kHz, V_{in}=10mVpp			5	%
Peak Detector	Peak Shift	PS	f=250kHz, V_{in}=0.5 to 10mVpp			2.5	%
Read Data Processor	Output Voltage	V_{OH}	V_{GG}=4.75V, I_{OH}=−400μA	2.7			V
		V_{OL}	V_{GG}=4.75V, I_{OL}=4mA			0.4	V
	Rising Time	t_{TLH}	V_{GG}=5V, V_{out}=0.4 to 2.7V		30		ns
	Falling Time	t_{THL}	V_{GG}=5V, V_{out}=2.7 to 0.4V		15		ns
	Timing Range #1	t_{1AB}	f=125kHz	1.3		4	μs
			f=250kHz	1.3		2	
	Timing Range #2	t_{2AB}	f=125kHz	0.15		1.5	μs
			f=250kHz	0.15		0.75	
Common Driver	Output Voltage at selected Write Mode	V_{WCMS}	V_{CC2}=12V, I_{COM}=120mA		11		V
	Output Voltage at unselected Write Mode	V_{WCMUS}	V_{CC2}=12V, at unselected			0.7	V
	Output Voltage at selected Read Mode	V_{RCMS}	V_{CC2}=12V, I_{COM}=1mA		2.7		V
	Output Voltage at unselected Read Mode	V_{RCMUS}	V_{CC2}=12V, at unselected			0.75	V
	Output Current Range	I_{COM}				150	mA
Erase Driver	Output Low Voltage	V_{OLE}	V_{GG}=5V, I_{OL}=100mA			0.5	V
	Output Leak Current	I_{OHE}	V_{OH}=12V, V_{GG}=5V			100	μA
	Erase Current Range	I_{ER}				120	mA
Write Driver	Write Current Accuracy	A_{CIW}	V_{GG}=5V, V_{CC2}=12V	−7		+7	%
	Write Current-Supply Voltage Sensitivity	P_{SIW}	V_{GG}=5V, V_{CC2}=10.8 to 13.2V		±1.5		% V
	Write Current-Temperature Coefficient	T_{CIW}	V_{GG}=5V, V_{CC2}=12V, Ta=0 to +70℃		±0.05		% ℃
	Write Current Symmetry	$\triangle I_{WT}$	V_{GG}=5V, V_{CC2}=12V, I_{WT1}-I_{WT2}	−1		+1	%
	Write Current Range	I_{WT}	V_{GG}=5V, V_{CC2}=12V	1		10	mA
	Leak Current at Off Driver	I_{okut}	V_{GG}=5V, V_{CC2}=12V, V_{WT}=20V			50	μA
Supply Voltage Monitor	Detection Voltage for 5V Supply	V_{MON1}	V_{CC2}=12V	3.5	3.9	4.3	V
	Detection Voltage for 12V Supply	V_{MON2}	V_{GG}=5V	8.0	9.0	9.8	V
Logic Input Gate	Input High Voltage	V_{IH}	V_{GG}=5V	2.0			V
	Input Low Voltage	V_{IL}	$\overline{WG}$, $\overline{EG}$			0.8	V
Schmitt Type Logic Input Gate	Input High Voltage	V_{IHS}	V_{GG}=5V	2.0			V
	Input Low Voltage	V_{ILS}	HS, WD			0.5	V
Dissipation Current	12V Supply	I_{CC}	V_{CC}=13.5V Read	–	25	40	mA
			V_{CC}=13.5V Write	–	16	–	
	5V Supply	I_{GG}	V_{GG}=5.5V Read	–	36	60	mA
			V_{GG}=5.5V Write	–	33	–	

■ PIN DESCRIPTION

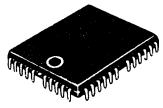
Symbol	Name	Description
AMP IN	Pre Amp Input	Terminal for differential input of pre amplifier in read circuit. A signal voltage picked up through R/W coil is applied.
OD	Gain Select	Terminal for DC offset compensation of pre amp, and for gain selection. The amp gain is available to be changed by connecting a resistor to the compensation capacitor in series.
AMP OUT	Pre Amp Output	Terminal for differential output of the pre amp in read circuit. A low pass filter is connected between the input terminal of differentiator and this terminal.
DIFF IN	Differentiator Input	Input terminal of differentiator in read circuit. Output voltage from the pre amp is applied to this terminal through the low pass filter.
DIFF CPL	Differential Coupling	Terminal for connecting a capacitor for differentiation. R_F, C_F and L_F are connected in series, as shown in the block diagram.
DIFF OUT	Differentiator Output	Output terminal of the differentiator. The differentiated signal is appeared on this terminal with the phase shifted by 90°. The output is coupled through the capacitor and is applied to the comparator input.
COMP IN	Comparator Input	Input terminal of the comparator in read circuit. A signal with the phase shifted by 90° through the differentiator is applied, and the zero-crossing point is detected. This terminal is pulled up to the bias source by the external resistor.
MM1	Mono Multi 1	A capacitor and a resistor are connected to these terminals. The capacitance and the resistance determine the output pulse width of the Pre Mono Multi Vibrator in the Time Domain Filter Circuit.
MM2	Mono Multi 2	A capacitor and a resistor are connected these terminals. The capacitance and the resistance determine the output pulse width of the Post Mono Multi Vibrator in the Time Domain Filter Circuit.
RD DATA OUT	READ Output	Output terminal of the read circuit. A pulse which is synchronized to the peak position of the read out signal from head coil is obtained. The output pulse width is determined by the external capacitor and resistor of MM 2. The signal output level is TTL compatible.
COM 0	Common Driver 0	Output terminal of Common Driver (SIDE 0). During the Head Select signal is selecting SIDE 0, a common voltage is appeared on this terminal. The voltage value at Write Mode and that at Read Mode are shown in the Electrical Characteristics. A current which equals to Write Current + Erase Current flows out from this terminal. When the SIDE 0 is unselected, a common voltage is not appeared, and this terminal is pulled down to ground by a high resistance in the IC.
COM 1	Common Driver 1	Output terminal of Common Driver (SIDE 1). The function is as same as that of COM 0.
$\overline{HS}$	Head Select	Input terminal for Head Select signal. This signal selects the SIDE 0 or SIDE 1 of the common driver. This terminal is consisted of Schmitt type input circuits. Input Low selects COM 1.
R/W SW	R/W Switch	A transistor output for switching the bias state in head coil and in diode SW circuit, according to READ/WRITE switching. This terminal is pulled down to ground level in READ Mode, and it is pulled up to 12V in WRITE Mode.
WSO	WRITE Regulated Voltage Output	Output from regulated supply source in Write Current Setting Circuit.
LWS	Low Current Set	Terminal to set a low level write current. The current is determined by connecting an external resistor $\bar{R}_{11}$ between terminal WSO and this terminal.
SWS	Difference Current Set	Terminal to set the current difference (I_{WDF}) between high level write current and low level write current. The difference current is determined by connecting an external resistor R_{10} between terminal WHO and this terminal. I_{WDF} = (High Level Write Current − Low Level Write Current) $I_{WH} = I_{WL} + I_{WDF}$ Where; I_{WH} is high level write current, and I_{WL} is low level write current. I_{WH}-to-I_{WL} current ratio is; $I_{WH}/I_{WL} = 1 + I_{WDF}/I_{WL}$ It can be set at any value by R_{10} and R_{11}.
ITS	Current Switch Signal Input	Input terminal for Write Current SW signal at inner & outer tracks. High Level Write Current is selected at input Low, and Low Level Write Current at input High.
WD	Write Data Input	Write Data Input Terminal. The signal is devided through the F/F circuit in the IC, and drives the Write Driver.

(to be continued)

Symbol	Name	Description
WT 1, 2	Write Driver 1, 2	Output terminal of Write Driver. The current determined by external resistors at terminal SWS and terminal MWS is sinked. WT 1 and WT 2 turns on alternately, according to the Write Data "1" or "0".
$\overline{WG}$	Write Gate	Input terminal for Write Gate signal. The write gate is enable at input Low, and allows data writing.
$\overline{EG}$	Erase Gate	Input terminal for Erase Gate signal. The erase gate is enable at input Low, and allows erasing.
EO	Erase Driver	Output terminal of Erase Driver. It turns on at erase gate input LOW. The output on this terminal is an open collector output of NPN transistor, and the erase current is determined by external resistor R_{12}.
PSM	Power Supply Monitor	The monitor circuit monitors the V_{GG} (+5V) and V_{CC2} (+12V), and will inhibit the common driver, the write driver and the erase driver when the supply voltage becomes abnormally low, and the FLAG signal will appear on this terminal PSM. The Driver Inhibit is released only when both V_{GG} and V_{CC2} are more that the specified voltages, regardless of the supply sequence.
V_{CC1}	Amp Voltage	Voltage for Pre Amp in read circuit.
V_{CC2}	Voltage for 12V	Another Voltage (Excepting for Pre Amp.)
V_{GG}	Voltage for 5V	
GND 1	Amp GND	GND for Pre Amp read circuit.
GND 2		GND for read circuit. (Excepting for Pre Amp.)
GND 3		GND for write circuit.

HA16643MP ●Mechanism Controller for Floppy Disk Drive

The HA16643MP is a monilithic mechanism control LSI for the floppy disk drive. It is designed to control the mechanism of FDD according to the input signals.

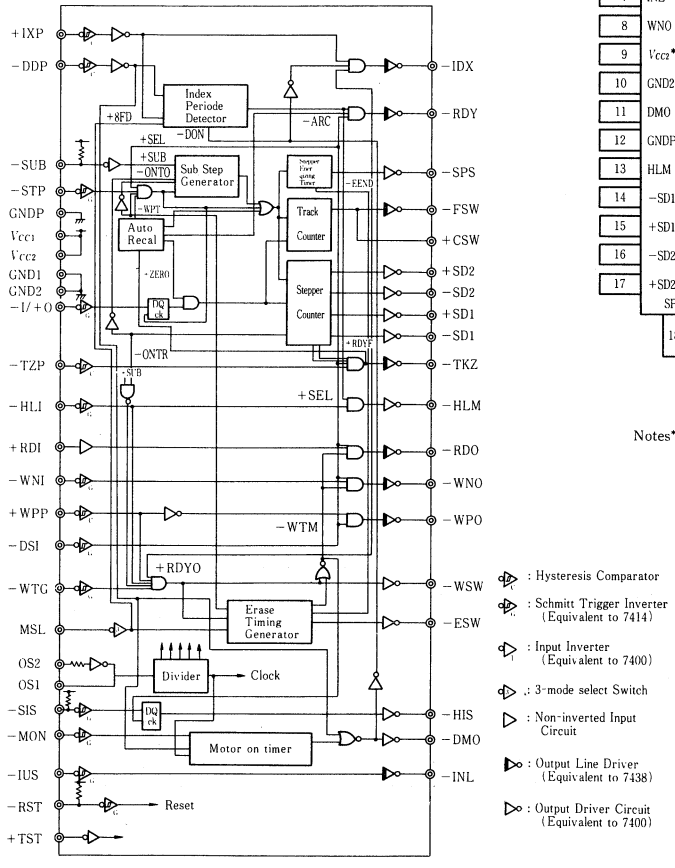


(MP-44)

■ FEATURES

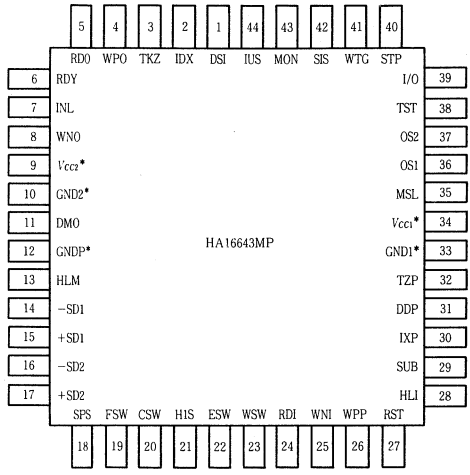
- Conform to FDD standard interface.
- Functional blocks are composed of CMOS logics.
- Bipolar line drivers equivalent to 7438 included.
- No external TTL IC.
- Input circuit is composed of the comparator with hysteresis.
- Oscillation circuit included for system clock, only required external ceramic resonator.
- High accurate internal timers by the clock count.
- Small outline package enables easy to design the PCB of FDD compactly.
- With the combination of our other FDD IC line-up, i.e. HA16642 (R/W) HA13421A (Stepper Driver), HA13431, 432 (Spindle motor control + driver) the PCB of FDD composed by only four IC's.

■BLOCK DIAGRAM



: Hysteresis Comparator
: Schmitt Trigger Inverter (Equivalent to 7414)
: Input Inverter (Equivalent to 7400)
: 3-mode select Switch
: Non-inverted Input Circuit
: Output Line Driver (Equivalent to 7438)
: Output Driver Circuit (Equivalent to 7400)

■PIN ARRANGEMENT



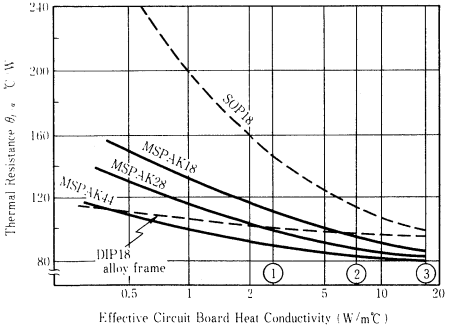
(Top View)

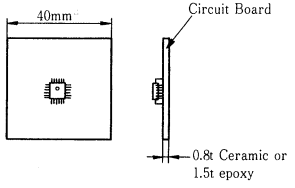
Notes*) V_{CC1} ·····Power supply for Bipolar circuits
V_{CC2} ·····Power supply for C-MOS circuits
GND_1 ····Ground for Bipolar circuits
GND_P·····Ground for high current output drivers
GND_2 ····Ground for C-MOS circuits

■ABSOLUTE MAXIMUM RATINGS (T_a=25°C)

Item	Symbol	Maximum Ratings	Unit	Note
Supply Voltage	V_{CC}	7	V	
Input Voltage	V_{IN}	5.5	V	1
Output Voltage	$V_{out\,1}$	7	V	2
Output Voltage	$V_{out\,2}$	7	V	3
Output Current	$I_{out\,1}$	50	mA	4
Output Current	$I_{out\,2}$	30	mA	5
Output Current	$I_{out\,3}$	5	mA	6
Output Current	$I_{out\,4}$	−40	mA	7
Input Voltage	$V_{in\ os}$	V_{DD}	V	8
Output Voltage	$V_{out\ os}$	V_{DD}	V	9
Input Voltage	$V_{in\ PL}$	V_{DD}	V	10
Power Dissipation	P_C	720	mW	11
Operating Temperature	T_{opr}	0 to +70	°C	
Storage Temperature	T_{stg}	−55 to +125	°C	
Maximum Operating Junction Temperature	T_{jopr}	135	°C	11

Notes) 1. Specificaiton value for the terminals such as schmitt gate input, input circuit equivalent to 7400 and MSL, TST input.
(・IXP, ・DDP, ・TZP, ・WPP)
(・STP, ・I ・O, ・RDI, ・WNI, ・DSI, ・HLI, ・WTG, ・MON, ・IUS)
2. Specification value for the output terminals when the open collector transistor turns off.
(・IDX, ・RDY, ・FSW, ・TKZ, ・RSO, ・WNO, ・WPO, ・INL)
3. Specification value for the terminals below at the high level condition.
4. Specification value for the terminals below when the open collector transistor turns on.
(・IDS, ・RDY, ・TKZ, ・RDO, ・WNO, ・WPO, ・INL)
5. Specification value for the FSW terminal when the open collector output gate turns on.
6. Specification value for the same terminals as Note.3 at the output low level.
7. Specification value for the same terminals as Note.3 at the output high level.
8. Specification value for the input terminal OS2.
9. Specification value for the output terminal OS1 at the high level.
10. Specification value for the input terminals with pull up resistances. The absolute value of the maximum ratings is 5.5V.
(・SUB, ・SIS, ・RST)
11. Power dissipation of mini-square package changes with the mounted condition, the kind of PCB and the pattern density on the PCB. So please use according to the derating curve and the thermal resistance data below.





① glass epoxy with 10% metallization density
② glass epoxy with 30% metallization density
③ 96% almina ceramic circuit board

■ELECTRICAL CHARACTERISTICS (T_a=25°C unless otherwise specified)

Item	Symbol	Test Condition	min	typ	max	Unit	Applicable Terminal	Note
Operating Supply Voltage	$V_{CC}-op$		4.5	5.0	5.5	V	$V_{CC\,1}$, $V_{CC\,2}$	
Input Threshold Voltage	V_{TCM+}	V_{DDB}=5V	−	1.8	−	V		
Input Threshold Voltage	V_{TCM-}	V_{DDB}=5V	−	1.7	−	V	+IXP, −DDP	
Hysteresis	$V_{TCM+}-V_{TCM-}$	V_{DDB}=5V	−	0.1	−	V	−TZP, +WPP	
Comparator Input Current	I_{IHCM}	V_{DDB}=5.5V, V_{IN}=4.0V	−	0.6	10	μA		
Comparator Input Current	I_{ILCM}	V_{DDB}=5.5V	−	−	1	μA		

(to be continued)

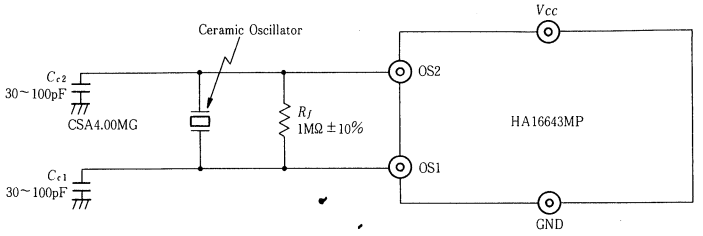
Item	Symbol	Test Condition	min	typ	max	Unit	Applicable Terminal	Note
"H" Level Input Voltage	V_{IHPG}		2.0	–	–	V	−SUB	
"L" Level Input Voltage	V_{ILPG}		–	–	0.8	V		
"H" Level Input Current	I_{IHPG}	V_{DDB}=5.5V V_{IL}=2.4V	−1	−0.3	–	mA		
"L" Level Input Current	I_{ILPG}	V_{DDB}=5.5V V_{IL}=0.4V	−1.6	−0.9	–	mA		
Input Threshold Voltage	V_{TST+}	V_{DDB}=5V	–	1.7	2.0	V	See Note 2	1
Input Threshold Voltage	V_{TST-}	V_{DDB}=5V	0.6	0.9	–	V		1
"H" Level Input Current	I_{IHST1}	V_{DDB}=5.5V V_{IH}=2.4V	–	–	40	μA		1
"L" Level Input Current (1)	I_{ILST1}	V_{DDB}=5.5V V_{IL}=0.4V	−1	−0.2	–	mA		1
"H" Level Input Current (2)	I_{IHST2}	V_{DDB}=5.5V V_{IH}=2.4V	−1	–	–	mA	−STS −RST	
"H" Level Input Current (3)	I_{IHST3}	V_{DDB}=5.5V V_{IH}= V_{DDB}	−50	–	+50	μA		
"L" Level Input Current (2)	I_{ILST2}	V_{DDB}=5.5V V_{IL}=0.4V	−1	–	–	mA		
"H" Level Input Voltage	V_{IHG1}		2.0	–	–	V	+RDI	
"L" Level Input Voltage	V_{ILG1}		–	–	0.8	V		
"H" Level Input Current	I_{IHG1}	V_{DDB}=5.5V V_{IH}=2.4V	–	–	400	μA		
"L" Level Input Current	I_{ILG1}	V_{DDB}=5.5V	−1.6	−0.4	–	mA		
Input Current (1)	I_{I1}	V_{DDB}=5.5V V_I=5.5V	–	0.2	1	mA	MSL	
Input Current (2)	I_{I2}	V_{DDB}=5.5V V_I=0V	−1	−0.2	–	mA		
Oxcillator Input Current	I_{IOSC}	V_{DDM}=5.5V V_I=3.0V	–	–	10	μA	OS2	
Oscillator Frequency	f_{OSC}	V_{DDM}=4.5V to 5.5V, Oscillator: CSA4.00MG, C_C=100pF, R_f=1MΩ	3.8	4.0	4.2	MHz	OS1, OS2	1
"H" Level Output Voltage (1)	V_{OHIG1}	V_{DDB}=4.75V, Output=High I_{OH}=−400μA	2.4	–	–	V	See Note 2	2
"H" Level Output Voltage (2)	V_{OHIG2}	V_{DDB}=4.5V, Output=High I_{OH}=−400μA	2.1	–	–	V		2
"L" Level Output Voltage	V_{OLIG}	V_{DDB}=4.5V, Output=Low I_{OL}=5mA	–	–	0.4	V		2
"L" Level Output Voltage	V_{OLBG}	V_{DDB}=4.5V, Output=ON, I_{OL}=50mA	–	–	0.4	V	See Note 3	3
"H" Level Output Current	I_{OHBG}	V_{DDB}=5.5V, Output=OFF, V_{OH}=5.5V	–	–	250	μA		3
RDO Output Delay Time	t_{pd}	V_{DDB}=5.5V, I_{OL}=48mA, V_{OH}=5.5V	–	–	1.0	μs	RDO	5
Quiescent Current	I_{CC1}	V_{DDB}=5.5V For Input/Output Signal level, see Note 5.	–	–	85	mA	V_{CC1}	4
Quiescent Current	I_{CC2}	V_{DDM}=5.5V IC operation at f=4MHz.	–	–	40	mA	V_{CC2}	4

Notes) 1. Specification values for the terminals below.
−STP, −I/+O, −WNI, −DSI, −HLI, −WTG, −MON, −IUS
2. Specified values for the following terminals.
−SPS, −DMO, +CSW, −SD2, +SD2, −SD1, +SD1, −HLM, −WSW, −ESW, −HIS
3. Values apply to the following terminals;
−IDX, −RDY, −TKZ, −RDO, −WNO, −WPO, −FSW, −INL.
4. Current specification values for the following Input/Output signal states.

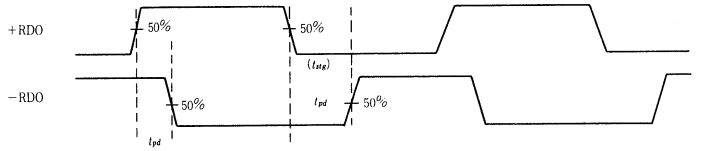
Input Terminal	Signal Level	Input Terminal	Signal Level	Output Terminal	Signal Level	Output Terminal	Signal Level
+IXP	"L"	−DSI	"L"	−IDX	"H"	−HLM	"H"
−DDP	"L"	−WTG	"L"	−RDY	"H"	−RDO	"L"*1
−SUB	"L"	MSL	Open	−SPS	"H"	−WNO	"L"*1
−STP	"L"	−SIS	"L"	−FSW	"H"	−WPO	"L"*1
−I/+O	"L"	−MON	"L"	+CSW	"L"*2	−WSW	"H"
−TZP	"L"	−IUS	"L"	+SD1	"L"*2	−ESW	"H"
−HLI	"L"	−RST	"H"	−SD1	"H"	−HIS	"L"*2
+RDI	"H"	+TST	"L"	+SD2	"L"*2	−DMO	"L"*2
−WNI	"L"			−SD2	"H"	−INL	"L"*1
+WPP	"H"			−TKZ	"L"*1		

*1 : I_{OL}=50mA
*2 : I_{OL}=5mA

TEST CIRCUIT



Note. 5. Read Data Input (+RDI) and Read Data Output (−RDO) waveforms are as follows.



PIN DESCRIPTION

Symbol	Pin No.	Name	Description
+IXP	30	Index Photo Input	Input terminal for the detected Index signal from the disk. Input "High" shows the Index detection.
−DDP	31	Disk Detect Photo Input	Input terminal for signal from the sensor which detect the diskchange Input "Low" shows the charged state. When the charged disk is detected, −DMO output turns "Low" during −MON input is keeping "Low". If the disk is discharged (−DDP input "High"), −DMO output turns off rapidly.
−SUB	29	Sub Step Control Input	Input terminal for the signal which selects Sub Step Pulse mode. When this input is "Low", sub step pulse is added and when input is "High", sub step pulse is not added. Normally sub step pulse is added after 3.072ms from each external step pulse in the sub step pulse mode. At this terminal a resistor is pulles up to the power supply line.
−STP	40	Step Signal Input	Input terminal for step signal which is sent by FDC. Which each one step pulse input, the driver output +SD1, +SD2, −SD1, −SD2 change to turn on sequentially.
−I/O	39	Direction Input (Inner or Outer)	Input terminal for Direction signal to determine the direction of stepping motor revolution. Output drivers change with the Inner Direction sequence of +SD1, +SD2, −SD1, −SD2 at the input "Low", and with the Outer Direction sequence of +SD1, −SD2, −SD1, +SD2 at the input "High".
−TZP	32	Track Zero Photo Input	Input terminal for 00 track detection signal. Low level input makes the 00 track detection.

(to be continued)

Symbol	Pin No.	Name	Description
+RDI	24	Read Data Input	Input terminal for Read Data from Read circuit. When −DSI (Drive Select Input) is "Low" and −WTG (Write Gate Input) is "High", inverted read data pulse stream appears on the −RDO terminal.
−WNI	25	Window Signal Input	Input terminal for Window signal from VFO. When −DSI is "Low" and −WTG is "High", this signal appears on the −WNO terminal through internal gates.
+WPP	26	Write Protect Photo Input	Input terminal for the detected Write Protect signal from the disk. −WTG signal is inhibited at this input "High" and −WPO output turns ON.
−SDI	1	Drive Select Input	Input terminal for Drive Select signal. Input "Low" makes the selected operation, and Write function and Output interface are all enable.
−HLI	28	Head Load Input	Input terminal for Head Load signal from FDC. When the spindle motor revolution goes to the normal, Head Load is enable at the input "Low". This signal "High" inhibits −WTG signal.
−WTG	41	Write Gate Input	Input terminal for Write Gate signal. The write driver is enable at input "Low", and allows data writing. Erase Gate signal is generated with the determined delay from the negative and positive edge of Write Gate signal. For example, this delay from the negative edge of Write Gate signal is 300μs and from the positive edge of Write Gate signal is 864μs at 3.5 inches mode (MSL input is open).
−MSL	35	Mode Select Input	Input terminal for the signal which selects the kind of delay of Erase Gate signal and the reference period of Disk revolution. Input "High" selects 8 inches mode, "Low" 5 inches mode and input Open 3.5 inches mode.
−SIS	42	Side Select Input	Input terminal for Head Select signal. This signal selects SIDE 0 or SIDE 1 in the double side FDD. This terminal is pulled up internally.
−MON	43	Motor On Input	Input terminal for Spindle Motor ON/OFF Control signal. Motor ON is enable at the input "Low". Under the condition of the charged disk (−DDP is "Low"), this signal is enable.
−IUS	44	Use LED Input	Input terminal for In Use signal. −INL output turns ON at the input "Low".
−RST	27	Power On Reset Input	Input terminal for Power ON Reset signal. This signal initializes all counters and Flip Flop circuits in the IC. This terminal is pulled up internally.
+TST	38	Test Mode Select	Test mode select pin. Input "High" selects test mode. Normal operation is made with this input keeping "Low".

(to be continued)

Symbol	Pin No.	Name	Description
−IDX	2	Index Output	Output terminal for Index pulse. This output is enable when the disk revolution reaches the normal state, and −MON, −DSI, and −DDP inputs are all "Low".
−RDY	6	Ready Output	Output terminal for Ready signal. Under the condition of −MON, −DSI and −DDP inputs "Low", when the disk revolution reaches the normal state (154ms~238ms Index period), the output on this terminal turns "Low" after counting two Index pulses, and indicates the FDD has gone into Ready state.
−SPS	18	Stepper Power Supply Output	Timer Output terminal to drive an external transistor switching supply voltage between +12V and +5V each other for stepping motor coil. With each step pulse input, the output turns ON during normally 32.768ms. It is enable to switch supply voltage +12V to +5V alternately and to supply +12V for the stepping motor coil during the period of Low level on this terminal.
−FSW	19	Filter Switch Output	Output terminal for Switch signal to switch the cut-off frequency of filter of Read Circuit. This signal is generated by preset data of track position.
+CSW	20	Current Switch	Output terminal for Write Current Switch signal. This signal is reversed against −FSW signal.
−TKZ	3	Track Zero Output	Output terminal for detected 00 Track signal. When the input level of −TZP is low and both outputs +SD1 and +SD2 are low, this output turns ON, and indicates the head is on the 00 track position.
−RDO	5	Read Data Output	Output terminal for Read Data. Circuit has an open collector driver, and negative data pulse appears on this terminal.
+SD1 −SD1 +SD2 −SD2	15 14 17 16	4-phase Stepper	Output terminals to drive the stepping motor coil. With each step pulse input, outputs change with the direction determained by Direction signal (−I/O). In sub step pulse mode, with each external step pulse and each sub step pulse, outputs change. Output drivers have no capability to drive stepping motor coil directly. It is necessary to have external driver devices such as discrete transistors.
−WNO	8	Window Signal Output	Output terminal for Window signal connected to FDC. When −DSI is "Low" and −WTG is "High", Window signal appears on this terminal.
−WPO	4	Write Protect Output	Output terminal for Write Protect signal. When the input level of +WPP is high and the drive select is executed, this output turns ON.
−HLM	13	Head Load Magnet Output	Output terminal for Head Load signal. Output Driver cannot drive the coil of Head Load Magnet directly. It is necessary to have an external driving transistor.
−WSW	23	Write Switch Output	Output terminal for Write Gate signal to control Write circuit.

(to be continued)

Symbol	Pin No.	Name	Description
−ESW	22	Erase Switch Output	Output terminal for Erase Gate signal to control Erase Driver.
−HIS	21	Head 1 Select Output	Output terminal for Head Select signal connected to Read/Write circuit. When output on this terminal is "Low", SIDE 1 of the head is selected.
−DMO	11	Spindle Motor On	Output terminal for Spindle Motor ON/OFF Control signal. Output "Low" makes the motor ON and "High" makes OFF. This terminal cannot drive the spindle motor directly. When −MON input turns "High" from "Low", −DMO turns "High" after 10.5sec.
−INL	7	In Use LED Output	Output terminal for In Use signal. Output circuit has an open collector NPN transistor, and can drive LED directly.
−OS1	36	Oscillator Input 1	Connection terminal for an external ceramic oscillator component.
−OS2	37	Oscillator Input 2	
V_{CC1}	34	Bipolar V_{CC}	Power supply for Bipolar circuits.
V_{CC2}	9	C-MOS V_{CC}	Power supply for C-MOS circuits.
GND 1	33	Bipolar Gnd	Ground for Bipolar circuits.
GND P	12	Power Gnd	Ground for high current output drivers.
GND 2	10	C-MOS Gnd	Ground for C-MOS circuits.

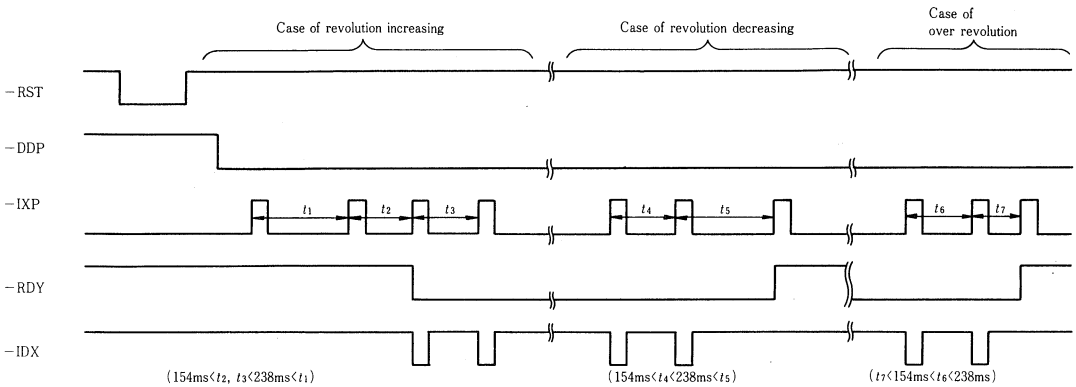
■TIMING SPECIFICATIONS

Timing Name		Internal Clock Period (N. 1)	Timing Spec
Normal Index Period Bound	3.5", 5"	1ms	163ms↔227ms
	8"		131ms↔195ms
External Step Pulse—sub Step Pulse Period		128μs	3.07ms
Step Energizing Timer		2ms	32.8ms
Pre Erase Timer	3.5"	4μs	300μs
	5.25"		428μs
	8"		228μs
Post Erase Timer	3.5"	4μs	864μs
	5.25"		948μs
	8"		568μs
Motor Off Timer		2ms	1.05s

Notes) 1. Above condition is $fosc = 4MHz$.
2. Timing accuracy.
Above timing spec have an error that maximum value is equal the internal clock period.

TIMING CHART

1. INDEX Period Detection



($154ms < t_2, t_3 < 238ms < t_1$)
When Index period becomes the value between 154ms ~ 238ms, −RDY output turns "L" after counting 2 Index pulses with the "L" −DDP input.

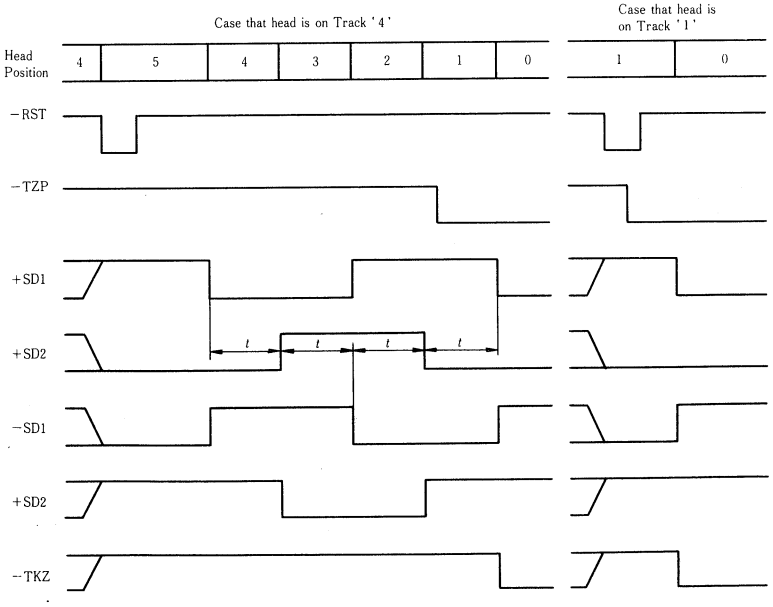
($154ms < t_4 < 238ms < t_5$)
−RDY turns "H" immediately if Index period becomes more than 238ms.

($t_7 < 154ms < t_6 < 238ms$)
−RDY turns "H" immediately if Index period becomes less than 154ms.

Detects the revolution of spindle if the revolution is within an allowable tolerance or not enable Read/Write operation, and generates READY signal. This function is inhibited when disk is discharged (equivalent to −DDP "H").

NOTE. Condition of above timing values is Osc. frequency $fosc = 4MHz \pm 5\%$.

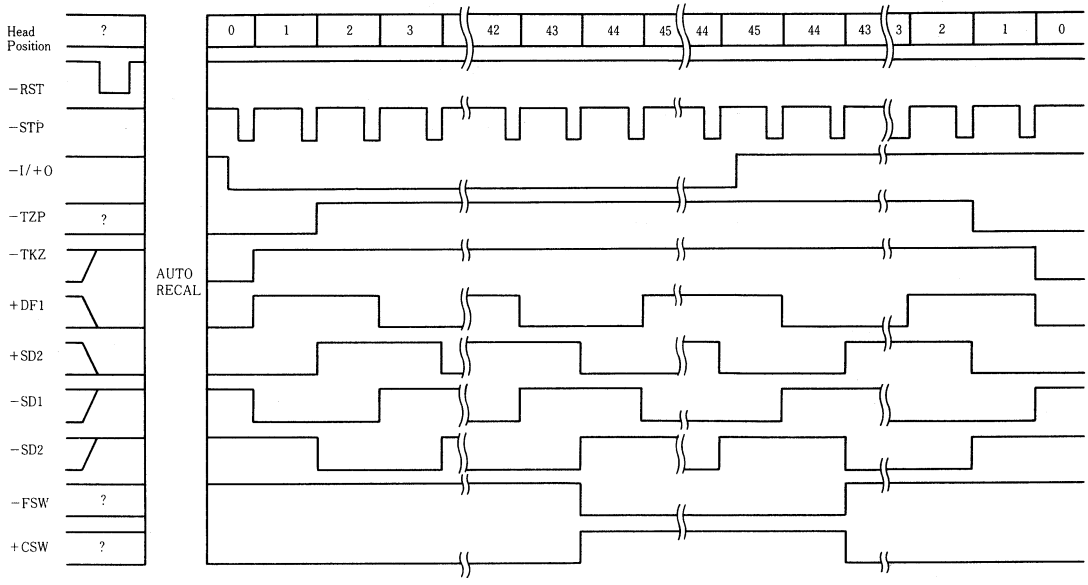
2. Auto Recalibration



($2.43ms \leqq t \leqq 3.23ms$)

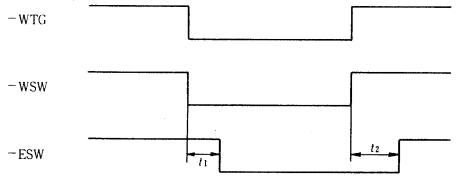
Initialize an internal track counter and a stepper counter by automatically returning the head to Track 00 position at the rising of power supply.

3. Track Counter, Stepper Counter



Track Counter stores the present track position of the head, −FSW(Filter switch) or +CSW(Write Current Switch) output is generated according to the stored position data. Stepper Counter generates +SD1, +SD2, −SD1 and −SD2 output to drive a 4-phase stepper motor coil.

4. Write Circuit and Erase Circuit

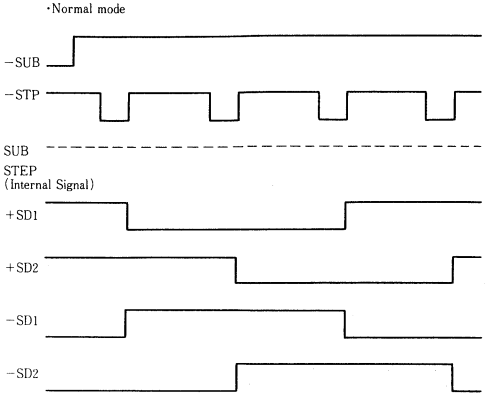


$\begin{pmatrix} 281\mu s < t_1 < 315\mu s \\ 817\mu s < t_2 < 908\mu s \end{pmatrix}$ for 3.5"

For the tunnel erase head, Erase gap has a lag position against Read/Write gap. So Erase gate timing is necessary to have some determined delay time against Write gate timing.

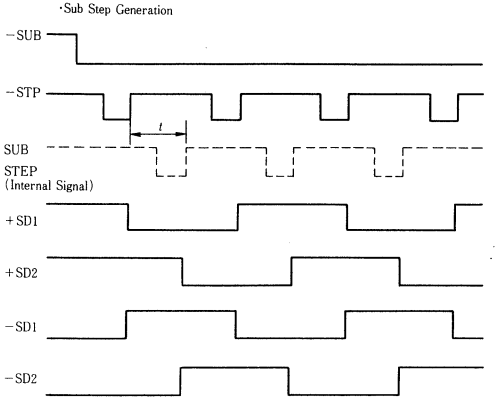
5. Step Motor Drive Output Signal Timing

● Normal mode



In normal mode, step output signals turn at the rising edge of −STP signal.

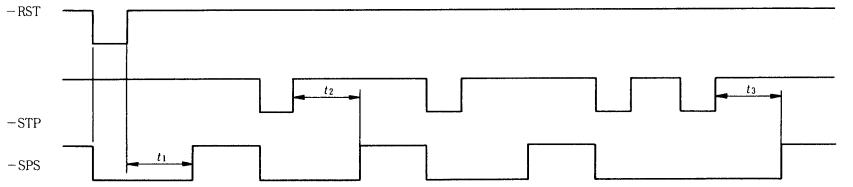
● Sub Step Generation



(2.79ms<t<3.23ms)

Sub Step Generator generates one more step pulse internally after 3.1ms from the leading −STP input.
A pair of leading and sub step pulse makes equivalence to double step pulses input.

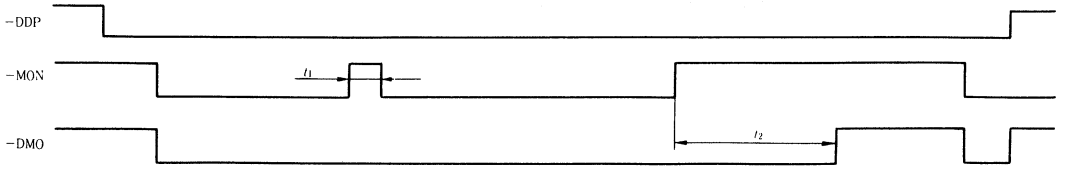
6. Stepper Energizing Timer



(29.2ms<t_1, t_2, t_3, <34.5ms)

This timer generates a switch signal to change a supply voltage for stepping motor coil between seeking and holding. This function is effective also when power supply rises.

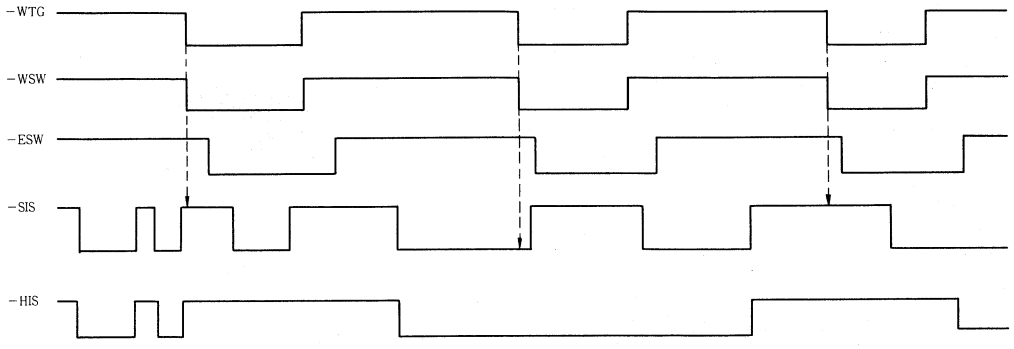
7. Motor Off Timer



(t_1<9.7s, 9.7s≦t_2≦11.0s)

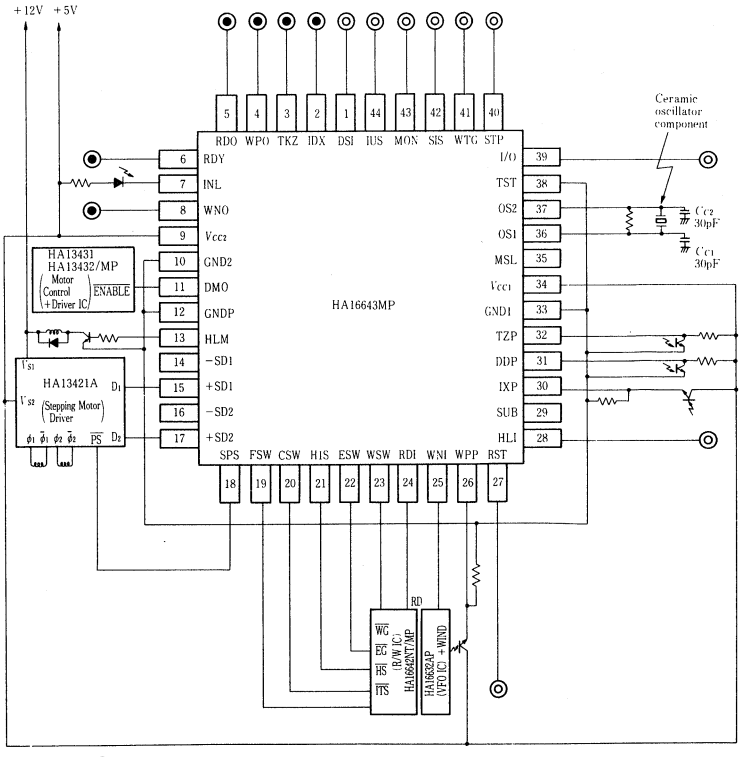
When motor control signal −MON turns "L", −DMO output turns "L" and makes the spindle motor rotate. When −MON input turns "H", −DMO output turns "H"after t_2 seconds and the motor stops. Therefore, if −MON once turns "H" and turns "L" again within 9.7seconds, −DMO output will hold "L" level and the motor will keep rotating.

8. Head Select Function



When both −WSW and −ESW output signal are 'High', same signal as −SIS input signal appears at −HIS output terminal. When either −WSW or −ESW is 'Low', −SIS input signal is latched at the 'H'→'L' edge of −WTG signal and the latched signal appears at −HIS output. After −ESW output turns 'H', same signal as −SIS input appears at −HIS output again.

■EXAMPLE OF APPLICATION CIRCUIT



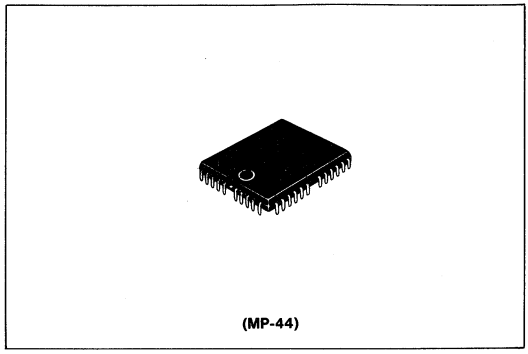
◎ : Terminal for Signal from FDC

● : Terminal for Signal to FDC

HA16651MP ●Read/Write Circuit for FDD

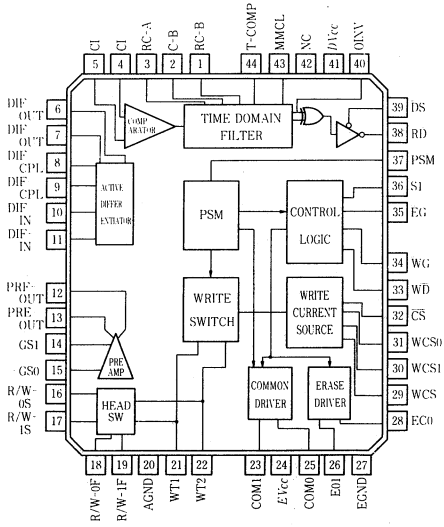
■FEATURES

- Read Amplifier has a differential voltage gain of 200 typ. Which is adjustable with inserting the resistance between gain select terminals.
- Read circuit can be applied for the signal amplitude of 0.25mVp-p to 10mVp-p. Which is read out from Head Coil, so that this IC has superior capability to apply to the FDD less than 5 inches.
- In the read circuit, the peak shift is less than 1% for the signal amplitude, 0.5mVp-p to 10mVp-p at the Amp input, resulting in no adjustment.
- Pre-Amp and Write driver circuit include a Read/Write mode switch circuit not to need the external diode switch circuit.
- Pulse width of monomulti-vibrator for the noise pulse filter can be switched the control terminal. Therefore this IC is applicable to the FDD which can deal with both 5.25 inches and 8 inches format.
- Output circuit for Read pulse is composed of the 3-state output circuit and controled by drive select signal. Also polarity of output pulse can be switched by the control terminal.
- 2 channel erase drivers built in, and are available to switching the erase current, for example at the inner track etc.
- Write current can be established at any value according to the external resistor. The write current is independent of the supply voltage drift and temperature drift, with the built-in stabilizing circuit.
- This IC provides a function to increase the write current at the inner track on the disk with a external switching signal. The increase ratio of the write current can be established at any value with the external resistor.
- A dual mode supply voltage monitor circuit is built in, to inhibit miss writing and miss erasing at the supply timing, ON and OFF, and the abnormal supply voltage.



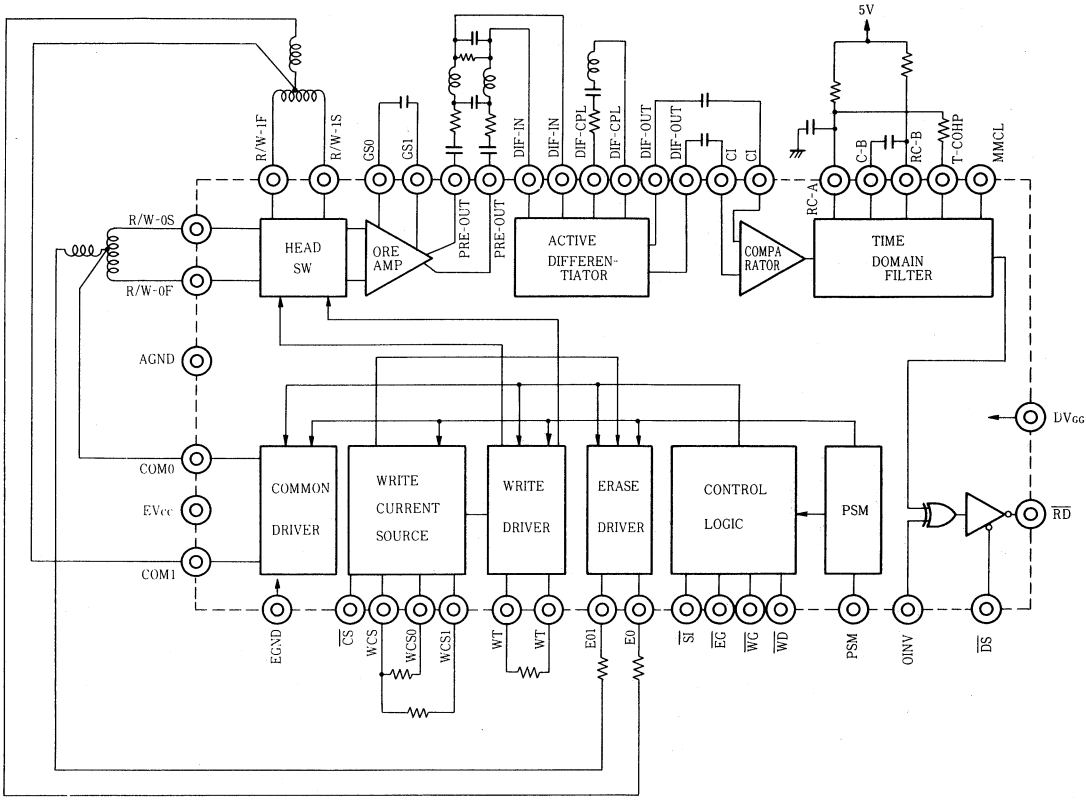
(MP-44)

■PIN ARRANGEMENT



(Top View)

■BLOCK DIAGRAM



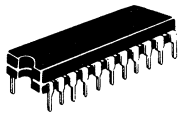
■ELECTRICAL CHARACTERISTICS (T_a=25°C unless otherwise specified.)

Circuit Block		Item	Symbol	Test Conditions	min	typ	max	Unit
		Supply Voltage Range	DV_{GG}		4.5	5.0	5.5	V
		Supply Voltage Range	EV_{CC}		10.2	12.0	13.8	V
Read Circuit	Pre-Amp.	Differential Voltage Gain	A_{VD}	V=250kHz, V_{IN}=5mVp-p	–	200	–	V/V
		Input Bias Current	I_{IB}		–	–	15	μA
		Input Resistance	r_i	f=250kHz	20	50	–	kΩ
		Common Mode Input Voltage Range	V_{CM}		3.0	3.7	4.4	V
		Common Mode Output Voltage	V_{CO}		–	3.1	–	V
		Output Harmonic Distortion	THD	f=1kHz, V_{IN}=10mVp-p	–	–	5	%
	Peak Detector	Peak Shift	PS	f=250kHz, V_{IN}=0.25 to 10mVp-p	–	–	1	%
	Differentiator	Input Resistance	r_{id}		–	15	–	kΩ
	Wave Processor	Output Sink Current	I_{SO-D}		400	600	–	μA
		"H" Level Output Voltage	V_{OH1}	DV_{GG}=4.5V, I_{OH}=−3mA	2.4	–	–	V
		"L" Level Output Voltage	V_{OL1}	DV_{GG}=4.5V, I_{OL}=12mA	–	–	0.4	V
		Timing Range #1	t_{I-1}		0.5	–	10	μs
		Timing Range #2	t_{I-2}		150	–	2000	μs
		"L" Level Input Current (DS, OINV)	I_{IL1}	DV_{GG}=5.5V	−100	–	–	μA
		"H" Level Input Current (DS, OINV)	I_{IH1}	DV_{GG}=5.5V	–	–	50	μA
Write Circuit	Common Driver	Output Voltage at Selected WRITE MODE	V_{COM-W}	EV_{CC}=12V, I_{OH}=90mA	10.4	–	11.3	V
		Output Voltage at Unselected WRITE MODE	$V_{COM-OFF}$	EV_{CC}=12V	–	–	0.7	V
		Output Voltage at Selected READ MODE	V_{COM-R}	EV_{CC}=12V	3.3	3.7	4.1	V
		Output Voltage at Unselected READ MODE	$V_{COM-OFF}$	EV_{CC}=12V	–	–	0.8	V
		Output Current Range	I_{COM}		–	–	100	mA
	Erase Driver	"L" Level Output Voltage	V_{OL2}	V_{GG}=4.5V, I_{OL}=80mA	–	–	0,4	V
		Output Leakage Current	I_{LEAK}	EV_{CC}=13.8V	–	–	100	μA
		Erase Current Range	I_{ER}		–	–	80	mA
	Write Driver	Write Current Accuracy	I_{WT-A}	EV_{CC}=12V DV_{GG}=5V	−7	–	+7	%
		Write Current Pair Characteristics	I_{WT}	EV_{CC}=12V EV_{GG}=5V	−1	–	+1	%
		Write Current Identification Range	I_{WT-I}		1	–	15	mA
	Logic Input Gate	"H" Level Input Voltage	V_{IH}		2.0	–	–	V
		"L" Level Input Voltage	V_{IL}		–	–	0.8	V
		"H" Level Input Current	I_{IH2}		–	–	50	μA
		"L" Level Input Current	I_{IL2}		−100	–	–	μA
	Supply Voltage Monitor	Detection Voltage for 5V Supply	V_{PSM5}	EV_{CC}=12V	3.6	4.0	4.4	V
		Detection Voltage for 12V Supply	V_{PSM12}	DV_{GG}=5V	–	–	8.0	V
	Quiescent Voltage Read Mode	Quiescent Supply Current (5V)	I_{GG}	EV_{CC}=12V, DV_{GG}=5V	–	40	–	mA
		Quiescent Supply Current (12V)	I_{CC}	EV_{CC}=12V, DV_{GG}=5V	–	15	–	mA

HA16652 Series ●Read/Write IC for Hard Disk Drive

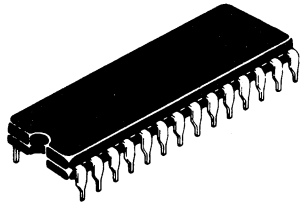
The HA16652P/MP is an one chip IC integrated with Read amplifiers and Write drivers to apply the small hard disk drive memory systems.

HA16652P (4 channels)



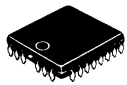
(DP-22)

HA16652P (6 channels)



(DP-28)

HA16652MP (6 channels) and (4 channels)



(MP-28)

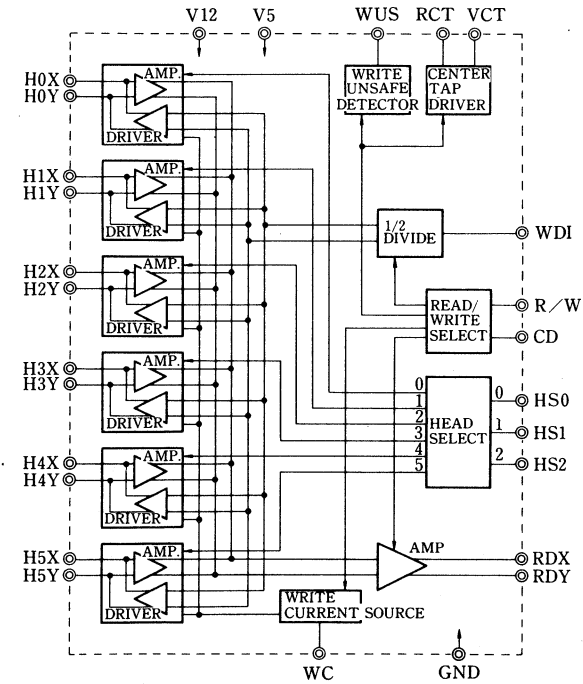
■ FUNCTIONS

- Read amplifier circuit
- Write driver circuit
- Write unsafe detection circuit
- Write current source circuit

■ FEATURES

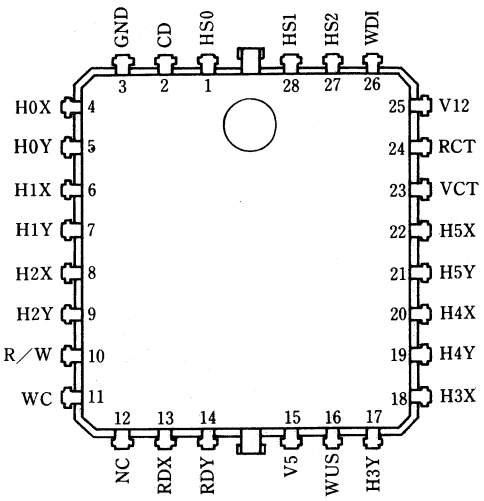
- Single polarity power supplies +5V, +12V.
- R/W channels: 4 or 6.
- Easily applicable for over 6-channel systems.
- Read channel has a low noise amplifier with a high differential voltage gain of 200 typ.
- Emitter followered read amplifier outputs.
- Adjustable write current with an external resistor.
- Supply voltage monitor circuit enables to inhibit miss writing at the lower supply voltage.
- TTL interface

■ BLOCK DIAGRAM

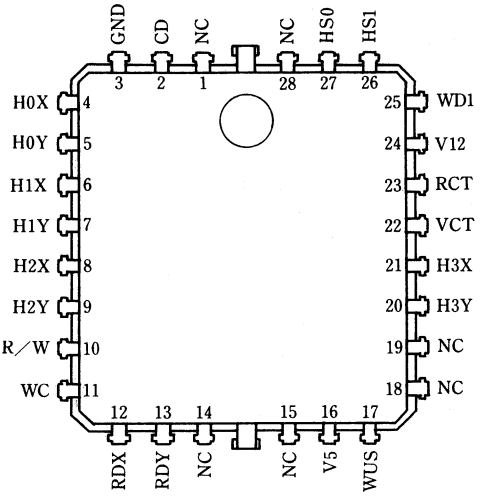


■ PIN ARRANGEMENT (Top View)

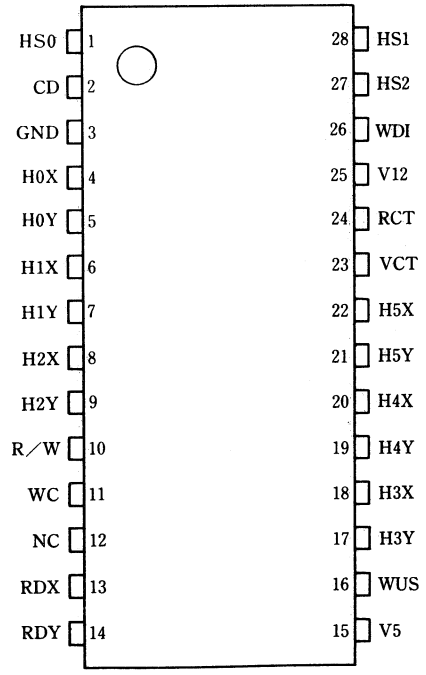
• **HA16652MP (6-channel)**



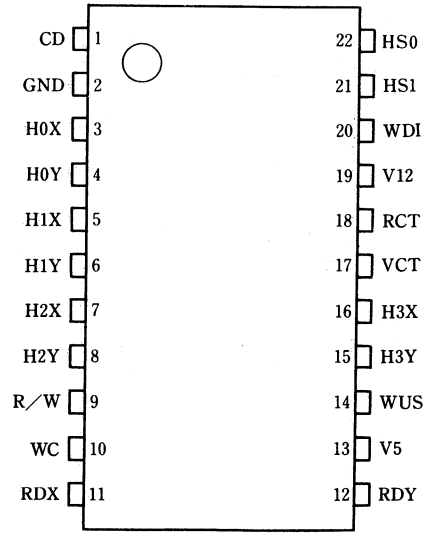
• **HA16652MP (4-channel)**



• **HA16652P (6-channel)**



• **HA16652P (4-channel)**



As power Dissipation of MSP. packages varies with the mounting structure, the substrate material and the wiring density on the substrate side, derate according to the following thermal resistance data.

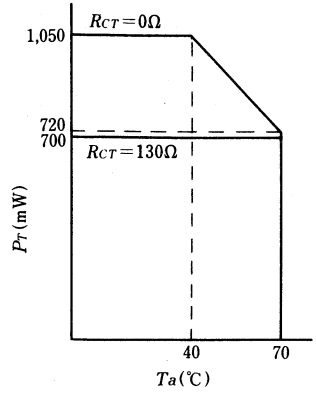


Fig. 1 Derating curve

The left figure shows the derating under the condition of the mounting

② ($\Theta j-a \fallingdotseq 90°C/W$).

In case of the mounting ① and ③, derate according to the following thermal resistance data.

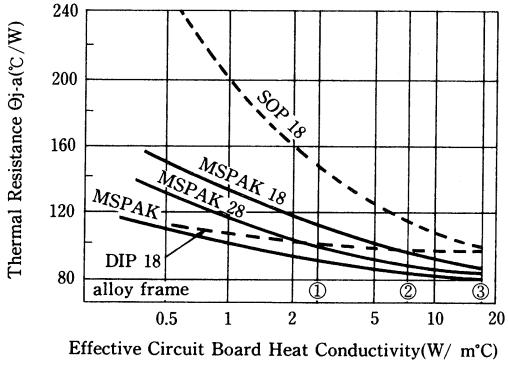
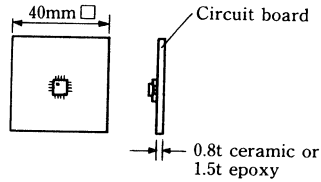


Fig. 2 MSPAK Thermal Resistance



① glass epoxy with 10% metallization density
② glass epoxy with 30% metallization density
③ 96% almina ceramic circuit board

■ ABSOLUTE MAXIMUM RATINGS (Ta = 25°C)

Item	Symbol	Rating	Unit	Application Terminal
Supply Voltage	V_5	−0.3 to 6.0	V	V_5
	V_{12}	−0.3 to 14.0	V	V_{12}
Write Current	Iw	60	mA	
Interface Input Voltage	Vin	−0.3 to V5 +0.3	V	HS0, HS1, HS2, WDI, R/W, CD
WUS Voltage	$Vwus$	−0.3 to 14.0	V	WUS
WUS Output Current	$Iwus$	12	mA	WUS
Center Tap Voltage	$Vcto$	−0.3 to 14.0	V	VCT
Center Tap Output Current	Ico	−60	mA	VCT
Read Data Output Current	Iro	−10	mA	RDX, RDY
Head Voltage	Vh	−0.3 to V12 +0.3	V	Note 1)
Operating Temperature	$Topr$	0 to 70	°C	
Storage Temperature	$Tstg$	−55 to 125	°C	

Note 1) H0X, H0Y, H1X, H1Y, H2X, H2Y, H3X, H3Y, H4X, H4Y, H5X, H5Y

■ ELECTRICAL CHARACTERISTICS (V_{12} = 12V ±10%, V_5 = 5V ±10%, unless otherwise specified.)

• Power Supply

Item	Symbol	Test Condition		min.	typ.	max.	Unit
Supply Voltage Range	V_5			4.5	5.0	5.5	V
	V_{12}			10.8	12.0	13.2	V
+5V Supply Current	I_5	Read Mode		–	–	25	mA
		Write Mode		–	–	30	mA
		Idle Mode		–	–	25	mA
+12V Supply Current	I_{12}	Read Mode		–	–	50	mA
		Write Mode		–	–	30 + Iw	mA
		Idle Mode		–	–	25	mA
Power Dissipation	Pd	Read Mode	Ta = 25°C	–	–	600	mW
		Write Mode Iw = 50 mA R_{CT} = 130Ω	Ta = 25°C	–	–	700	mW
		Write Mode Iw = 50 mA R_{CT} = 0Ω	Ta = 25°C	–	–	1050	mW
		Idle Mode	Ta = 25°C	–	–	400	mW

• Digital Input

Item	Symbol	Test Condition	min.	typ.	max.	Unit
Low Level Input Voltage	V_{IL}		−0.3	–	0.8	V
Low Level Input Current	I_{IL}	V_{IL} = 0.8V	−0.4	–	–	mA
High Level Input Voltage	V_{IH}		2.0	–	V5 +0.3	V
High Level Input Current	I_{IH}	V_{IH} = 2.0V	–	–	100	μA
Read/Write Transition Time	Trw	Delay to 90% of Write Current Note 3)	–	–	1.0	μs
Write/Read Transition Time	Twr	Note 2), Note 3)	–	–	1.0	μs
Head Select Switching Delay Time	Ths	Read or Write Mode Note 3)	–	–	1.0	μs
Chip disable Transition Time	$Tirw$	R/W to Idle or Idle to R/W Note 3)	–	–	1.0	μs

Note 2) Delay to 90% of 10 MHz read signal envelope, Write current delay to 90%.

• Write Faults Detection

Item	Symbol	Test Condition	min.	typ.	max.	Unit
Low Level US Voltage	V_{OL}	I_{OL} = 8 mA	–	–	0.5	V
High Level US Current	I_{OH}	V_{OH} = 5.0V	–	–	100	μA
Unsafe to Safe Delay Time	Td_2	Iw = 20 mA Note 3)	–	–	1.0	μs
Safe to Unsafe Delay Time	Td_1	Iw = 50 mA Note 3)	1.6	–	8.0	μs

• Head Select Table

HS2	HS1	HS0	Head Select
L	L	L	0
L	L	H	1
L	H	L	2
L	H	H	3
H	L	L	4
H	L	H	5
H	H	L	none
H	H	H	none

• Mode Select Table

CD	R/W	Mode
L	L	Write
L	H	Read
H	L	Idle
H	H	Idle

- **Read Amplifier**

Item	Symbol	Test Condition	min.	typ.	max.	Unit
Differential Voltage Gain	*Avd*	*Vin* = 1 mVpp, R_L = 1 kΩ *f* = 300 kHz	160	200	240	V/V
Band Width (−3 dB)	*Bw*	*Zs* < 5Ω, *Vin* = 1 mVpp	20	–	–	MHz
Input Noise Voltage	*Vn*	*f* = 15 MHz, Lh = 0, Rh = 0	–	–	2.1	nV/$\sqrt{\text{Hz}}$
Input Bias Current	*Ib*		–	–	45	μA
Dynamic Range	*Vomax*	Gain, falls to 90% of 0.0V_{DC}, *f* = 300 kHz, *Vin* = *Vi* + 0.5 mVpp	−2.0	–	2.0	mV
Common Mode Rejection Ratio	*CMRR*	*Vin* (cm) = V_{CT} + 100 mVpp 0.0V_{DC}, *f* = 5 MHz	50	–	–	dB
Power Supply Rejection Ratio	*PSRR*	V_5, V_{12} ±100 mVpp f = 5 MHz	45	–	–	dB
Channel Separation	*Sep*	*Vin* = 100 mVpp on unselected channels *Vin* = 0 mVpp on selected channels *f* = 5 MHz	45	–	–	dB
Output Offset Voltage	*Vo*		−960	–	960	mV
Differential Input Resistance	*Rin*	*f* = 5 MHz	2	–	–	kΩ
Differential Input Capacitance	*Cin*	*f* = 5 MHz	–	–	23	pF
Common Mode Output Voltage	*Vocm*		5.0	–	7.0	V
Single Ended Output Resistance	*Ro*	*f* = 5 MHz	–	–	30	Ω

- **Write Driver**

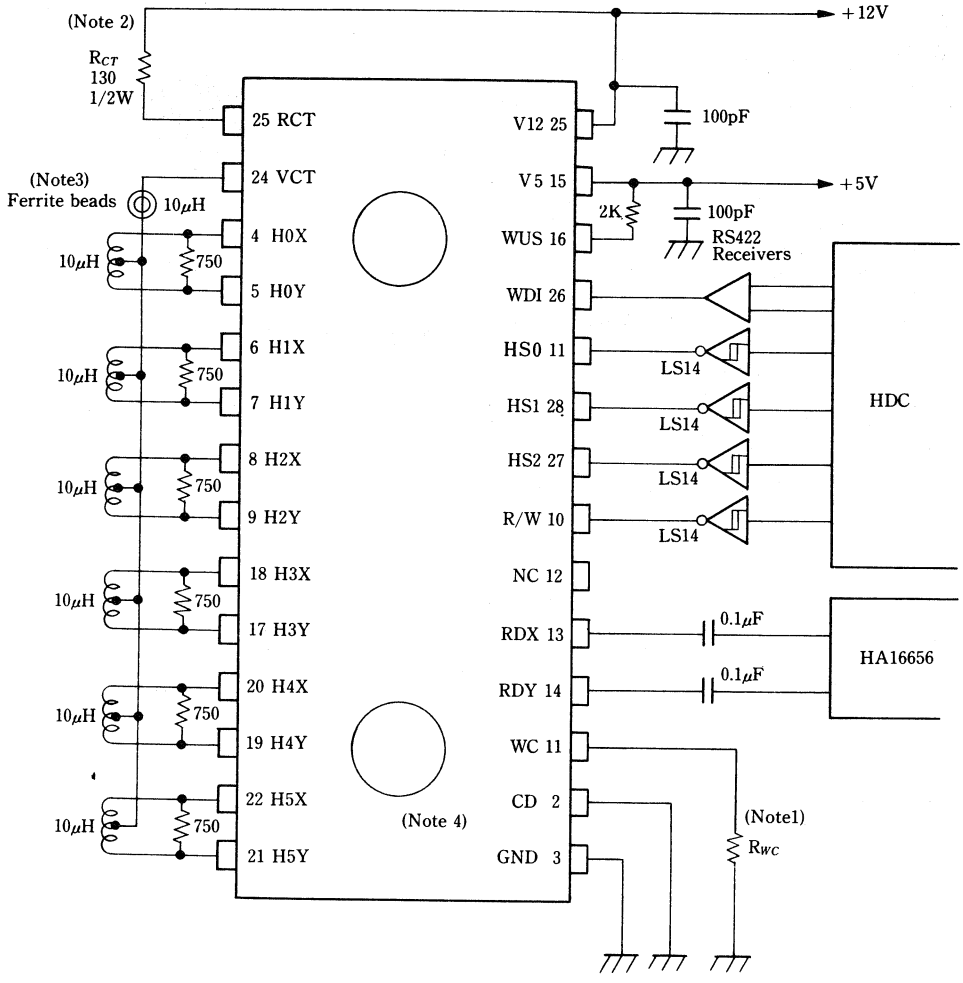
Item	Symbol	Test Condition	min.	typ.	max.	Unit
Write Current Setting Range	*Iw*	*Iw* · L_{head} > 200 mA · μH	10	–	50	mA
Head Current Rise Time	*Thcx*	*Lh* = 0 μH, Rh = 0Ω, Note 3) 10% to 90% Point	–	–	20	ns
Head Current Switching Delay Time	Td_3	Rh = 0Ω, Lh = 0μH From 50% Point WDI Input Duty = 50% rise/fall time = 1 ns Note 3)	–	–	25	ns
Head Current Switching Symmetry	Td_4		–	–	2	ns
Differential Head Voltage Swing	Δ*Vh*		5.7	–	–	Vpk
Unselected Head Transient Leakage Current	*Ih*		–	–	2	mApk
Differential Output Capacitance	*Cout*	f = 5 MHz	–	–	15	pF
Differential Output Resistance	*Rout*	f = 5 MHz	10	–	–	kΩ
WDI Minimum Input Frequency	*Fw*	WUS Output = Low	125	–	–	kHz
Head Current Gain	Ih/I_{WC}	Head Current/Iwc	–	20	–	
VCT Output Voltage	V_{CT}	Read Mode	–	4.0	–	V
	V_{CT}	Write Mode	–	6.0	–	V
Write Current Setting Coefficient	K		129	140	151	

Note 3) Conditions in Write Driver and time measuring conditions V_{12} = 12V ±10%, V_5 = 5V ±10%, Ta = 25°C, Iw = 45 mA, Lh = 10μH, Rd = 750Ω, f (data) = 5 MHz

PIN DESCRIPTION

SYMBOL	NAME	DESCRIPTION
RDX RDY	Read Amplifier Output	Differential output pins for the Pre-Amp. in the Read Circuit. The signal read out from the Head Coil is amplified and provided on these pins.
R/W	R/W Switch	Mode Select Switch for changing over the bias condition of the Head Coil. A Low level selects the Write mode, while a High level selects the Read Mode.
CD	Chip Disable	Chip Select Pin. This pin enables more chips to be used for multi channel systems. When selecting a chip, set this pin "Low".
V_{CT}	Center Tap Voltage Output	Center Tap Voltage Output Pin for the head coil. Current corresponding to the write current flows out from this pin in the Write mode.
R_{CT}	Power Supply for Center Tap	The chip power dissipation is reduced by pulling up this pin to the +12V supply with 1/2W and a 130Ω resistor. When the power dissipation has no problem, R_{CT} pin can be pulled up to V_{12} voltage directly.
HS0 HS1 HS2	Head Select 0 Head Select 1 Head Select 2	Input pins for head select signals. The combination of these signals selects each one Head.
H0X, H0Y	Head 0X, 0Y	These pins are connected to the R/W head coil of channel 0.
H1X, H1Y	Head 1X, 1Y	These pins are connected to the R/W head coil of channel 1.
H2X, H2Y	Head 2X, 2Y	These pins are connected to the R/W head coil of channel 2.
H3X, H3Y	Head 3X, 3Y	These pins are connected to the R/W head coil of channel 3.
H4X, H4Y	Head 4X, 4Y	These pins are connected to the R/W head coil of channel 4.
H5X, H5Y	Head 5X, 5Y	These pins are connected to the R/W head coil of channel 5.
WC	Write Current Setting	Write Current Setting Pin. The Write current is defined as the equation (1) by connecting the external resistance R_{WC} between this pin and GND. WRITE CURRENT = k /R_{WC} [A] ..... (1)
WDI	Write Data Input	Write data input pin. The signal is divided through the F/F circuit in the IC, and drives the Write driver.
WUS	Write Unsafe Detection Output	A high level output indicates the unsafe writing conditions. Unsafe conditions are shown as follows, at head pins 1 Short-circuit to Ground 2 Open Others 3 Center tap open 4 Extremely low WDI input frequency 5 No write current flow 6 All the combinations of the above conditions 7 In the Read Mode 8 Chip unselected
V_5	5V Power Supply	5V Power Supply
V_{12}	12V Power Supply	12V Power Supply
GND		System ground

■ EXAMPLE OF APPLICATION CIRCUIT



(Note 1) : External resistance value, R_{WC} is changed by Write Current used. Determine the value by (Expression 1).

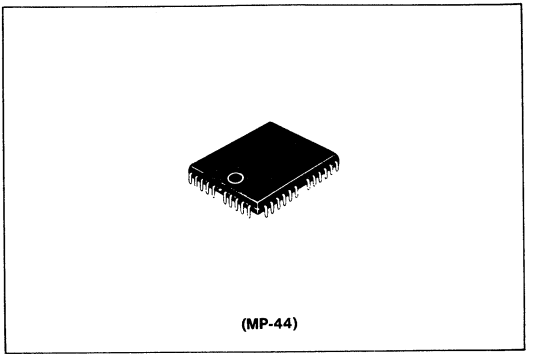
(Note 2) : External resistance, R_{CT} (130Ω, 1/2W) restricts the power dissipation in a chip.

(Note 3) : Ferrite beads control overshoot of Write Current, ringing and so on.

(Note 4) : It is pulled down to GND in case of using in 6 channels.

HA16656MP ●Read Data Peak Detector for HDD

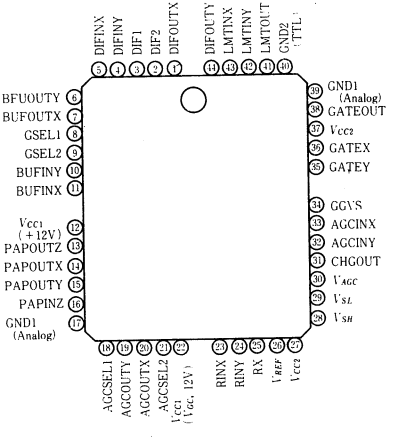
HA16656MP is the read data peak detector IC for a hard disk drive to generate a digital pulse from the signal read out by the head coil.
The output signal of an external preamplifier is amplified by the AGC Amplifier and is input the Differential Amplifier through the Low Pass Filter.
By the Differential Amplifier output and the Gate signal from Gate Generator, the read pulse is generated.



■FEATURES

- Built-in AGC Amplifier makes it possible to stabilize read pulse generation independent of the characteristic deviation caused by the kind of media (the plating media, the coating media), by the kind of head (the ferrite, the thin film).
- Wide differential input voltage range of AGC Amplifier: 20mVp-p to 0.5Vp-p.
- Voltage gain is controlled 0dB to 40dB.
- Gate Generator enables it to set slice level to eliminate incorrect read pulse which the time domain filter can not. So the resolution of signal is raised without incorrect pulse.
- AGC Amplifier has the function of making 0 of the gain in write mode.
- Small, surface-mount package enables high density mounting.
- Assembly board can be small by combining with the read/write IC HA16652P/MP and the read pulse generator IC HA16663MP.

■PIN ARRANGEMENT

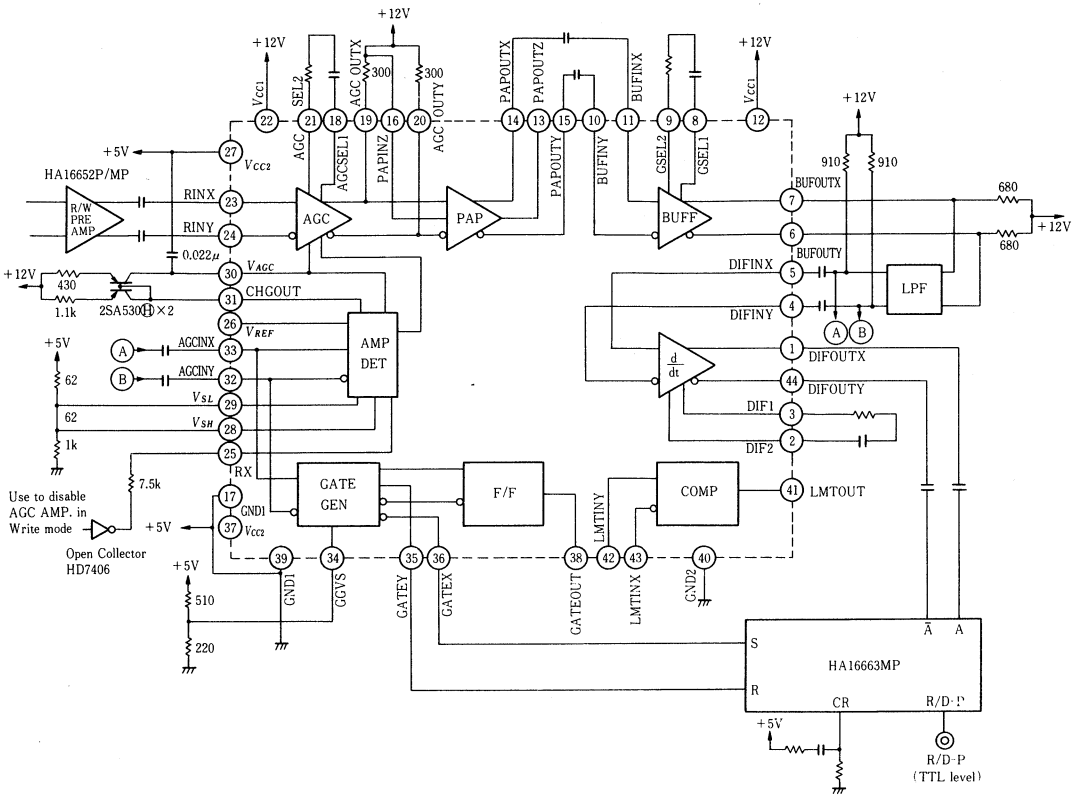


(Top View)

■ABSOLUTE MAXIMUM RATINGS (T_a=25°C)

Item	Symbol	Rating	Unit	Notes
Supply Voltage	V_{CC1}	15	V	
Supply Voltage	V_{CC2}	7	V	
Input Voltage	V_{IRX}	V_{CC1}	V	Applies to RX.
Input Voltage	V_{ISL}	V_{CC2}	V	Applies to V_{SL} and V_{SH}
Input Voltage	V_{IGV}	V_{CC2}	V	Applies to GGVS.
Output Current	I_{OPAP}	−10	mA	Applies to PAPOUTX and PAPOUTY.
Output Current	I_{ODIF}	−10	mA	Applies to DIFOUTX and DIFOUTY.
Output Voltage	V_{OCH}	V_{CC2}+2	V	Applies to CHGOUT.
Output Voltage	V_{ODCH}	V_{CC1}	V	Applies to V_{AGC}
Output Current	I_{OL}	4	mA	Applies to LMTOUT and GATEOUT.
Output Current	I_{OH}	−200	μA	Applies to LMTOUT and GATEOUT.
Output Current	I_{OG}	−13	mA	Applies to GATEX and GATEY.
Differential Input Voltage	V_{IDIFA}	0.5	Vpp	Applies to RINX and RINY.
Differential Input Voltage	V_{IDIFB}	3	Vpp	Applies to BUFINX and BUFINY.
Differential Input Voltage	V_{IDIFD}	3	Vpp	Applies to DIFINX and DIFINY.
Differential Input Voltage	V_{IDIFG}	3	Vpp	Applies to AGCINX and AGCINY.
Differential Input Voltage	V_{IDIFL}	3	Vpp	Applies to LMTINX and LMTINY.
Operating Temperature	T_{OP}	0 to +70	°C	
Storage Temperature	T_{STG}	−55 to +125	°C	
Power Dissipation	P_T	765	mW	

■BLOCK DIAGRAM



■PIN DESCRIPTION

Pin	Symbol	Description
Power supply pins	V_{CC1}	+12V supply voltage
	V_{CC2}	+5V supply voltage
	GND_1	GND for all blocks except TTL output circuit
	GND_2	GND for the TTL output circuit
Input signal pins	RINX RINY	Differential input pins for read signal from Hard Disk
	BUFINX BUFINY	Differential input pins of Buffer Amp.
	AGCINX AGCINY	Differential input pins of AGC Amplitude Detector circuit
	LMTINX LMTINY	Differential input pins of Zero Cross Comparator
	V_{SL}	Input pin for setting Low slice level voltage of AGC amplitude detector, corresponding to threshold of discharge current
	V_{SH}	Input pin for setting High slice level voltage of AGC amplitude detector, corresponding to threshold of charge current
	RX	Input pin to control ON/OFF of AGC loop RX=open; AGC loop ON RX=Low; AGC loop OFF (Minimum gain of AGC Amp.)
	GGVS	Input pin for setting slice level of gate generator
	DIFINX DIFINY	Differential input pins of Differential Amp.

(to be continued)

Pin	Symbol	Description
Output signal pins	AGCOUTX AGCOUTY	Open-collector differential output pins of AGC Amp.
	PAPOUTX PAPOUTY PAPOUTZ	Emitter followered differential output pins of output buffer of AGC Amp.
	BUFOUTX BUFOUTY	Open-collector differential output pins of Buffer Amp.
	DIFOUTX DIFOUTY	Emitter-follower differential output pins of Differential Amp.
	LMTOUT	TTL level output pin of zero cross comparator
	V_{AGC}	Discharge current output pin of AGC amplitude detector
	CAGOUT	Charge current output pin of AGC amplitude detector
	V_{REF}	Monitoring pin for reference voltage of AGC Amp.
	GATEX GATEY	ECL level output pins of gate generator
	GATEOUT	TTL level output pin of gate generator
Resistor & capacitor pins	$AGCSEL_1$ $AGCSEL_2$	Resistor and capacitor connection pins for setting voltage gain and cut-off frequency of AGC Amp.
	$GSEL_1$ $GSEL_2$	Resistor and capacitor connection pins for setting Buffer Amp voltage gain and cut-off frequency
	DIF_1 DIF_2	Resistor and capacitor connection pins for setting differential sensitivity and voltage gain of Differential Amp.

■ELECTRICAL CHARACTERISTICS (T_a=25°C, V_{CC1}=12V, V_{CC2}=5V, unless otherwise specified.)

	Item	Symbol	Test Conditions	min	typ	max	Unit	Applied Pin	Note
Total	Supply Voltage	V_{CC1}		10.8	12	13.2	V	V_{CC1}	
		V_{CC2}		4.5	5	5.5	V	V_{CC2}	
	Supply Current	I_{CC1}	V_{CC1}=13.2V, V_{CC2}=5.5V	—	24	32	mA	V_{CC1}	
		I_{CC2}	V_{CC1}=13.2V, V_{CC2}=5.5V	—	65.5	87.5	mA	V_{CC2}	
AGC Amplifier	Differential Input Resistance	R_{IA}		—	3	—	kΩ	RINX RINY	
	Input Bias Voltage	V_{BA}		3.1	3.5	3.9	V		
	Differential Input Voltage	V_{IDIFA}		—	—	300	mVpp		
	Common Mode Output Voltage	V_{OCA}	R_L=300Ω	10.6	11.1	11.5	V	AGCOUTX AGCOUTY	
	Differential Output Offset Voltage	V_{OFA}	R_L=300Ω	−130	—	130	mV		
	Output Sink Current	I_{OSA}		1.6	3	4.6	mA		
	Output Dynamic Range	V_{ODA}		—	—	2.5	Vpp		
Buffer Amplifier	Differential Input Resistance	R_{IB}		—	10	—	kΩ	BUFINX BUFINY	
	Input Bias Voltage	V_{BB}		4.35	4.85	5.1	V		
	Common Mode Output Voltage	V_{OCB}	R_L=430Ω	9.8	10.5	11.2	V	BUFOUTX BUFOUTY	
	Differential Output Offset Voltage	V_{OFB}	R_L=430Ω	−230	—	230	mV		
	Output Sink Current	I_{OSB}		1.8	3.5	5.5	mA		
	Differential Voltage Gain	A_{VDB}	R_L=300Ω, f_{in}=1MHz, V_{in}=200mVp-p	—	7.9	—	dB		1
Differential Amplifier	Differential Input Resistance	R_{ID}		—	10	—	kΩ	DIFINX DIFINY	
	Input Bias Voltage	V_{BD}		3.4	3.6	3.8	V		
	Common Mode Output Voltage	V_{OCD}		2.8	3.3	3.6	V	DIFOUTX DIFOUTY	
	Differential Output Offset Voltage	V_{OFD}		−230	—	230	mV		
	Differential Voltage Gain	A_{VDD}	V_{in}=200mVpp, f_{in}=1MHz	—	11.8	—	dB		2
	Differential Output Clamp Voltage	V_{ODD}	V_{in}=2Vpp, f_{in}=1MHz	—	1.5	—	Vpp		

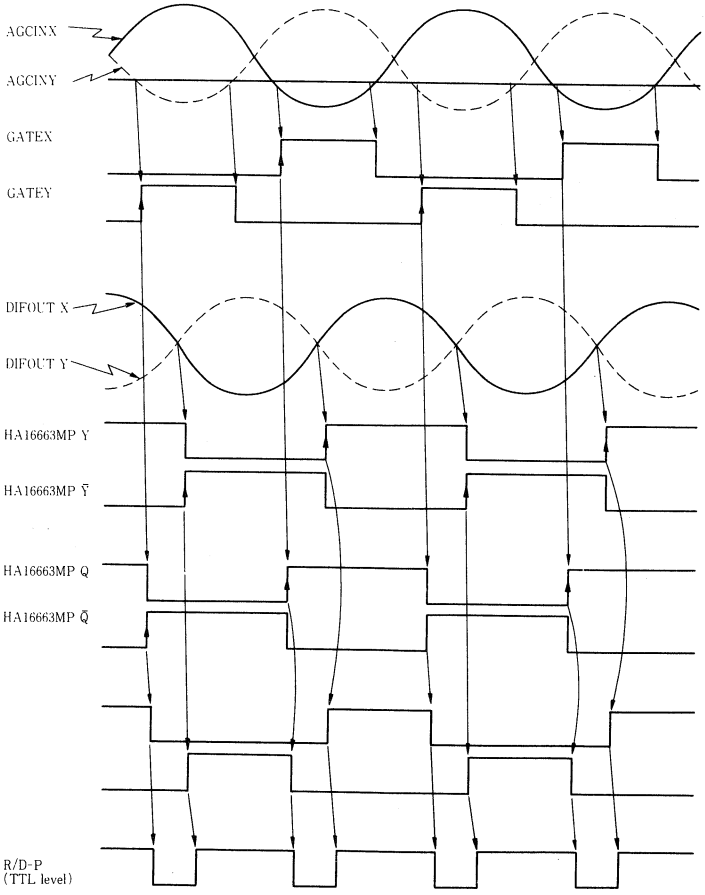
Note 1 : R=220Ω and C=0.1μF are connected serially between GSEL1 and GSEL2.

(to be continued)

	Item	Symbol	Test Conditions	min	typ	max	Unit	Applied Pin	Note
AGC Controller	Differential Input Resistance	R_{IC}		–	10	–	kΩ	AGCINX AGCINY	
	Input Bias Voltage	V_{BC}		4.9	4.95	5.1	V		
	Input Voltage	V_{FSL}		–	4.85	–	V	V_{SL}	
	Input Bias Current	I_{BSH}	V_{FSL}=4.85V	–	–	15	μA		
	Input Voltage	V_{FSH}		–	4.7	–	V	V_{SH}	
	Input Bias Current	I_{BSH}	V_{FSH}=4.7V	–	–	15	μA		
	Charge Output Current	I_{OCH}	V_{FSH}=4.85V	480	800	1420	μA	CHGOUT	
	Discharge Output Current	I_{ODC}	V_{FSL}=4.7V	210	360	640	μA	V_{AGC}	
	External Resistance	R_{RX}	V_{IRX}=0.4V	–	–	7.5	kΩ	RX	
Gate Generator	Input Voltage	V_{FG}		–	1.5	–	V	GGVS	
	Input Bias Current	I_{BG}	V_{FG}=1.5V	−230	–	–	μA		
	"H" Level Output Voltage	V_{OHE}		3.99	4.12	4.3	V	GATEX GATEY	
	"L" Level Output Voltage	V_{OLE}		3	3.2	3.4	V		
	"H" Level Output Voltage	V_{OHG}	I_{OH}=−200μA	2.4	–	–	V	GATEOUT	
	"L" Level Output Voltage	V_{OLG}	I_{OL}=4mA	–	–	0.5	V		
Limiter	Differential Input Resistance	R_{IL}		–	3	–	kΩ	LMTINX LMTINY	
	Input Bias Voltage	V_{BL}		2.7	3	3.3	V		
	Input Offset Voltage	V_{IFL}		−5	–	5	mV		
	"H" Level Output Voltage	V_{OHL}	I_{OH}=−200μA	2.4	–	–	V	LMTOUT	
	"L" Level Output Voltage	V_{OLL}	I_{OL}=4mA	–	–	0.5	V		

Note 2 : C=0.1μF is connected between DIF1 and DIF2.

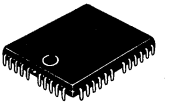
■TIMING CHART



HA16662MP, HA16682MP

● Interface IC for Winchester HDD

HA16662MP/682MP is a monilithic IC designed for ST-506 interface logics in hard disk drive memory systems.



(MP-44)

■ FUNCTIONS

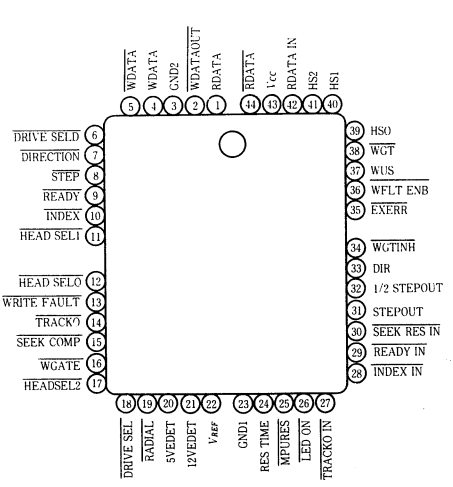
- A pair of RS-422 receiver, driver.
- Line driver for ST-506 interface.
- Line receiver with hysteresis input threshold.
- Included ST-506 interface logics.
- 2 channels supply voltage monitor circuit for 5V and 12V.
- Reset signal generator for micro processor.
- Write gate signal and write fault signal generator for R/W amp. IC.

■ FEATURES

- Can be connected with MPU (6301V, 6301X, 6305V, 8049 etc.) directly.
- Logic components for I/O interface can be reduced.
- No external TTLs and RS-422 receiver driver.
- Write inhibit input for embedded servo system.
- High reliable fail-safe with write inhibit functions at power on period and abnormal supply voltage.
- Small surface mount package (MSP: Mini-Square-Package) for high density PCB.

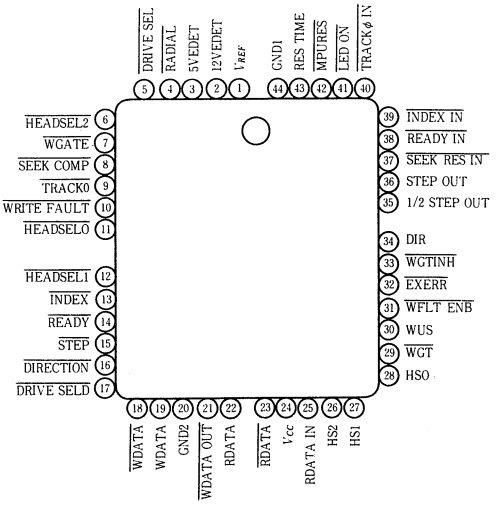
■ PIN ARRANGEMENT

● HA16662MP



(Top View)

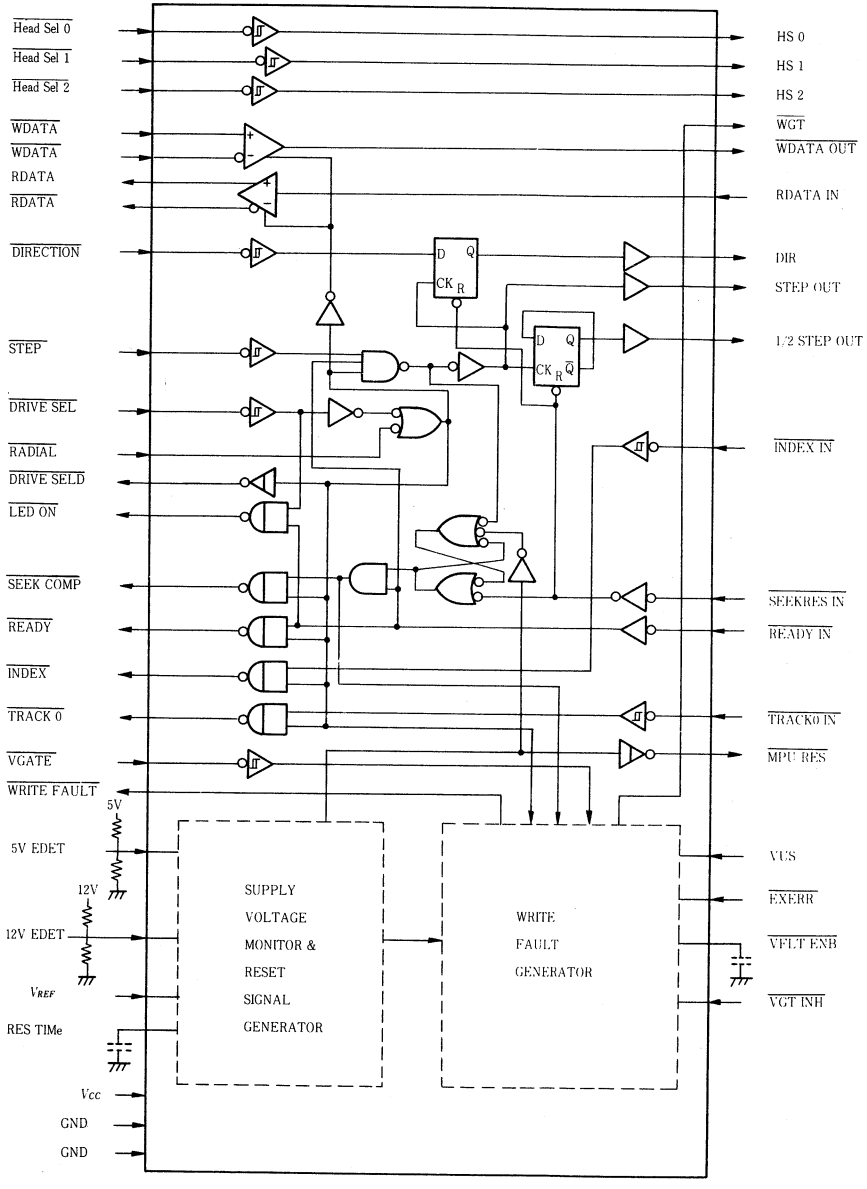
● HA16682MP



(Top View)

HITACHI

■BLOCK DIAGRAM



■ABSOLUTE MAXIMUM RATINGS (T_a=25°C)

Item	Symbol	Ratings	Unit	Note
Supply Voltage	V_{CC}	7	V	
Input Voltage 1	V_{IN1}	7	V	1
Input Voltage 2	V_{IN2}	V_{CC}	V	2
Differential Input Voltage	V_{DIN}	±7	V	3
Output Voltage 1	V_{OUT1}	7	V	4
Output Voltage 2	V_{OUT2}	V_{CC}	V	5
Differential Output Voltage	V_{DOUT}	5.5	V	6
Output Current 1	I_{OUT1}	50	mA	7
Output Current 2	I_{OUT2}	10	mA	8
Output Current 3	I_{OUT3}	10	mA	9
Output Current 4	I_{OUT4}	−0.4	mA	10
Differential Output Current	I_{DOUT}	30	mA	11
Operating Temperature Range	T_{OP}	0 to +70	°C	
Storage Temperature Range	T_{stg}	−55 to +125	°C	
Power Dissipation	P_T	750	mW	

Notes) 1. Applied for schmitt inputs and other inputs equivalent to 74LS04.
(HEAD SEL 0~2, DIRECTION, STEP, DRIVE SEL, TRACK 0 IN, INDEX IN, RDATAIN, SEEK RES IN, READYIN, WUS, EXERR, WGTINH, WGATE)
2. Applied for the following inputs.
(5 VEDET, 12 VEDET, V_{REF}, RESTIME, WFLTENB, RADIAL)
3. Applied for the following differential receiver inputs.
(WDATA, $\overline{\text{WDATA}}$)
4. Applied for the following open collector outputs when being OFF mode.
(DRIVESELD, LED ON, SEEK COMP, READY, INDEX, TRACK0, WRITE FAULT, MPURES)
5. Applied for the following outputs when being High.
(HS 0~2, WGT, WDATAOUT, DIR, STEPOUT, 1/2 STEPOUT)
6. Applied for the following differential driver outputs when being High.
(RDATA, $\overline{\text{RDATA}}$)
7. Applied for the following open collector outputs when being ON mode.
(DRIVE SELD, LED ON, SEEK COMP, READY, INDEX, TRACK 0, WRITE FAULT)
8. Applied for the following open collector output when being ON mode.
(MPURES)
9. Applied for the following outputs when being Low.
(HS 0~2, WGT, WDATA OUT, DIR, STEPOUT, 1/2 STEPOUT)
10. Applied for the same outputs as note 9 when being outputs High.
11. Applied for the following differential driver outputs.
(RDATA, $\overline{\text{RDATA}}$)

■ELECTRICAL CHARACTERISTICS (T_a=25°C)

Item	Symbol	Applied terminal	Test Condition	min	typ	max	Unit	Note
Supply Voltage Range	V_{CC}			4.5	5.0	5.5	V	
High Level Input Threshold Voltage	V_{T1+}	HEADSEL0 HEADSEL1 HEADSEL2 DIRECTION STEP DRIVESEL WGATE TRACK0IN INDEX IN WGATE	V_{CC}=5V	−	1.7	−	V	
Low Level Input Threshold Voltage	V_{T1-}		V_{CC}=5V	−	0.9	−	V	
Hysteresis	V_{HYS1}		V_{CC}=5V	−	0.8	−	V	
High Level Input Current	I_{IH1}		V_{CC}=5.5V, V_{IN}=2.7V	−	−	20	μA	
Low Level Input Current	I_{IL1}		V_{CC}=5.5V, V_{IN}=0.4V	−0.4	−	−	mA	
Differential Input Voltage	V_{DIN}	WDATA $\overline{\text{WDATA}}$	−5.5V< V_{CM}<5.5V	1.0	−	−	V	
High Level Differential Input Current	I_{IN1+}		V_{IN}=+5.5V, other V_{IN}=0	−	−	1	mA	
Low Level Differential Input Current	I_{IN1-}		V_{IN}=−5.5V, other V_{IN}=0	−1.5	−	−	mA	
Input Hysterisis	V_{DHYS}		V_{CC}=5V, V_{CM}=0V	−	50	−	mV	
High Level Output Voltage 1	V_{OH1}	$\overline{\text{WDATAOUT}}$	V_{CC}=4.75V, $\overline{\text{WDATA}}$=0V, WDATA=1V, I_{OH}=−0.44mA	2.7	−	−	V	
High Level Output Voltage 2	V_{OH2}		V_{CC}=4.5V, $\overline{\text{WDATA}}$=0V, WDATA=1V, I_{OH}=−0.44mA	2.5	−	−	V	
Low Level Output Voltage 1	V_{OL1}		V_{CC}=4.5V, V_{DIN}=1.0V, I_{OL}=4.0mA	−	−	0.4	V	
Low Level Output Voltage 2	V_{OL2}		V_{CC}=4.5V, V_{DIN}=1.0V, I_{OL}=8.0mA	−	−	0.45	V	

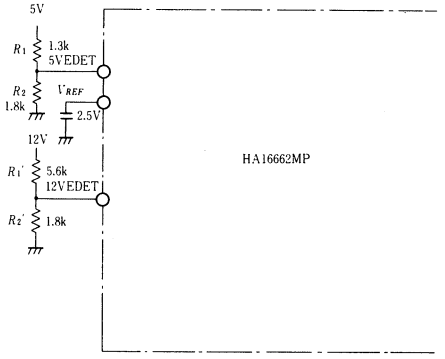
(to be continued)

Item	Symbol	Applied terminal	Test Condition	min	typ	max	Unit	Note
High Impedance Output Current 1	I_{ZOUT1}	$\overline{\text{WDATAOUT}}$	V_{CC}=5.5V, V_O=2.4V	–	–	50	μA	
High Impedance Output Current 2	I_{ZOUT2}		V_{CC}=5.5V, V_O=0.4V	−50	–	–	μA	
High Level Input Voltage 1	V_{IH1}	RDATAIN	V_{CC}=4.5V	2.0	–	–	V	
Low Level Input Voltage 1	V_{IL1}		V_{CC}=5.5V	–	–	0.8	V	
High Level Input Current 2	I_{IH2}		V_{CC}=5.5V, V_{IN}=2.7V	–	–	20	μA	
Low Level Input Current 2	I_{IL2}		V_{CC}=5.5V, V_{IN}=0.4V	−0.36	–	–	mA	
High Level Output Voltage 3	V_{OH3}	RDATA $\overline{\text{RDATA}}$	V_{CC}=4.75V, I_{OH}=−20mA	2.5	–	–	V	
High Level Output Voltage 4	V_{OH4}		V_{CC}=4.5V, I_{OH}=−20mA	2.2	–	–	V	
Low Level Output Voltage 3	V_{OL3}		V_{CC}=4.5V, I_{OL}=20mA	–	–	0.5	V	
High Impedance Output Current 3	I_{ZOUT3}		V_{CC}=5.5V, V_{OUT}=2.5V	–	–	50	μA	
High Impedance Output Current 4	I_{ZOUT4}		V_{CC}=5.5V, V_{OUT}=0.5V	−50	–	–	μA	
Low Level Output Voltage 4	V_{OL4}	DRIVE SELD SEEK COMP READY INDEX $\overline{\text{TRACK0}}$ WRITE FAULT LED ON	V_{CC}=4.5V, I_{OL}=48mA	–	–	0.4	V	
High Level Output Current 1	I_{OH1}		V_{CC}=4.5V, V_{OH}=5.5V	–	–	250	μA	
High Level Input Voltage 2	V_{IH2}	$\overline{\text{SEEK RESIN}}$	V_{CC}=4.5V	2.0	–	–	V	
Low Level Input Voltage 2	V_{IL2}	$\overline{\text{READY IN}}$	V_{CC}=5.5V	–	–	0.8	V	
High Level Input Current 3	I_{IH3}	$\overline{\text{WGTINH}}$	V_{CC}=5.5V, V_I=2.7V	–	–	20	μA	
Low Level Input Current 3	I_{IL3}	WUS	V_{CC}=5.5V, V_I=0.4V	−0.4	–	–	mA	
High Level Input Voltage 3	V_{IH3}	$\overline{\text{RADIAL}}$		2.0	–	–	V	
Low Level Input Voltage 3	V_{IL3}			–	–	0.8	V	
High Level Input Current 4	I_{IH4}		V_{CC}=5.5V, V_I=2.7V	−0.5	–	–	mA	
Low Level Input Current 4	I_{IL4}		V_{CC}=5.5V, V_I=0.4V	−1.2	–	–	mA	
High Level Output Voltage 5	V_{OH5}	HS0 HS1 HS2 $\overline{\text{WGT}}$ DIR STEPOUT 1/2 STEPOUT	V_{CC}=4.75V, V_I=0.8V, I_{OH}=−0.4mA	2.7	–	–	V	
High Level Output Voltage 6	V_{OH6}		V_{CC}=4.5V, V_I=0.8V I_{OH}=−0.4mA	2.5	–	–	V	
Low Level Output Voltage 5	V_{OL5}		V_{CC}=4.5V, V_I=2V, I_{OL}=4mA	–	–	0.4	V	
Low Level Output Voltage 6	V_{OL6}		V_{CC}=4.5V, V_I=2V, I_{OL}=8mA	–	–	0.5	V	
Low Level Output Voltage 7	V_{OL7}	$\overline{\text{MPURES}}$	V_{CC}=4.5V, V_I=2V, I_{OL}=8mA	–	–	0.4	V	
High Level Output Current 7	I_{OH7}		V_{CC}=4.5V, V_I=0.8V, V_{OH}=5.5V	–	–	250	μA	
High Level Input Threshold Voltage	V_{T2+}	$\overline{\text{EXERR}}$ $\overline{\text{WFLTENB}}$	V_{CC}=5V	–	1.7	–	V	
Low Level Input Threshold Voltage	V_{T2-}		V_{CC}=5V	–	0.9	–	V	
Hysteresis	V_{HYS2}		V_{CC}=5V	–	0.8	–	'V	
High Level Input Current	I_{IH5}		V_{CC}=5.5V, V_{IN}=2.7V	–	–	20	μA	
Low Level Input Current	I_{IL5}		V_{CC}=5.5V, V_{IN}=0.4V	−0.4	–	–	mA	
Internal Charge Up Resistance	R_C	$\overline{\text{WFLTENB}}$		140	200	260	Ω	
Sense Voltage Range 1	V_{SVR1}	5VEDET	V_{CC}≧2V	0	–	V_{CC}−1.0	V	
Input Bias Current 1	I_{IB1}		V_{CC}=5.5V, 5VEDET=2.4V, V_{REF}=2.5V, 12VEDET=2.9V	–	40	60	μA	
Input Bias Current 2	I_{IB2}		V_{CC}=5.5V, 5VEDET=5.5V, V_{REF}=2.5V, 12VEDET=2.9V	–	–	2	μA	
Hysteresis	V_{HYS3}		V_{REF}=2.5V, R_1=1.3kΩ, R_2=1.8kΩ	–	(140)	–	mV	1
Sense Voltage Level 1	V_{SVL1}		V_{REF}=2.5V, V_{CC}=5V	2.48	2.50	2.52	V	
Sense Voltage Range 2	V_{SVR2}	12VEDET	V_{CC}≧2V	0	–	V_{CC}−1.0	V	
Input Bias Current 3	I_{IB3}		V_{CC}=5.5V, 12VEDET=2.4V, V_{REF}=2.5V, 5VEDET=2.9V	–	35	50	μA	
Input Bias Current 4	I_{IB4}		V_{CC}=5.5V, 12VEDET=5.5V, V_{REF}=2.5V, 5VEDET=2.9V	–	–	2	μA	
Hysteresis	V_{HYS4}		V_{REF}=2.5V, R_1'=5.6kΩ R_2'=1.8kΩ	–	(270)	–	mV	1

(to be continued)

Item	Symbol	Applied terminal	Test Condition	min	typ	max	Unit	Note
Sense Voltage Level 2	V_{SVL2}		V_{REF}=2.5V, V_{CC}=5V	2.48	2.50	2.52	V	
Applied Reference Voltage Range	V_{REF}	V_{REF}		2	—	V_{CC} -1.0	V	2
Input Bias Current 5	I_{IB5}		V_{CC}=5.5V, 5VEDET=12VEDET=2.9V, V_{REF}=2.5V	−3.0	−1.0	—	μA	
Input Bias Current 6	I_{IB6}		V_{CC}=5.5V, 5VEDET=12VEDET=0V, V_{REF}=5.5V	—	—	2	μA	
High Level Input Threshold Voltage	V_{T3+}	RESTIME	V_{CC}=5V	—	2.3 V_{CC}	—	V	
Low Level Input Threshold Voltage	V_{T3-}		V_{CC}=5V	—	6.10 V_{CC}	—	V	
Capacitor Charge Up Current	I_{CHG}		V_{CC}=5V	0.5	1	2	μA	
Dissipation Current	I_{CC}	V_{CC}	V_{CC}=5.5V	—	—	135	mA	

Note 1. Test circuit is shown in the following schematic.



Calculation of Hysteresis

$$V_{HYS3} = \left\{ K_1 \left(1 + \frac{R_1}{R_2}\right) + \frac{R_1}{K_2} \right\} V_{REF}$$

$K_1 = 0.02 \pm 5\%$

$K_2 = 60K \pm 30\%$

$$V_{HYS4} = \left\{ K_3 \left(1 + \frac{R'_1}{R_2}\right) + \frac{R'_1}{K_4} \right\} V_{REF}$$

$K_3 = 0.0069 \pm 5\%$

$K_4 = 72K \pm 30\%$

Note 2. When applied reference voltage becomes less than 0.6V, supply voltage monitor circuit generates the supply fault signal.

■PIN DESCRIPTION

No.	Terminal Name	I/O	Pin No.	Description
1	WDATA $\overline{\text{WDATA}}$	I	4 5	Differential input terminals for input of write data from hard disk controller, and input characteristics are equivalent to that of "26LS32" in AC and DC characteristics.
2	$\overline{\text{WDATA OUT}}$	O	2	Output of differential write data signal with TTL level. This output turns high impedance when "$\overline{\text{DRIVE SELD}}$" signal is not asserted.
3	RDATA $\overline{\text{RDATA}}$	O	1 44	Differential output terminals of read data which are transmitted to hard disk controller. Output characteristics are equivalent to that of "26LS31".
4	RDATA IN	I	42	Input terminal of read data from read write amplifier. This input has TTL compatible input threshold.

(to be continued)

No.	Terminal Name	I/O	Pin No.	Description
5	$\overline{\text{DIRECTION}}$	I	7	Input terminal for "$\overline{\text{DIRECTION}}$" signal from the hard disk controller. Input characteristics are equivalent to that of "7414".
6	DIR	O	33	Output terminal for the latched "$\overline{\text{DIRECTION}}$" with the leading edge of "$\overline{\text{STEP}}$" signal, and can be reset by "SEEKRES IN" signal.
7	$\overline{\text{STEP}}$	I	8	Input terminal for "$\overline{\text{STEP}}$" signal from the hard disk controller, and its characteristics are equivalent to that of "7414".
8	STEP OUT	O	31	Output terminal for the inverted "$\overline{\text{STEP}}$" Signal.
9	1/2 STEP OUT	O	32	Output terminal for the signal which is devided by two of the inverted "$\overline{\text{STEP}}$" signal.
10	$\overline{\text{SEEK COMP}}$	O	15	Output terminal for the signal which indicates that the seek movement is completed. This signal is disasserted when both "$\overline{\text{MPURES}}$" signal and "$\overline{\text{STEP}}$" signal is asserted, and is asserted when "$\overline{\text{SEEKRES IN}}$" signal is asserted. Output DC characteristics are equivalent to that of "7438".
11	$\overline{\text{SEEKRES IN}}$	I	30	Input terminal for the completed seek operation signal which resets the R-S flip flop for the "$\overline{\text{DIRECTION}}$" signal, the counter for the "$\overline{\text{STEP}}$" signal, and the R-S flip flop for the "$\overline{\text{SEEK COMP}}$" signal.
12	$\overline{\text{READY IN}}$	I	29	Input terminal for the signal which indicates that the hard disk drive is ready.
13	$\overline{\text{READY}}$	O	9	Output terminal for the ready signal which indicates that the HDD is in the ready state. This signal is transfered to hard disk controller and its output DC characteristics are equivalent to that of "7414".
14	$\overline{\text{DRIVE SEL}}$	I	18	Input terminal for the "$\overline{\text{DRIVE SELECT}}$" signal from the hard disk controller. Its input DC characteristics are equivalent to that of "7414".
15	$\overline{\text{DRIVE SELD}}$	O	6	Output terminal for the "$\overline{\text{DRIVE SELECTED}}$" signal to the hard disk controller. Its output DC characteristics are equivalent to that of "7438".
16	$\overline{\text{INDEX IN}}$	I	28	Input terminal for the "$\overline{\text{INDEX}}$" signal. Its input DC characteristics are equivalent to that of "7414".
17	$\overline{\text{INDEX}}$	O	10	Output terminal for the "$\overline{\text{INDEX}}$" signal to the hard disk controller. Its output DC characteristics are equivalent to that of "7438".
18	$\overline{\text{TRACK 0 IN}}$	I	27	Input terminal for the "$\overline{\text{TRACK 0}}$" signal. Its input DC characteristics are equivalent to that of "7414".
19	$\overline{\text{TRACK 0}}$	O	14	Output terminal for the "$\overline{\text{TRACK 0}}$" signal to the hard disk controller. Its output DC characteristics are equivalent to that of "7438".

(to be continued)

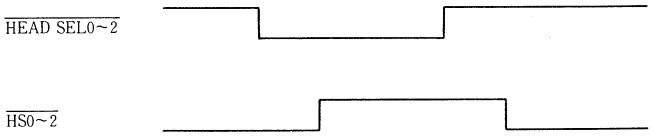
No.	Terminal Name	I/O	Pin No.	Description
20	$\overline{\text{LED ON}}$	O	26	Output terminal for the LED drive signal which indicates that the HDD is in the ready and drive selected state when both the "$\overline{\text{DRIVE SEL}}$" signal and the "$\overline{\text{READY IN}}$" signal are asserted. Its outout DC characteristics are equivalent to that of "7438".
21	$\overline{\text{HEAD SEL 0}}$ ~ $\overline{\text{HEAD SEL 2}}$	I	12 11 17	Input terminals for the "$\overline{\text{HEAD SELECT}}$" signal from the hard disk controller. Its input DC characteristics are equivalent to that of "7414".
22	HS0 ~ HS2	O	39 40 41	Output terminals for the "$\overline{\text{HEAD SELECT}}$" signals to the R/W head amplifier.
23	$\overline{\text{WGATE}}$	I	16	Input terminal for the "$\overline{\text{WRITE GATE}}$" signal from the hard disk controller. Its input DC characteristics are equivalent to that of "7414".
24	$\overline{\text{WGT}}$	O	38	Output terminal for the "$\overline{\text{WGATE}}$" signal to the R/W head amplifier. This signal is disasserted when supply voltage becomes abnormal low, or "$\overline{\text{WUS}}$" signal or "$\overline{\text{EXERR}}$" signal is asserted, and also when "$\overline{\text{WGATE}}$" is asserted with the condition of not seek completed.
25	WUS	I	37	Input terminal for the "WUS" signal from the R/W head amplifier. This signal makes the "$\overline{\text{WFLTENB}}$" signal and the "$\overline{\text{WRITE FAULT}}$" signal be asserted, and disasserted the "$\overline{\text{WGT}}$" signal.
26	$\overline{\text{EXERR}}$	I	35	Input terminal for the external error signal to asserts the "$\overline{\text{WFLT ENB}}$" signal and the "$\overline{\text{WRITE FAULT}}$" signal, and to disasserts "$\overline{\text{WGT}}$" signal.
27	WFLT ENB	–	36	This terminal is used to eliminate the glitch of the "$\overline{\text{WRITE FAULT}}$" signal by connecting with the external capacitor.
28	$\overline{\text{WGT INH}}$	I	34	Input terminal to disassert the "$\overline{\text{WGT}}$" signal. In case of being unused, this terminal may be open.
29	$\overline{\text{WRITE FAULT}}$	O	13	Output terminal for the "WRITE FAULT" signal to the hard disk controller. This signal is asserted when the supply voltage (5 volts to 12 volts) becomes abnormal low, or "WUS" signal or "$\overline{\text{EXERR}}$" signal is asserted, and also when "$\overline{\text{WGATE}}$" is asserted with the condition of not seek completed.
30	$\overline{\text{MPURES}}$	O	25	Output terminal for the reset signal for the microprocessor or peripheral devices. This signal is asserted when the supply voltage (5 volts or 12 volts) becomes abnormal low (includes power on period). The output pulse width can be adjusted by connecting the external capacitor with the "RES TIME" terminal.
31	RES TIME	–	24	This terminal is used for adjusting the pulse width of the "$\overline{\text{MPURES}}$" signal by connecting the external capacitor.

(to be continued)

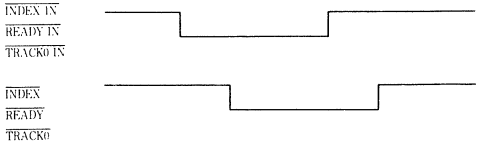
No.	Terminal Name	I/O	Pin No.	Description
32	5VEDET	I	20	This terminal is used to detect the "5 volts" supply voltage fall. Input voltage must be adjusted to the desired detecting value by using the resistance ratio of the external resistor pair against the reference voltage "V_{REF}".
33	12VEDET	I	21	This terminal is used to detect the "12 volts" supply voltage fall. Input voltage must be adjusted against the reference voltage "V_{REF}" by using the same method written in No.32 item.
34	V_{REF}	I	22	Input terminal for the reference voltage of the internal comparators used to detect the supply voltage fall of "5 volts" and "12 volts".
35	$\overline{\text{RADIAL}}$	I	19	Input terminal for radial option.
36	V_{CC}	–	43	5 volts power supply pin.
37	GND1	–	23	Ground pin for the internal bipolar circuit except high current output drivers.
38	GND2	–	3	Ground pin for only internal high current output drivers.

■TIMING SCHEMATICS FOR EACH FUNCTIONAL CIRCUIT.

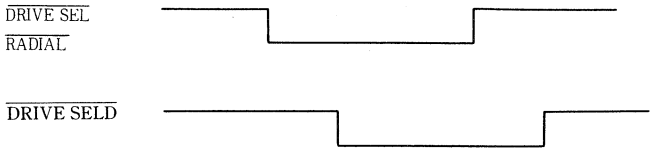
1. $\overline{\text{HEADSEL0}\sim\text{2}}\rightarrow\overline{\text{HS0}\sim\text{2}}$



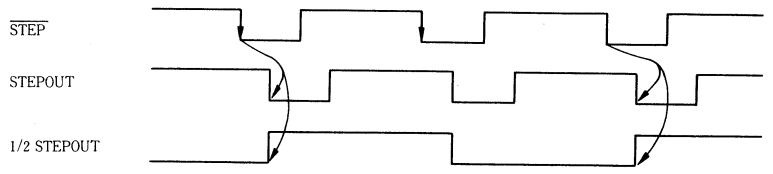
2. $\overline{\text{INDEX IN}}\rightarrow\overline{\text{INDEX}}$
   $\overline{\text{READY IN}}\rightarrow\overline{\text{READY}}$
   $\overline{\text{TRACK0 IN}}\rightarrow\overline{\text{TRACK0}}$



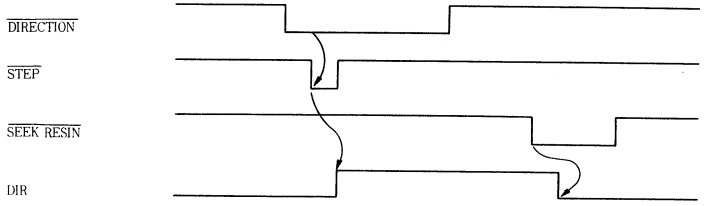
3. $\overline{\text{DRIVE SEL}}\rightarrow\overline{\text{DRIVE SELD}}$
   $\overline{\text{RADIAL}}$



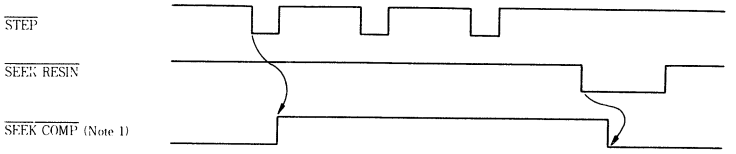
4. $\overline{\text{STEP}}$→STEPOUT
   1/2 STEPOUT



5. $\overline{\text{DIRECTION}}$→DIR

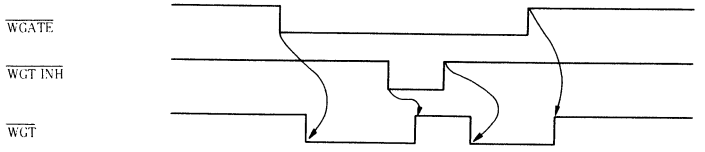


6. $\overline{\text{SEEK COMP}}$

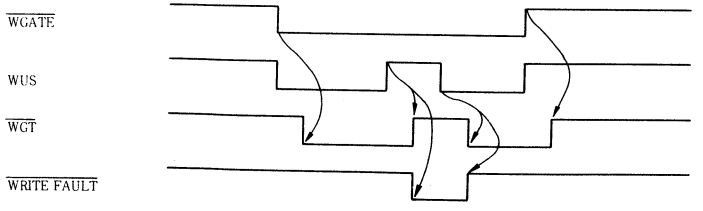


Note 1. This output is kept at high level in the condition of power ON period or abnormal supply voltage.

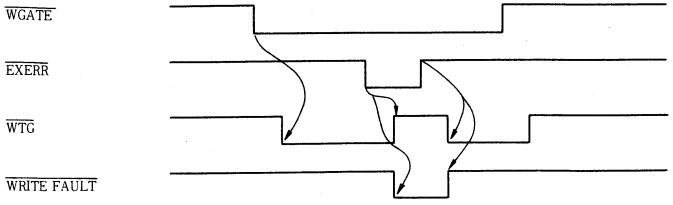
7. $\overline{\text{WGATE}}$→$\overline{\text{WGT}}$
   $\overline{\text{WGT INH}}$



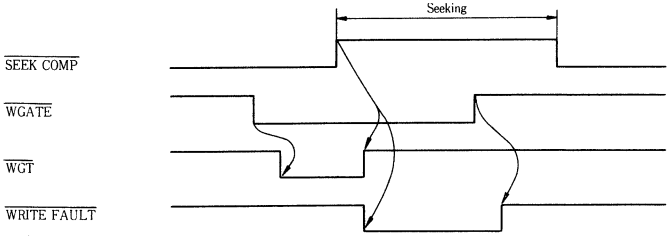
8. $\overline{\text{WGATE}}$→$\overline{\text{WRITE FAULT}}$
   WUS $\overline{\text{WGT}}$



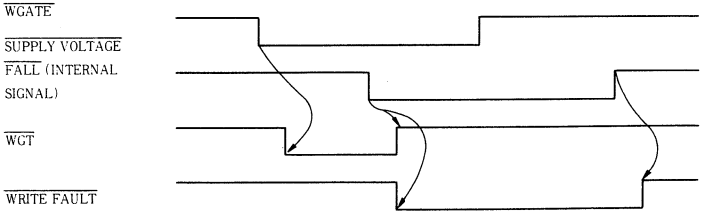
9. $\overline{\text{WGATE}} \rightarrow \overline{\text{WRITE FAULT}}$
   $\overline{\text{EXERR}}$ $\overline{\text{WGT}}$



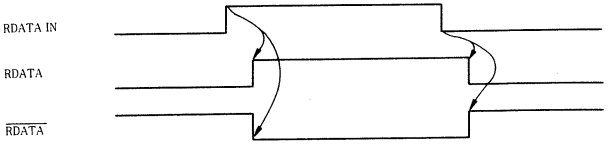
10. $\overline{\text{WGATE}} \rightarrow \overline{\text{WRITE FAULT}}$
    (SEEKING) $\overline{\text{WGT}}$



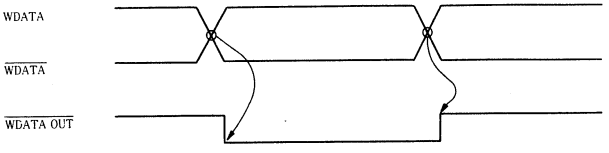
11. $\overline{\text{SUPPLY VOLTAGE FALL}} \rightarrow \overline{\text{WRITE FAULT}}$
    $\overline{\text{WTG}}$



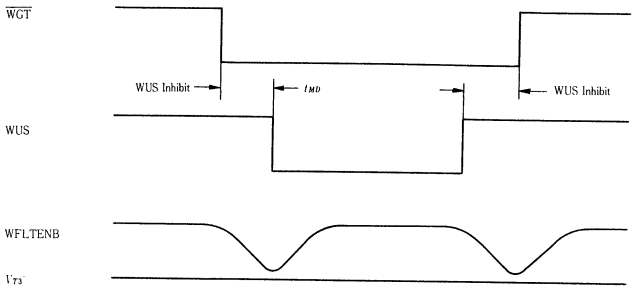
12. RDATA IN→RDATA
    $\overline{\text{RDATA}}$



13. WDATA→$\overline{\text{WDATA OUT}}$
    $\overline{\text{WDATA}}$



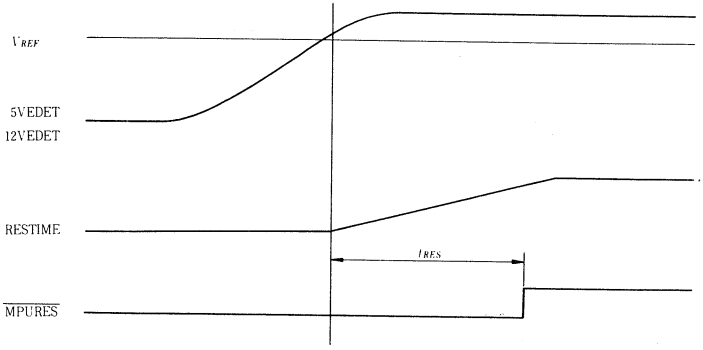
14. $\overline{\text{WFLTENB}}$ TIMING



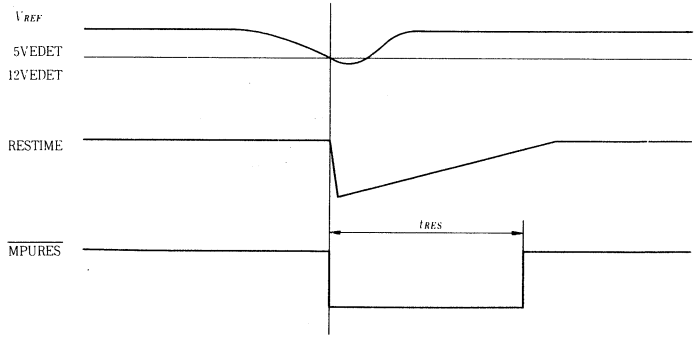
$t_{MD} = 0.38 \cdot 10^3 \cdot C_1$(F) (S)
C_1; Capacitance of an external capacitor connected with the "WFUTENB" Pin.

15. $\overline{\text{MPURES}}$ PULSE TIMING

(1) At power ON period

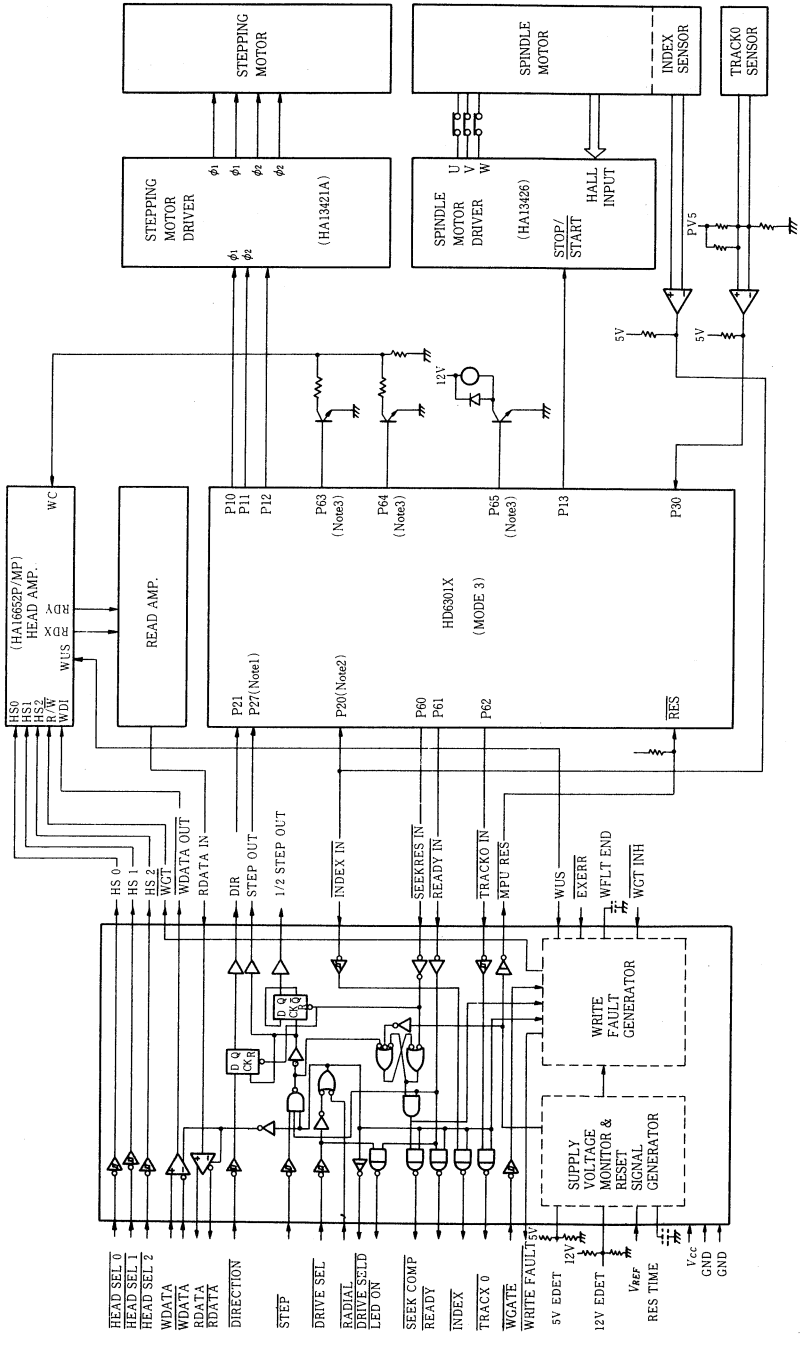


(2) At abnormal supply voltage



$t_{RES} = 4 \cdot 10^6 \cdot C_2$(F) (S)
C_2; Capacitance of an external capacitor connected with the "RESTIME" pin.

■HA16662MP APPLICATION EXAMPLE



(Note 1) P27 ; Event counter input
(Note 2) P20 ; Trigger input of input capture resistor
(Note 3) P63~65 ; Driving outputs for darlington pairs

HA16663MP ●Read Pulse Generator for HDD —Preliminary—

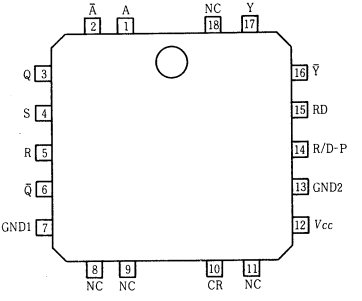
HA16663MP is a read pulse generator IC for regenerating read data pulse by the differential amplifier output and the gate signal of the read data peak detector IC HA16656MP.

(MP-18)

■FEATURES

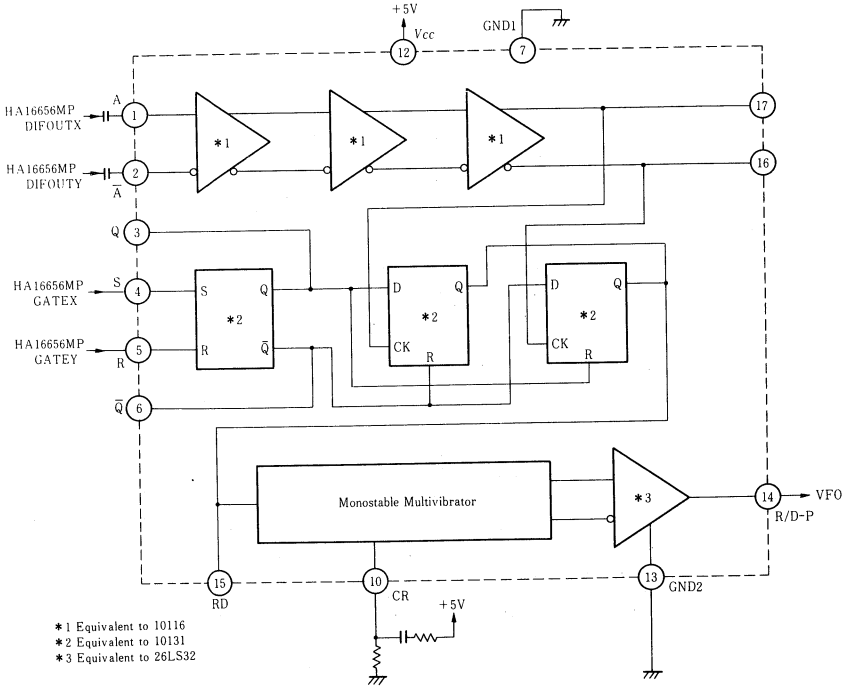
- Generates TTL level output of read data pulse by connecting with HA16656MP.
- The read data pulse output has drive capability equivalent to 26LS32.
- Small, surface-mount package enables high density mounting.
- Assembly board can be small by combining with the read/write IC HA16652P/MP and the read data peak detector IC HA16656MP.

■PIN ARRANGEMENT



(Top View)

■BLOCK DIAGRAM



HITACHI

■ABSOLUTE MAXIMUM RATINGS (T_a=25°C)

Item	Symbol	Ratings	Unit	Applied Terminal
Supply Voltage	V_{CC}	7	V	
Input Voltage	V_I	V_{CC}	V	S, R
Output Current 1	I_{O1}	−2	mA	Y, $\overline{Y}$
Output Current 2	I_{O2}	−2	mA	Q, $\overline{Q}$
RD Output Current	I_{O3}	−2	mA	RD
CR Output Current	I_{OCR}	−30	mA	CR
Low Level Output Current	I_{OL}	+4	mA	R/D-P
High Level Output Current	I_{OH}	−440	μA	R/D-P
Differential Input Voltage	V_{IDIF}	2	Vp-p	A, $\overline{A}$
Operating Temperature Range	T_{opr}	0 to 70	°C	
Storage Temperature Range	T_{stg}	−55 to +125	°C	
Operating Junction Temperature Range	T_{jopr}	135	°C	
Power Dissipation	P_T	680	mW	

■ELECTRICAL CHARACTERISTICS (T_a=25°C, V_{CC}=5V)

Item	Symbol	Test Condition	min	typ	max	Unit	Applied Terminal
Operating Supply Voltage	V_{CC}		4.5	5.0	5.5	V	V_{CC}
Quiescent Current	I_{CC}	V_{CC}=5.5V	−	104	123	mA	
Input Resistance	R_i		−	1k	−	Ω	A, $\overline{A}$
Input Bias Voltage	V_E		2.6	3	3.4	V	
High Level Output Voltage 1	V_{OH1}		3.7	4	4.3	V	Y, $\overline{Y}$
Low Level Output Voltage 1	V_{OL1}		3.0	3.2	3.4	V	
High Level Input Voltage	V_{IH}		3.95	4.1	4.30	V	S, R
Low Level Input Voltage	V_{IL}		3.0	3.2	3.4	V	
High Level Output Voltage 2	V_{OH2}		3.7	4.0	4.3	V	Q, $\overline{Q}$
Low Level Output Voltage 2	V_{OL2}		2.8	3.0	3.2	V	
High Level Output Voltage 3	V_{OH3}		3.9	4.2	4.5	V	RD
Low Level Output Voltage 3	V_{OL3}		3.3	3.5	3.7	V	
High Level Output Voltage 4	V_{OH4}	R_{CR}=2.2kΩ	3.39	3.53	3.80	V	CR
Low Level Output Voltage 4	V_{OL4}	R_{CR}=2.2kΩ	1.80	2.0	2.48	V	
High Level Output Voltage 5	V_{OH5}	V_{CC}=4.5V, I_{OH}=−440μA	2.5	3.4	−	V	R/D-P
Low Level Output Voltage 5	V_{OL5}	V_{CC}=4.5V, I_{OL}=4mA	−	0.2	0.4	V	
Rise Time	t_r	R_{T1}=30Ω, R_{T2}=2.2kΩ, C_T=82pF	−	15	−	ns	
Fall Time	t_f	R_{T1}=30Ω, R_{T2}=2.2kΩ, C_T=82pF	−	4	−	ns	
Propagation Delay Time	t_{pdHL}	R_{T1}=30Ω, R_{T2}=2.2kΩ, C_T=82pF	−	27	−	ns	
Pulse Width	t_W	R_{T1}=30Ω, R_{T2}=2.2kΩ, C_T=82pF	−	46	−	ns	

■PIN DESCRIPTION

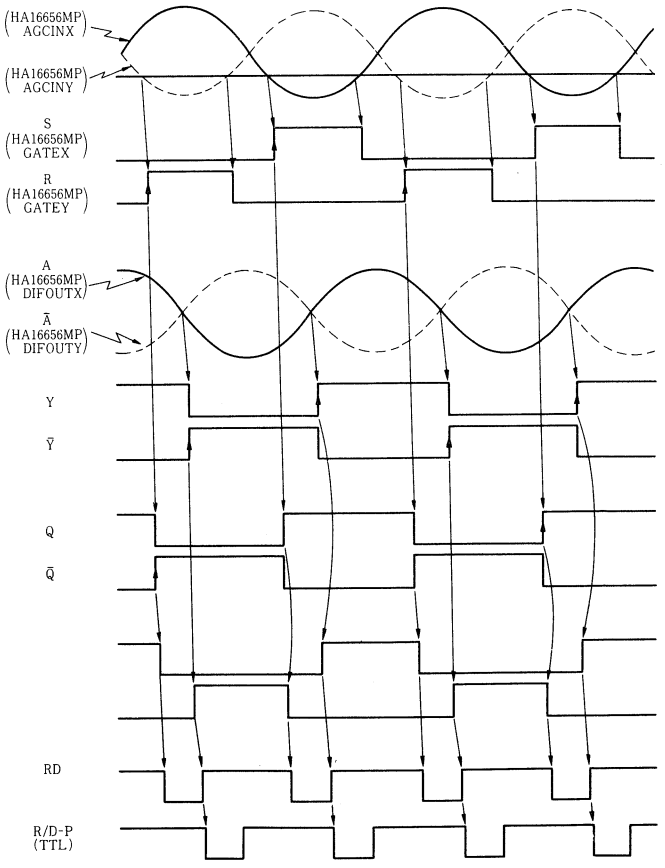
Terminal Name	I/O	Pin No.	Description
V_{CC}	−	12	5 volts power supply pin.
GND1	−	7	Ground pin for the internal Bipolar circuit except high current output drivers.
GND2	−	13	Ground pin for only internal high current output drivers.

(to be continued)

Terminal Name	I/O	Pin No.	Description
A, $\overline{A}$	I	1, 2	Differential input pins for the line receivers, The output of HA16656MP differentiation circuit is applied to these pins.
S, R	I	4, 5	Input pins for the RS latch. The output of HA16656MP gate generator circuit is applied to these pins.
Q, $\overline{Q}$	O	3, 6	Output pins for the RS latch. The signal is at ECL level at output.
RD	O	15	Output pin for the read data. The signal is at ECL level at output.
R/D-P	O	14	Output pin for the read data pulse. The width of the output pulse is determined by the external capacitor and resistor on MM.* The signal is at TTL level at output.
Y, $\overline{Y}$	O	17, 16	Differential output pins for the line receivers.
CR	—	10	This pin provides connections to the capacitor and resistor determining the output pulse width of read data pulse.

• Monstable Multivibrator

■TIMING CHART



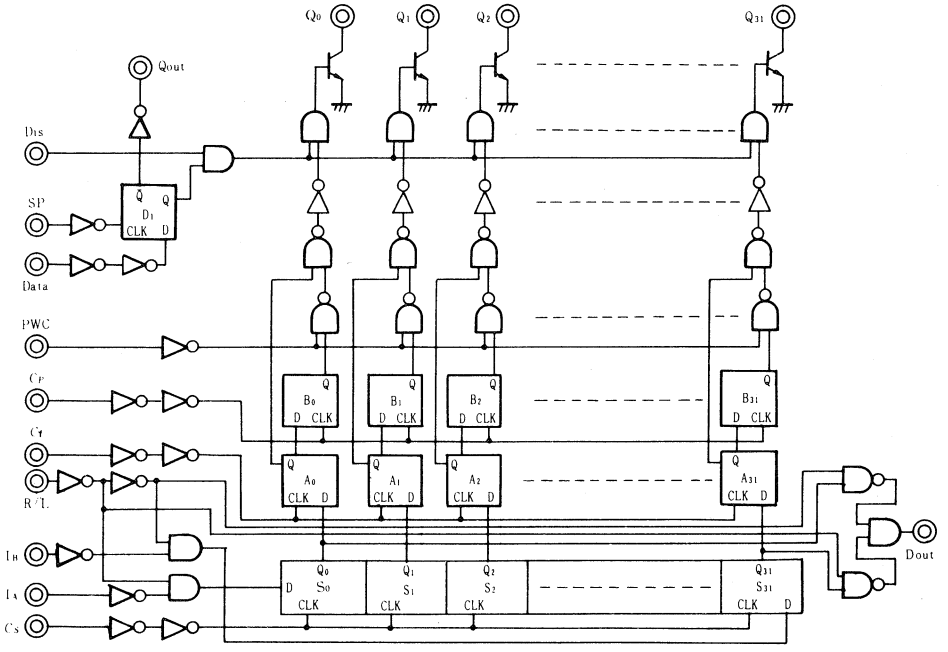
HC16701 ● Thermal Head Driver

HC16701 has a function of serial-in-parallel-out plus 32ch driver, bi-directional shift register, two stage latches, strobe gate and large current driver.
Logic circuits are composed of IIL and output 32ch driver has a capability of driving large current. HC16701 is suitable for applications of thermal head driver and LED display driver.

■ FEATURES

- Each driver of built-in 32ch drivers (NPN Open Collector) has a capability of driving 70mA.
- Enable to shift the shift register in right and left directions by mode select terminals.
- Every channel has two stage latches and is available with controlling output pulse width in the unit of channel.
- Enable to prohibit driver output by Dis terminal. Available with prohibition against driver output at power "ON".
- Built-in D-F/F for selecting chip is available with the application of chip selector in the system of using some HC16701 IC's.

■ BLOCK DIAGRAM



■ MAXIMUM RATINGS ($Ta = +25°C$)

Item	Symbol	Rating	Unit	Remarks
Supply Voltage	V_{CC}	7	V	
Output Sink Current	I_{OL}	100	mA	1
Output Terminal Voltage	V_{OH}	+25	V	2
Power Dissipation	P_C	$T_{j\,max} = 125°C$		
Operating Temperature Range	Ta_{-op}	−20 to +70	°C	
Operating Junction Temperature Range	T_{j-op}	−20 to +100	°C	
Storage Temperature Range	T_{STG}	−35 to +125	°C	

Notes) 1. Applied to output driver terminal Q_0 to Q_{31} when output driver transistor "ON".
2. Applied to output driver terminal Q_0 to Q_{31}, when output driver terminal "OFF".

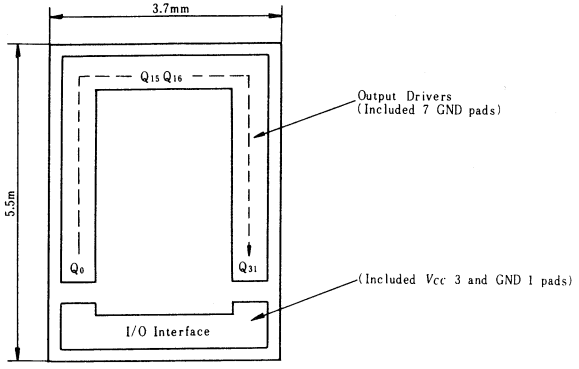
■ELECTRICAL CHARACTERISTICS (T_j = +25°C)

Item	Symbol	Test Condition	min	typ	max	Unit	Applicable Terminals
Operating Supply Voltage	V_{CCop}	V_{CC}=5.0V, Driver:ON Duty 50%	4.5	5.0	5.5	V	V_{CC}
Quiescent Current	I_{CC}	V_{CC}=5.0V, Driver : ON Duty 50%	—	120	160	mA	V_{CC}
Iinj Operating Voltage (Note 5)	V_{inj}		3.0	—	V_{CC}	V	I_{inj}
Injection Current	I_{inj}	V_{CC}=5.0V V_{inj}=5.0V	—	30	—	mA	I_{inj}
Input High Voltage 1	V_{IH1}	V_{CC}=5.0V	3.0	—	—	V	SP, PWC, CP, CT
Input High Voltage 2	V_{IH2}	V_{CC}=5.0V	2.5	—	—	V	CS, IA, IB, DATA
Input High Voltage 3	V_{IH3}	V_{CC}=5.0V	3.0	—	—	V	DIS, R/L
Input Low Voltage 1	V_{IL1}	V_{CC}=5.0V	—	—	0.3	V	SP, PWC, CP, CT
Input Low Voltage 2	V_{IL2}	V_{CC}=5.0V	—	—	0.8	V	CS, IA, IB, DATA
Input Low Voltage 3	V_{IL3}	V_{CC}=5.0V	—	—	0.8	V	DIS, R/L
Input High Current 1	I_{IH1}	V_{CC}=5.0V, CS=IA=IB=5.0V	—	—	150	μA	CS, IA, IB
Input High Current 2	I_{IH2}	V_{CC}=5.0V DATA=5.0V	—	—	150	μA	DATA
Input High Current 3	I_{IH3}	V_{CC}=5.0V DIS=3.5V	—	—	150	μA	DIS
Input High Current 4	I_{IH4}	V_{CC}=5.0V R/L=3.5V	—	—	150	μA	R/L
Input High Current 5	I_{IH5}	V_{CC}=5.0V, SP=PWC=CP=CT=3.5V	—	120	180	μA	SP, PWC, CP, CT
Input Low Current 1	I_{IL1}	V_{CC}=5.5V, CS=IA=IB=GND	−600	−400	—	μA	CS, IA, IB
Input Low Current 2	I_{IL2}	V_{CC}=5.5V, DATA=GND	−600	−400	—	μA	DATA
Input Low Current 3	I_{IL3}	V_{CC}=5.5V, DIS=R/L=GND	−20	—	—	μA	DIS, R/L
Input Low Current 4	I_{IL4}	V_{CC}=5.5V, SP=PWC=CP=CT=GND	−20	—	—	μA	SP, PWC, CP, CS
Output Low Voltage 1 (Note 1)	V_{OL1}	V_{CC}=5.0V, I_{OL}=10mA	—	—	0.3	V	Q_0 to Q_{31}
Output Low Voltage 2 (Note 2)	V_{OL2}	V_{CC}=5.0V, I_{OL}=0.6mA	—	—	0.5	V	Q_{out}
Output Low Voltage 3 (Note 2)	V_{OL3}	V_{CC}=5.0V, I_{OL}=1.2mA	—	—	0.6	V	D_{out}
Output Current 1 (Note 3)	I_{sht1}	V_{CC}=4.5V, D_{out} 2.7V	300	500	—	μA	D_{out}
Output Current 2 (Note 3)	I_{sht2}	V_{CC}=4.5V, Q_{out} 2.7V	150	250	—	μA	Q_{out}
Output Leak Current (Note 4)	I_{leak1}	V_{CC}=5.5V, Q_0 to Q_{31} 25V	—	—	500	μA	Q_0 to Q_{31}

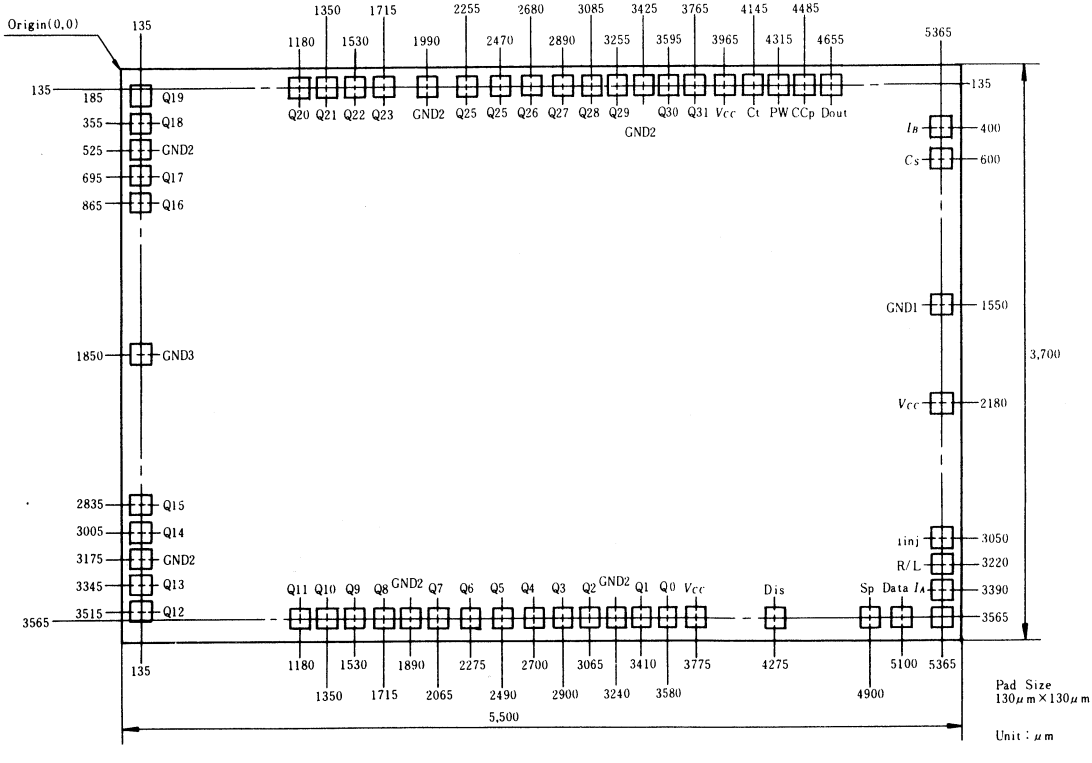
Notes 1. When setting the measuring output driver transistor "ON" and other thirty one output driver transistors "OFF".
2. When setting the state of output "LOW".
3. When setting the state of output "HIGH".
4. When output transistor is "OFF".
5. Iinj is pin for IIL logic power supply.

■PACKAGE (the chip product for sale)

- Chip size; 5.5 x 3.7mm
- The number of pads; 56 pcs. (output driver; 32 pcs. Vcc; 3 pcs. GND; 8 pcs. others; 13 pcs.)
- Pad Arrangement; See the following figure. (an outline)

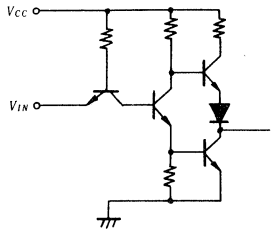


■DICE DIMENSION

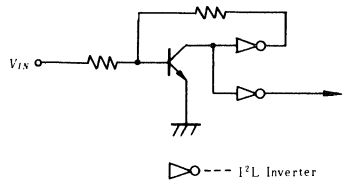


INPUT INTERFACE CIRCUIT

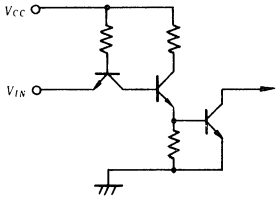
● C_S, I_A, I_B



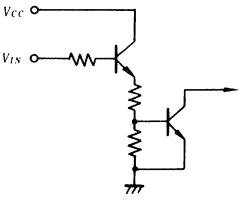
● S_P, C_1, C_P, PWC



● DATA

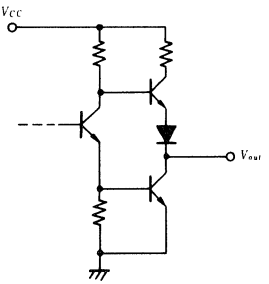


● R/L, D_{IL}

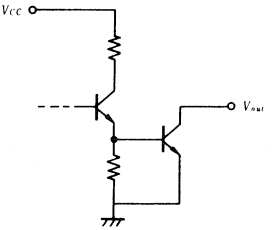


OUTPUT INTERFACE CIRCUIT

● D_{out}, Q_{out}

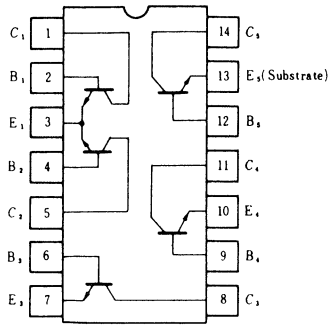


● Q_0~Q_{31}



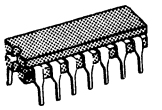
DATA SHEETS
Other Functions

■ PIN ARRANGEMENT

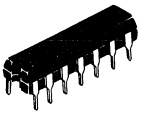


(Top View)

Note: Use pin-13 as the lowest potential of this IC.



(DG-14)



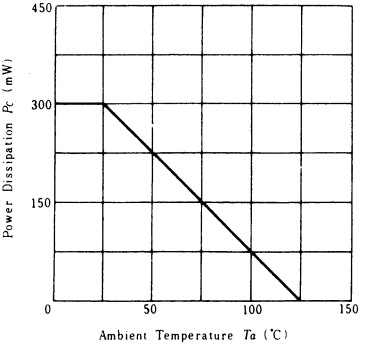
(DP-14)

■ ABSOLUTE MAXIMUM RATINGS (Ta=25°C)

Item	Symbol	HA1127P	HA1127	Unit
Collector-Base Voltage	V_{CBO}	20	20	V
Collector-Substrate Voltage	V_{CIO}	20	20	V
Collector-Emitter Voltage	V_{CEO}	15	15	V
Emitter-Base Voltage	V_{EBO}	5	5	V
Collector Current	I_C	50	50	mA
Collector-Power Dissipation	P_C*	300	300	mW
Collector-Power Dissipation	P_C**	750	750	mW
Operating Temperature	T_{opr}	−55~+125	−55 to +125	°C
Storage Temperature	T_{stg}	−55~+125	−65 to +150	°C

* per transistor. Value under $T_a \leqq 25$°C, In case of more than it, 3mW/°C derating shall be done.
** per package. Value under $T_a \leqq 50$°C, In case of more than it, 7.6mW/°C derating shall be done at HA1127
Value under $T_a \leqq 35$°C, In case of more than it, 8.3mW/°C derating shall be done at HA1127P

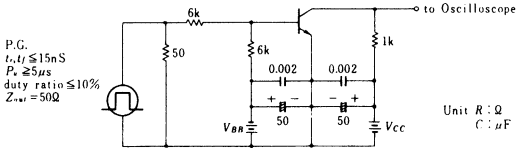
CHANGE IN THE COLLECTOR-POWER DISSIPATION BY THE AMBIENT TEMPERATURE



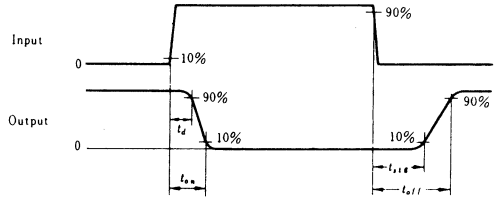
■ ELECTRICAL CHARACTERISTICS (Ta=25°C)

Item	Symbol	Test Conditions		Min	Typ	Max	Unit
Collector-Base Breakdown Voltage	$V_{(BR)CBO}$	I_C=10μA, I_E=0		20	–	–	V
Collector-Emitter Breakdown Voltage	$V_{(BR)CEO}$	I_C=1mA, R_{BE}=∞		15	–	–	V
Collector-Substrate Breakdown Voltage	$V_{(BR)CIO}$	I_C=10μA, I_E=0, I_B=0		20	–	–	V
Emitter-Base Breakdown Voltage	$V_{(BR)EBO}$	I_E=10μA, I_C=0		5	–	–	V
Collector Breakdown Voltage	I_{CBO}	V_{CB}=10V, I_E=0		–	0.002	40	nA
	I_{CEO}	V_{CE}=10V, R_{BE}=∞		–	–	0.5	μA
Collector-Emitter Saturation Voltage	$V_{CE(sat)}$	I_C=10mA, I_B=1mA		–	0.17	–	V
Base-Emitter Voltage	V_{BE}	V_{CE}=3V	I_C=1mA	–	0.72	–	V
			I_C=10mA	–	0.80	–	
Forward Current Transfer Ratio	h_{FE}	V_{CE}=3V	I_C=1mA	40	140	–	
			I_C=10mA	–	120	–	
Gain Bandwidth Product	f_T	V_{CE}=3V, I_C=3mA		–	460		MHz
Collector Output Capacitance	C_{ob}	V_{CB}=3V, I_E=0, f=1MHz		–	1.7	–	pF
Emitter Input Capacitance	C_{ib}	V_{EB}=3V, I_E=0, f=1MHz		–	2.0	–	pF
Switching Time	t_{on}	V_{CC}=10V, I_C=10 I_{B1}=－10 I_{B2}=10mA		–	35	–	ns
	t_{off}			–	130		ns
	t_{stg}			–	75	–	ns

SWITCHING TIME MEASURING CIRCUIT



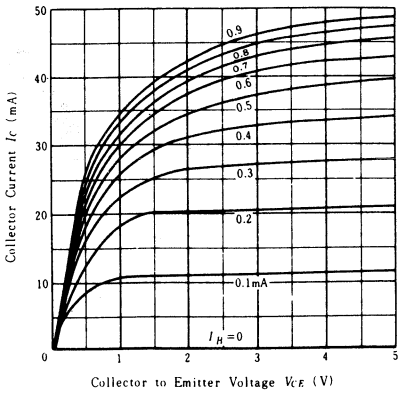
RESPONSE WAVEFORM



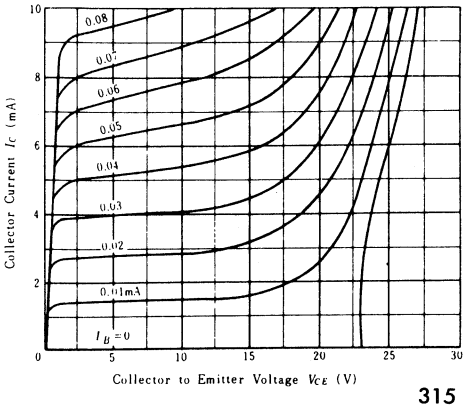
OPERATING CONDITIONS

Symbol	I_C	I_{B1}	I_{B2}	V_{CC}	V_{BB}	V_{in}
Unit	mA	mA	mA	V	V	V
Bias	10	+1.0	−1.0	10.3	−6.0	+13.0

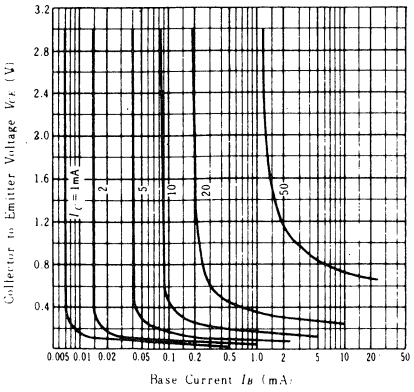
EMITTER GROUNDED STATIC OUTPUT CHARACTERISTICS(1)



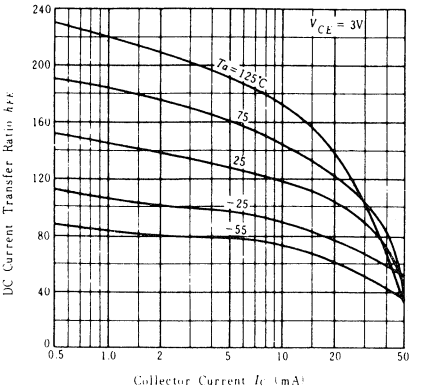
EMITTER GROUNDED STATIC OUTPUT CHARACTERISTICS(2)



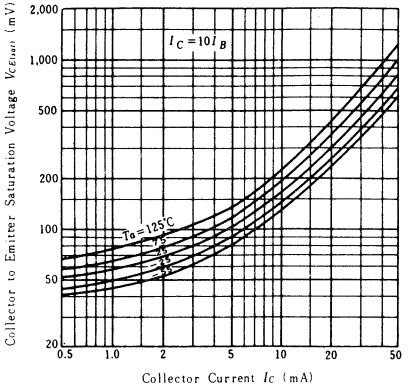
COLLECTOR-EMITTER VOLTAGE VS. BASE CURRENT



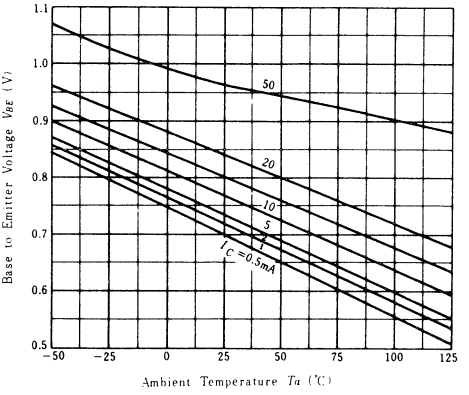
FORWARD CURRENT TRANSFER RATIO VS. COLLECTOR CURRENT



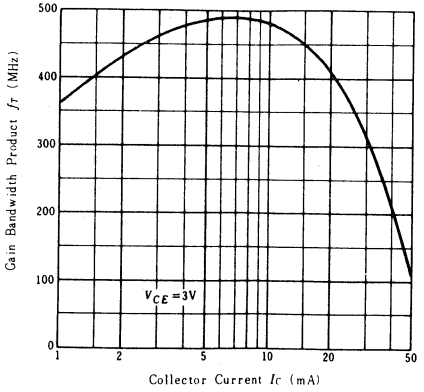
COLLECTOR TO EMITTER SATURATION VOLTAGE VS. COLLECTOR CURRENT



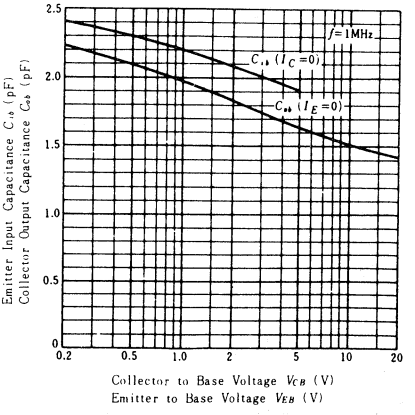
BASE TO EMITTER VOLTAGE VS. AMBIENT TEMPERATURE



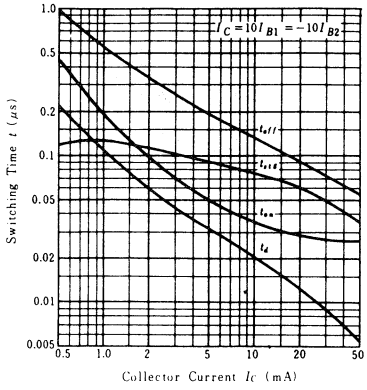
GAIN BANDWIDTH PRODUCT VS. COLLECTOR CURRENT



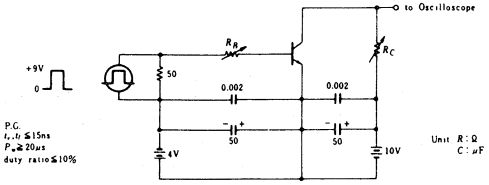
INPUT OUTPUT CAPACITANCE VS. VOLTAGE



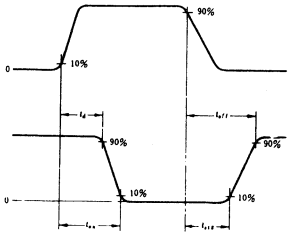
SWITCHING TIME VS. COLLECTOR CURRENT



SWITCHING TIME MEASURING CIRCUIT



RESPONSE WAVEFORM

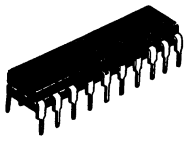


HA16605W ●Burner Controller

Recently burner control equipment has been improved and required to obtain small outline, high performance and multi functions. And now, electronic burner controller is going to become more popular to save energy and to have better safety functions.

The HA16605W is a one chip monolithic IC, integrated of the sequential control part in the burner control equipment. This IC has four sequence control modes, so that it can provide functions for various burner systems.

In each mode, fail-safe functions are provided. And this IC has capability of drive relays directly.

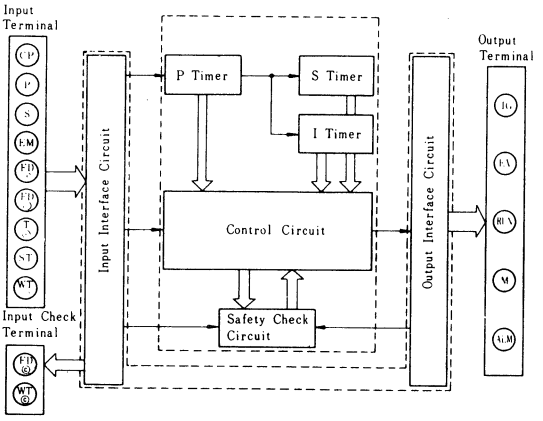


(DP-20)

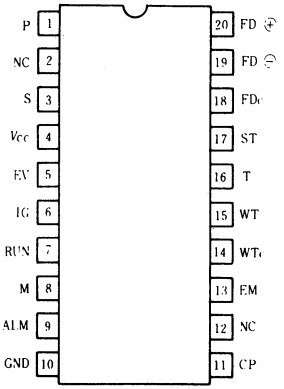
■ FEATURES

- Four kinds of fixed control sequence
- Commercial frequency 50/60Hz can be used for the clock pulse of internal timer.
- Transistors which can drive the power relay directly are built in.
- Comparators are built in.
- Provides safety functions.

■ BLOCK DIAGRAM



■ PIN ARRANGEMANT



(Top View)

■ PIN DESCRIPTION

Pin No.	Symbol	Description
1	$\overline{P}$	Decoder input to discriminate four kinds of control sequence.
2	*NC*	Non Connect
3	*S*	Decoder input to discriminate four kinds of control sequence.
4	V_{CC}	Power Supply
5	*EV**	Power transistor output for driving the magnetic-valve.
6	*IG**	Power transistor output for driving the ignition equipment
7	*RUN**	Power transistor output for driving the operation lamp
8	*M**	Power transistor output for driving the blower motor
9	*ALM**	Power transistor output for driving the alarm lamp
10	*GND*	GND
11	*CP*	Clock signal(50/50Hz)input
12	*NC*	Non connect
13	*EM*	Emergency stop signal input
14	WT_C	Output of the water temperature detection signal
15	*WT*	Input of the water thermo signal
16	*T*	Input of the reference voltage for the water thermo and for the safety thermo
17	*ST*	Input of the safety thermo signal
18	FD_C	Output of the flame detection signal
19	$FD\ominus$	Input of the flame detection signal
20	$FD\oplus$	Input of the reference signal for the flame detection

*Open collector output of NPN transistor

■ABSOLUTE MAXIMUM RATINGS (Ta=25℃)

Item	Symbol	Rating	Unit	Applied Terminal	Note
Supply Voltage	V_{CC}	7.0	V	V_{CC}	
Input Voltage	V_{IN}	−0.5 to V_{CC}+5.0	V	CP, EM	
		−0.5 to V_{CC}+1.0		P, S	
		−0.5 to V_{CC}+3.0		FD⊕, FD⊖, T, ST, WT	1
Output Voltage	V_{out}	−0.5 to V_{CC}+3.0	V	FDc, WTc	
		−0.5 to +25		IG, EV, RUN, M, ALM	2
Output Current	I_{out}	2	mA	FDc, WTc	
		75		IG, EV, M, ALM	3
		100		RUN	
Power Dissipation	P_T	500	mW		
Operating Temperature Range	T_{opr}	−20 to +75	℃		
Storage Temperature Range	T_{stg}	−55 to +125	℃		

Notes: 1. Internal impedance of the drive source should be more than 1kΩ.
2. Allowable value when the output transistor is in OFF state.
3. Allowable value when the output transistor is in ON state.

■ELECTRICAL CHARACTERISTICS

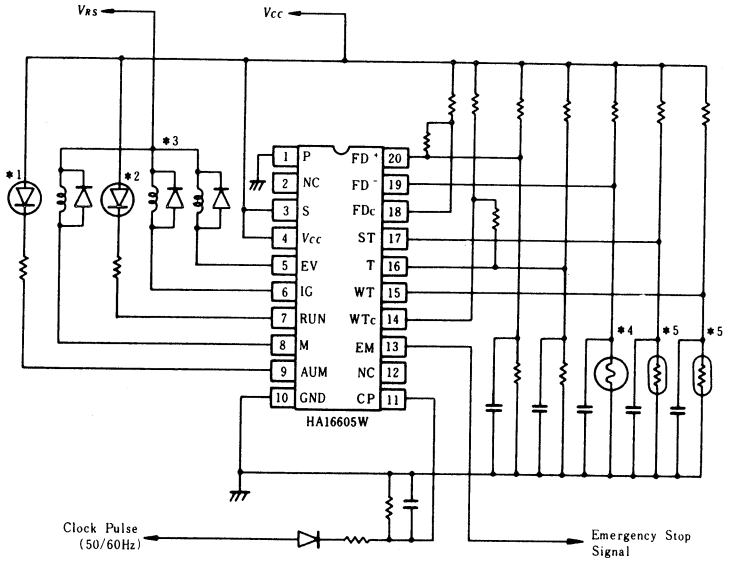
Item		Symbol	Test Condition	min	max	Unit	Application Terminal	Note
Input Voltage	Low	V_{IL}		—	0.6	V	CP, EM	1
	High	V_{IH}		2.8	—			
Input Clamp Voltage		V_{IC}	I_{IC}=−12mA	−1.5	—	V	CP, EM	
Output Voltage (Low Level)		V_{OL}	V_{CC}=4.5V, I_{OL}=2mA	—	0.3	V	FDc, WTc	
			V_{CC}=4.5V, I_{OL}=75mA	—	0.7	V	IG, EV, M, ALM	
			V_{CC}=4.5V, I_{OL}=100mA	—	0.7	V	RUN	
Input Current	Low	I_{IL}	V_{CC}=5.5V, V_{IL}=0V	−200	—	μA	CP, EM	
	High	I_{IH}	V_{CC}=5.5V, V_{IH}=5.5V	—	100	μA		
Output Current (High Level)		I_{OH}	V_{CC}=5.5V, V_{OH}=8.5V	—	0.2	μA	FDc, WTc	
			V_{CC}=5.5V, V_{OH}=20V	—	50	μA	IG, EV, RUN, M	
			V_{CC}=5.5V, V_{OH}=25V	—	1.0	mA	ALM	
Comparator Input Bias Current		I_{IB}	V_{CC}=5.5V, V_I=0V	−250	—	nA		2
Comparator Input Offset Voltage		V_{IO}	V_{CC}=5.0V, V_{ref}=1.4V	—	10	mV		3
Comparator Common Mode Input Voltage		V_{CM}		0	V_{CC}−1.6	V		3
Supply Current		I_{CC}	V_{CC}=5.0V	—	70	mA		
Power Supply Voltage		V_{CC}		4.5	5.5	V		
Maximum Clock Frequency		f_{CP}		10	—	kHz		

Notes: 1. Low and High signal levels applied to terminals CP and EM.
2. This item is applied to the inputs of comparators, FD+, FD−, T, ST and WT.
3. These items are applied to FD+↔FD−, T↔ST and T↔WT of the comparators.

■ SIGNAL STATES AND LEVELS OF I/O INTERFACE

Interface Block	Terminal Name	Signal State	Signal Level
Decoder	P	Connect to V_{CC} at "1" level input, and to GND at "0" level input.	$V_{IH} \geqq 4.0V$ $V_{IL} \leqq 2.0V$
	S		
Clock Interface	CP		$V_{IH} \geqq 2.8V$ $V_{IL} \leqq 0.6V$
Emergency Input	EM	Emergency state is detected at Low level input on this terminal, and ALM output turns ON.	
Comparator	FD⊕	High level on this terminal turns the sequence to the flame detected state.	$0 \leqq V_{CM} \leqq V_{CC} - 1.6V$
	ST	Low level on the inverting input turns the ALM output ON.	
	WT	Low level on the inverting input turns the all sequence Reset.	
Driver	EV, IG, RUN, M, ALM	Output OFF equals to "1" level. Output ON equals to "0" level.	

■ SYSTEM CONNECTION



*1 LED for alarm lamp.
*2 LED for operation monitor lamp.
*3 Relay coils to drive the electromagnetic-valve, the ignition equipment and the blower motor.
*4 Device for flame detection e. g. Cds
*5 Thermistors for detection of water temperature.

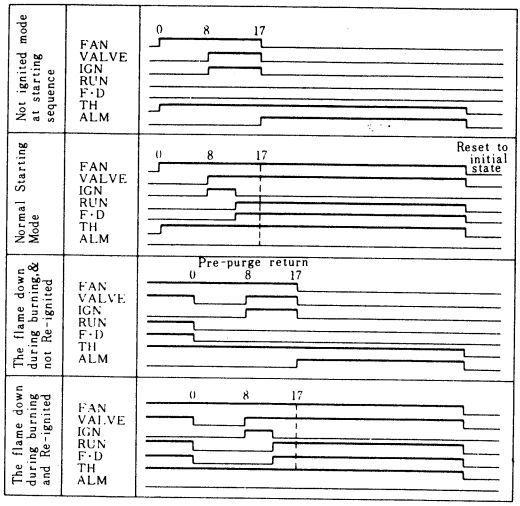
■ SEQUENCE TIME TABLE

Item \ Sequence Code	P 0 S 0	P 1 S 0	P 0 S 1	P 1 S 1
Pre-purge Timing	8 sec	17 sec	17 sec	68 sec
Ignition Timing *1	9 MAX	4 MAX	8 MAX	—
Post-ignition Timing	—	—	17	170
Safety Switch Timing	9	4	8	—
Ignition Return	None	None	Possible	—
Pre-purge Return	Provided	Provided	Provided	—

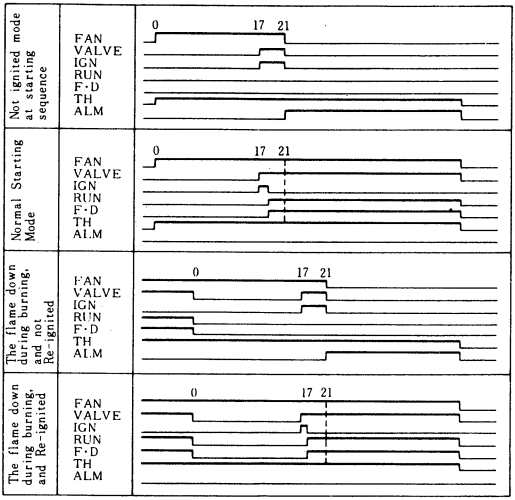
Note) *1 Ignition should be turned off at the same time of flame ON.
*2 All values shown in this table are measured under the condition of that:
clock input : f= 60Hz (commercial frequency)

■ SEQUENCE CHART

● P:0, S:0

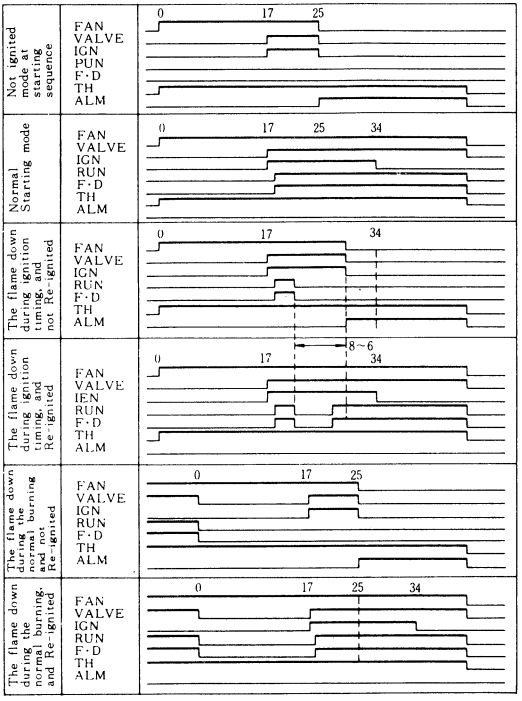


● P:1, S:0

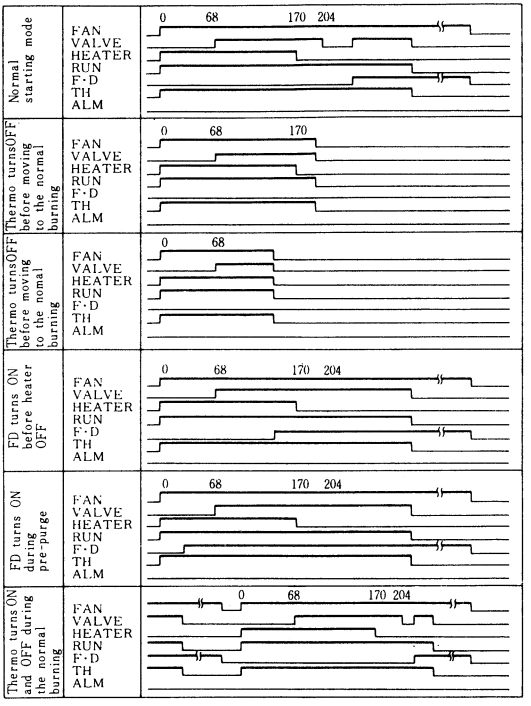


Note) The values in the Time Chart show the operating time (in second) at f=60Hz clock input.

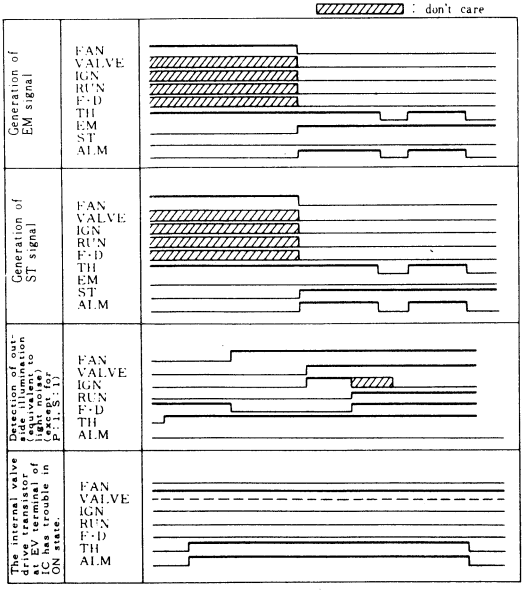
● P:0, S:1



● P:1, S:1

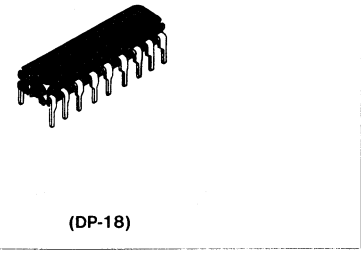


● P:＊, S:＊(in abnormal conditions)



HA16617P, HA16619P ●Fluorescent Display Drivers

HA16617P and HA16619P are fluorescent display drivers operating in high voltage which use positive and negative power source, respectively.



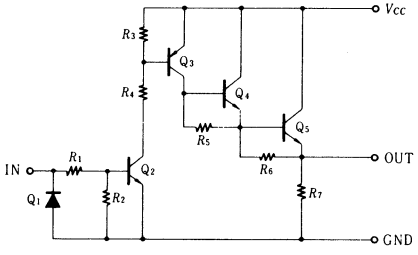
(DP-18)

■ FEATURES

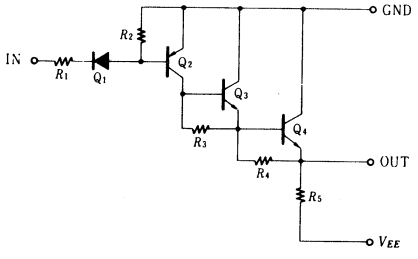
- Capable of driving fluorescent display tube directly because of the built-in 8 circuits and the built-in pull down resistors at output.
- For the inputs, CMOS or TTL accepted.
- The output pulse is non-inverted or inverted from the input pulse in HA16617P or HA16619P, respectively.

■ CIRCUIT SCHEMATIC (1/8)

●HA16617P

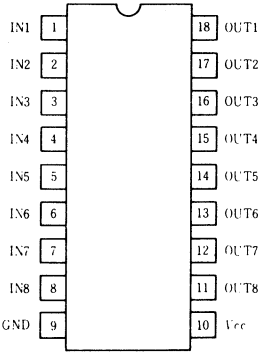


●HA16619P



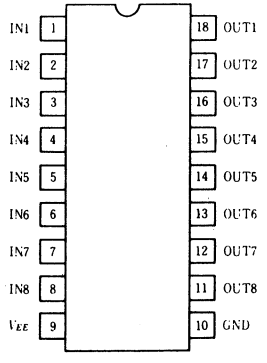
■PIN ARRANGEMENT

●HA16617P



(Top View)

●HA16619P



(Top View)

■ ABSOLUTE MAXIMUM RATINGS (Ta=25°C)

Item	Symbol	HA16617P	HA16619P	Unit
Supply Voltage	V_{EE}	−0.3 to +65	+0.3 to −65	V
Input Voltage	V_{in}	−0.5 to +10	+0.5 to −10	V
Output Voltage	V_{out}	−0.3 to +65	+0.3 to −65	V
Output Current*	I_{out}	−45	−45	mA
Power Dissipation**	P_T	625	625	mW
Operating Temperature	T_{opr}	−20 to +75	−20 to +75	°C
Storage Temperature	T_{stg}	−55 to +125	−55 to +125	°C

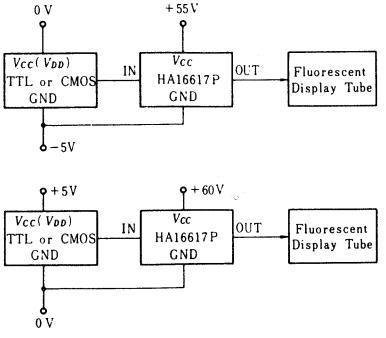
* When only one circuit turns ON.
** Value when $Ta \leqq 50$°C. Derating curve above Ta=50°C shall be 8.3mW/°C.

■ ELECTRICAL CHARACTERISTICS (Ta=−20 to +75°C)

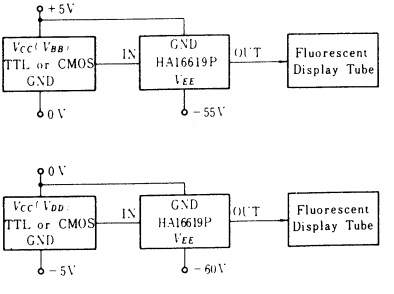
Item	Symbol	Test Conditions	HA16617P			HA16619P			Unit
			min	typ	max	min	typ	max	
Input Voltage	V_{IH}	V_{CC}=60V, $V_O \geqq$ 57V	2.4	—	—	—	—	—	V
		V_{EE}=−60V, $V_O \leqq$ −55V	—	—	—	—	—	−1.5	
	V_{IL}	V_{CC}=60V, $V_O \leqq$ 3V	—	—	0.4	—	—	—	V
		V_{EE}=−60V, $V_O \geqq$ −3V	—	—	—	−4	—	—	
Input Current	I_{IH}	V_{CC}=60V, V_{in}=2.4V	—	—	0.22	—	—	—	mA
		V_{CC}=60V, V_{in}=5V	—	—	0.45	—	—	—	
		V_{EE}=−60V, V_{in}=−1.5V	—	—	—	−280	—	—	μA
	I_{IL}	V_{CC}=60V, V_{in}=0.4V	—	—	80	—	—	—	μA
		V_{EE}=−60V, V_{in}=−4V	—	—	—	−1.2	—	—	mA
		V_{EE}=−60V, V_{in}=−7V	—	—	—	−2.6	—	—	
Output Voltage	V_{OH}	V_{CC}=60V, V_{in}=2.4V, I_O=−40mA	57	58.5	—	—	—	—	V
		V_{EE}=−60V, V_{in}=−4V, I_O=−40mA	—	—	—	−3	−1.5	—	
	V_{OL}	V_{CC}=60V, V_{in}=0.4V	—	—	3.0	—	—	—	V
		V_{EE}=−60V, V_{in}=−1.5V	—	—	—	−55	—	—	
Quiescent Current	$I_{CC(OFF)}$	V_{CC}=60V, all Circuit V_{in}=0.4V	—	0.04	0.4	—	—	—	mA
	$I_{EE(OFF)}$	V_{EE}=−60V, All Circuit V_{in}=−1.5V	—	—	—	−1.3	—	—	
	$I_{CC(ON)}$	V_{CC}=60V, One Circuit V_{in}=2.4V	—	—	4.0	—	—	—	mA
	$I_{EE(ON)}$	V_{CC}=−60V, All Circuit V_{in}=−4V	—	—	—	−12	—	—	

■ APPLICATIONS

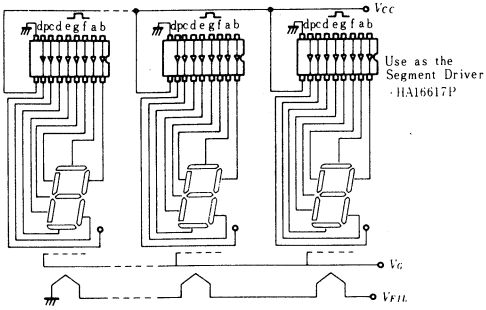
● HA16617P



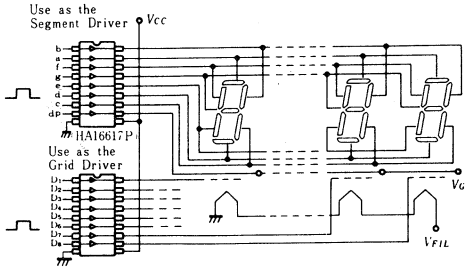
● HA16619P



■ BASIC CIRCUIT



(a) Static Type

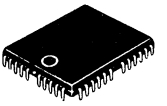


(b) Dynamic Type

HA16721MP, HA16722MP

●32 Output High Voltage Driver IC for Flat Display

HA16721MP and HA16722MP are good for a flat display, especially a driver of vacuum fluorescent display (VFD). High speed logic circuits operating at lock frequency of 5MHz and push-pull output circuits of 150V high voltage are integrated in one chip. By using small package (MSP) they are fit for high reliability, high density mounting.

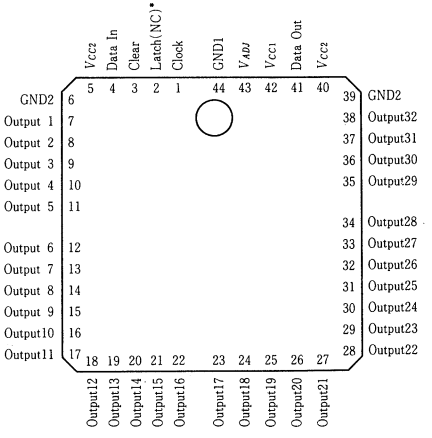


(MP-44)

■ CHARACTERISTICS

HA16721MP	HA16722MP
• 150V high Voltage push-pull outputs. • 5MHz high speed data transfer. • It has 32 push-pull outputs. • Logic circuits are operated at 5V. • It is good for anode driver for VFD.	• 150V high voltage push-pull outputs. • 25mA high output current drive. • It has 32 push-pull outputs. • Logic circuits are operated at 5V. • It is good for grid driver for VFD.

■PIN ARRANGEMENT



(Top View)

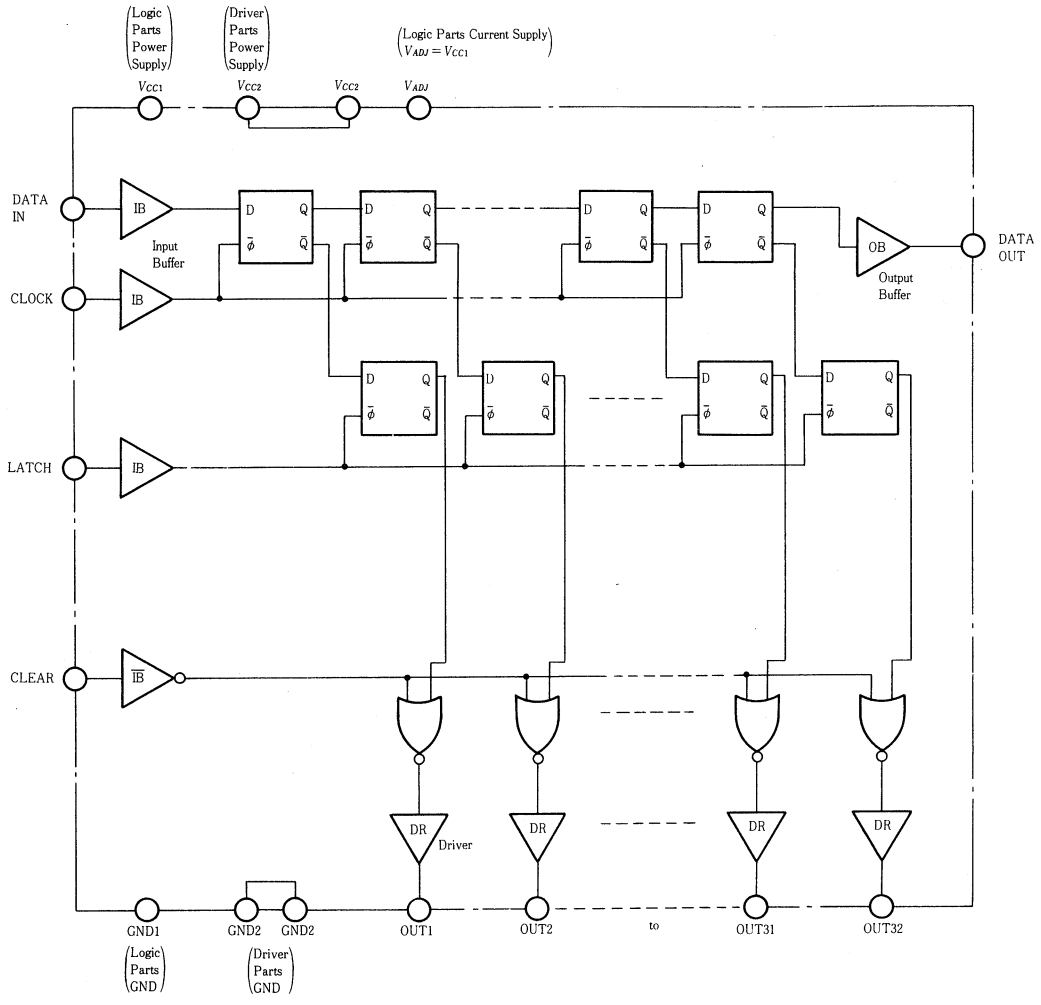
* Latch is used in HA16721MP only.

■ABSOLUTE MAXIMUM RATINGS (T_a=25°C)

Item	Symbol	Rating		Unit
		HA16721MP	HA16722MP	
Logic Parts Supply Voltage	V_{CC1}	7	7	V
Driver Parts Supply Voltage	V_{CC2}	150	150	V
Logic Parts Input Voltage	V_{in}	−0.3 to +7	−0.3 to +7	V
Logic Parts Output Voltage	V_{Dout}	7	7	V
Driver Parts Output Voltage	V_{out}	150	150	V
Logic Parts Current Supply Terminal	V_{ADJ}	7	7	V
Logic Parts Output Current	$I_{Dsource}$	−2	−2	mA
Logic Parts Output Current	I_{Dsink}	2	2	mA
Driver Parts Output Current	$I_{Osource}$	−1	−25	mA
Driver Parts Output Current	I_{Osink}	2	2	mA
Power Dissipation	P_T	750	750	mW
Operating Temperature Range	T_{opr}	0 to +70	0 to +70	°C
Storage Temperature Range	T_{stg}	−55 to +125	−55 to +125	°C

■BLOCK DIAGRAM

● ANODE CIRCUIT (HA16721MP)

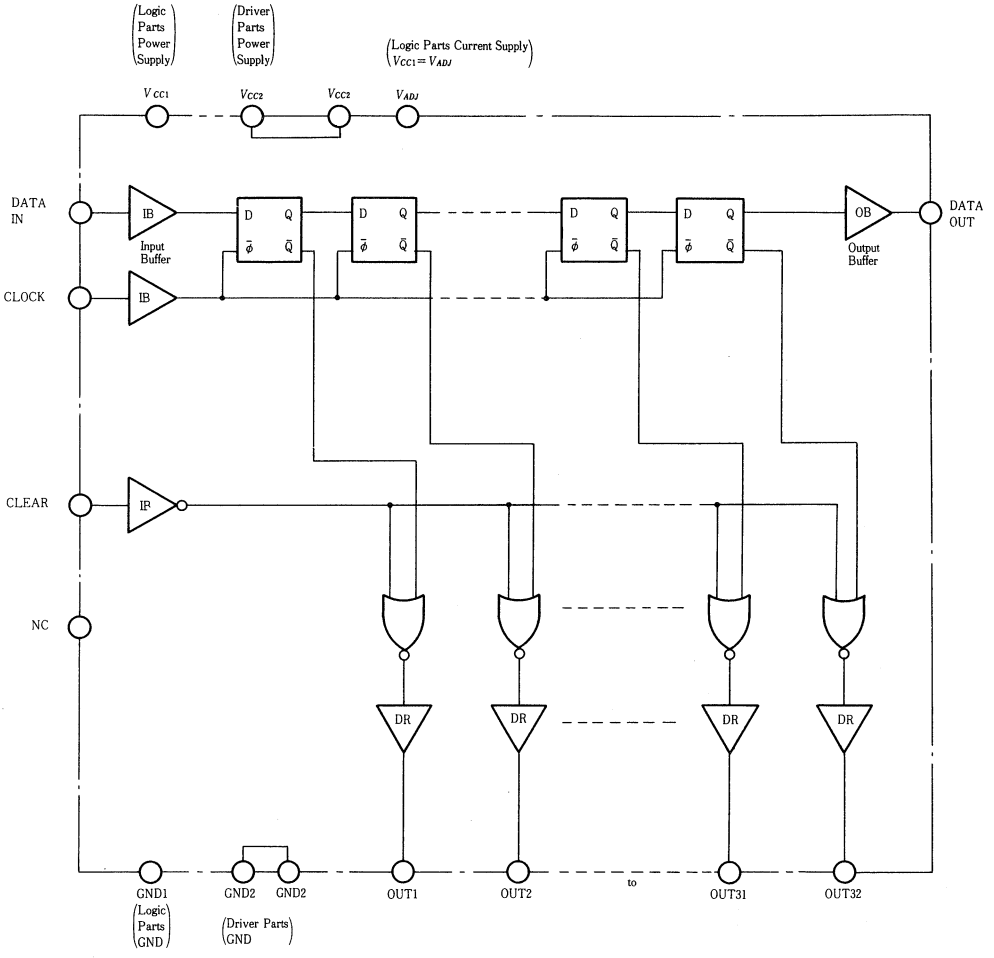


Total 44 pins

FUNCTION

$(DATA)^n_{IN}$	CLOCK	LATCH	CLEAR	$(OUT)^n$
★	★	★	L	L
★	↑	★	H	$(OUT)^{n-1}$
★	↓	L	H	$(DATA\ IN)^n$
★	↓	H	H	$(OUT)^{n-1}$
L	↓	↓	H	L
H	↓	↓	H	H

● GRID CIRCUIT (HA16722MP)



Total 44 pins

FUNCTION

$(DATA)^n_{IN}$	CLOCK	CLEAR	$(OUT)^n$
★	★	L	I.
★	↑	H	$(OUT)^{n-1}$
L	↓	H	L
H	↓	H	H

■ELECTRICAL CHARACTERISTICS

(T_a=25°C, V_{CC1}= V_{ADJ}=5V, V_{CC2}=130V : Unless otherwise specified)

● HA16721MP

Item	Symbol	Test Condition	min	typ	max	Unit	Application Terminal
Input [H] Voltage	V_{IH}		2.0	–	–	V	DATA-IN, LATCH, CLOCK, CLEAR
Input [L] Voltage	V_{IL}		–	–	0.7	V	
Input [H] Current	I_{IH}	V_{in}=2.0V	–	–	10	μA	
Input [L] Current	I_{IL}	V_{in}=GND	−400	−200	–	μA	
Output [H] Voltage	V_{DH}	I_{DH}=−400μA	2.4	–	–	V	DATA-OUT
Output [L] Voltage	V_{DL}	I_{DL}=1mA	–	–	0.4	V	
Output [H] Voltage	V_{OH}	I_{OH}=−1mA	125	–	–	V	OUTPUT
Output [L] Voltage	V_{OL}	I_{OL}=1mA	–	–	2	V	
Logic Parts Quiescent Current	I_{CC1}	(Including I_{ADJ})	–	55	80	mA	
Driver Parts Quiescent Current	I_{CC2}	OUTPUT all "L"	–	2	3	mA	
Logic Parts Operating Supply Voltage Range	$V_{CC1\,opr}$	(= $V_{ADJ\,opr}$)	4.75	5	5.25	V	
Clock Frequency	f_{CLK}		–	–	5	MHz	
Clock Pulse Width	t_{WCLK}		100	–	–	ns	
Set Up Time	t_{su}		60	–	–	ns	
Hold Time	t_h		60	–	–	ns	

● HA16722MP

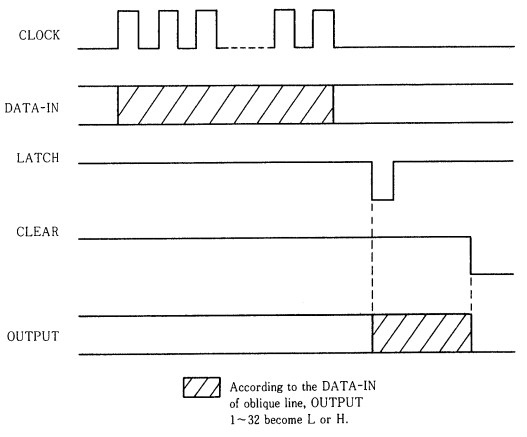
Item	Symbol	Test Condition	min	typ	max	Unit	Application Terminal
Input [H] Voltage	V_{IH}		2.0	–	–	V	DATA-IN, CLOCK, CLEAR
Input [L] Voltage	V_{IL}		–	–	0.7	V	
Input [H] Current	I_{IH}	V_{in}=2.0V	–	–	10	μA	
Input [L] Current	I_{IL}	V_{in}=GND	−400	−200	–	μA	
Output [H] Voltage	V_{DH}	I_{DH}=−400μA	2.4	–	–	V	DATA-OUT
Output [L] Voltage	V_{DL}	I_{DL}=1mA	–	–	0.4	V	
Output [H] Voltage	V_{OH}	I_{OH}=−20mA	125	–	–	V	OUTPUT
Output [L] Voltage	V_{OL}	I_{OL}=1mA	–	–	2	V	
Logic Parts Quiescent Current	I_{CC1}	(Including I_{ADJ})	–	50	75	mA	
Driver Parts Quiescent Current	I_{CC2}	OUTPUT all "L"	–	2	3	mA	
Logic Parts Operating Supply Voltage Range	$V_{CC1\,opr}$	(= $V_{ADJ\,opr}$)	4.75	5	5.25	V	
Clock Frequency	f_{CLK}		–	–	1	MHz	
Clock Pulse Width	t_{WCLK}		500	–	–	ns	
Set Up Time	t_{su}		250	–	–	ns	
Hold Time	t_h		250	–	–	ns	

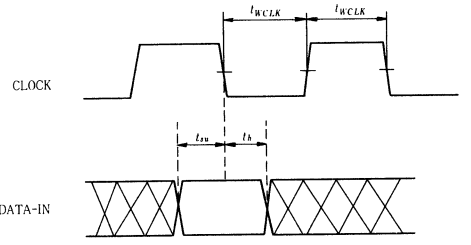
■PIN EXPLANATION

Symbol	Pin Name	Remarks	Symbol	Pin Name	Remarks
V_{CC1}	Logic Supply Voltage		V_{CC2}	Driver Supply Voltage	Connect with 5pin, 40pin
GND1	Logic GND	Connect with GND2	GND2	Driver GND	Connect with 6pin, 39pin.
V_{ADJ}	Logic Current Supply	Connect with V_{CC1}	CLOCK	Clock Input	
LATCH	Latch Input	Only HA16721MP	CLEAR	Clear Input	
DATA-IN	Data Input		DATA-OUT	Data Out	
OUTPUT	High Voltage Output		NC	No connect	Only HA16722MP Open

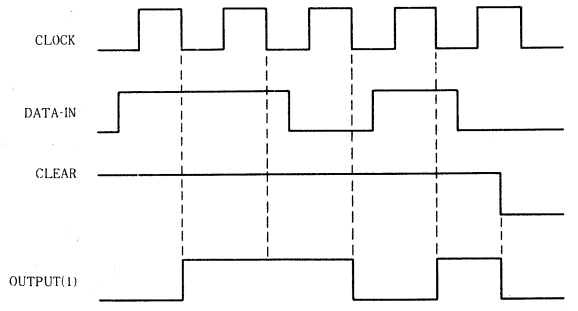
■ TIMING CHART

● HA16721MP





● HA16722MP



HA17555 Series ●Precision Timer

HA17555 is an IC designed for accurate time delays or oscillations.
It provides both of trigger terminal and reset terminal in order to enable a wide scope of application including Mono Multi Vibrator and Astable Multi Vibrator, and the number of external components is fewer. Further, it's compatible with NE555 of Signetics.
Industrial Use: HA17555GS, HA17555PS
Commercial Use: HA17555

HA17555GS

(DG-8)

HA17555PS
HA17555

(DP-8)

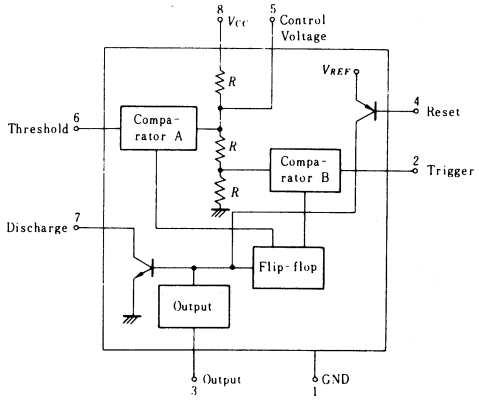
■ FEATURES

- Mono Multi Vibrator can be constructed with one resistor and one capacitor.
- Astable Multi Vibrator can be constructed with two resistors and one capacitor.
- Delay time can be established widely from several μseconds to several hours.
- Pulse Duty can be controlled.
- The maximum value of both sink current and source current is 200mA.
- Direct connection of output to TTL is possible.
- Temperature/delay time ratio is 50ppm/°C (typ).
- Output is normally in the ON and OFF states.

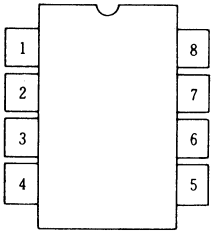
■ APPLICATIONS

- Delay Time Generator (Mono Multi Vibrator)
- Pulse Generator (Astable Multi Vibrator)
- Pulse Width Modulator
- Pulse Location Modulator
- Miss Pulse Detector

■ BLOCK DIAGRAM



■ PIN ARRANGEMENT



(Top View)

1	GND Terminal
2	Trigger Terminal
3	Output Terminal
4	Reset Terminal
5	Control Voltage Terminal
6	Threshold Terminal
7	Discharge Terminal
8	V_{CC} Terminal

■ ABSOLUTE MAXIMUM RATINGS (Ta=25°C)

Item	Symbol	1)HA17555GS	2)HA17555PS	2)HA17555	Unit
Supply Voltage	V_{CC}	18	18	18	V
Discharge Current	I_7	200	200	200	mA
Output Source Current	I_{source}	200	200	200	mA
Output Sink Current	I_{sink}	200	200	200	mA
Power Dissipation	P_T*	600	600	600	W
Operating Temperature	T_{opr}	−20 to +75	−20 to +75	0 to +70	°C
Storage Temperature	T_{stg}	−65 to +150	−55 to +125	−55 to +125	°C

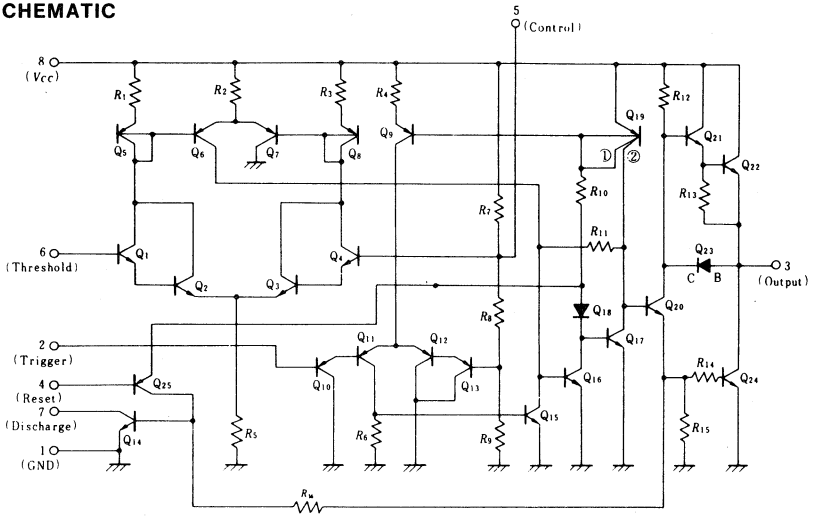
*1) : Value under the condition of $Ta \leqq 35$°C. In case of more than it, 6.7mW/°C derating shall be performed.
2) : Value under the condition of $Ta \leqq 60$°C. In case of more than it, 6.7mW/°C derating shall be performed.

■ ELECTRICAL CHARACTERISTICS (V_{CC}=5 to 15V, Ta=25°C)

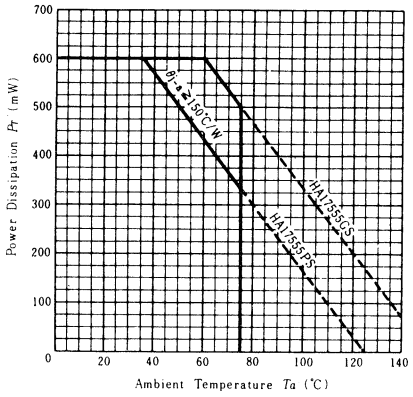
Item		Symbol	Test Condition		min	typ	max	Uuit
Supply Voltage		V_{CC}			4.5	–	16	V
Supply Current *		I_{CC}	V_{CC}=5V, $R_L=\infty$		–	3.0	6.0	mA
			V_{CC}=15V, $R_L=\infty$		–	10	15	
Timing Error **	Inherent Error	E_t				1.0		%
	Ta Dependency		Ta= 20 to +75°C		–	50	–	ppm/°C
	Voltage Dependency		V_{CC}=5 to 15V			0.01		%/V
Threshold Voltage		V_{th}				2/3		xVcc
Trigger Voltage		V_T	V_{CC}=15V			5.0	–	V
			V_{CC}=5V		–	1.67	–	
Trigger Current		I_T			–	0.5		μA
Reset Voltage		V_R			0.2	0.5	1.0	V
Reset Current		I_R				0.1		mA
Threshold Current		I_{th}***				0.1	0.25	μA
Control Voltage		V_C	V_{CC}=15V		9	10	11	V
			V_{CC}=5V		2.6	3.33	4.0	
Output Voltage		V_{OL}	V_{CC}=15V	I_{sink}=10mA	–	0.1	0.25	V
				I_{sink}=50mA	–	0.4	0.75	
				I_{sink}=100mA	–	2.0	2.5	
				I_{sink}=200mA	–	2.5	–	
			V_{CC}=5V, I_{sink}=5mA		–	0.25	0.35	
		V_{OH}	V_{CC}=15V	I_{source}=200mA	–	12.5	–	V
				I_{source}=100mA	12.75	13.3		
			V_{CC}=5V, I_{source}=100mA		2.75	3.3	–	
Output Rise Time		t_r	No loading		–	100	–	ns
Output Fall Time		t_f			–	100	–	ns
Oscillation Pulse Width		t_w	****		10.0		–	μs

*When output is Low (When it is high, I_{CC} is lower by 1mA typically.)
**R_A, R_B: 1k to 100kΩ, C: 0.1μF, V_{CC}: 5V or 15V
***(R_A+R_B) at V_{CC}=15V is determined by the value of Ith. It is 20MΩ max.
****Output pulse width at mono multi circuit. Output high level pulse width at astable circuit

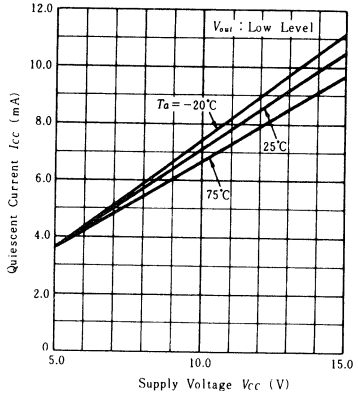
■ CIRCUIT SCHEMATIC



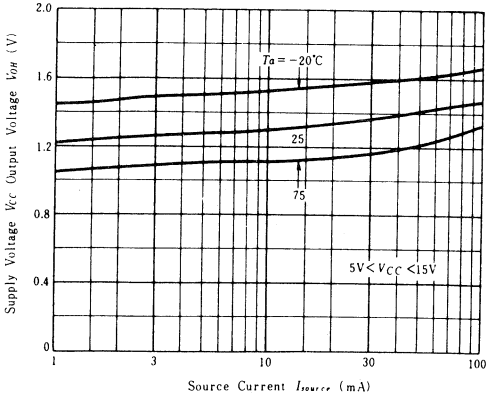
DERATING CURVE



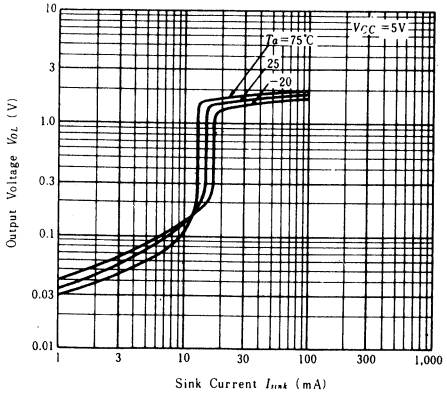
QUIESCENT CURRENT VS. SUPPLY VOLTAGE



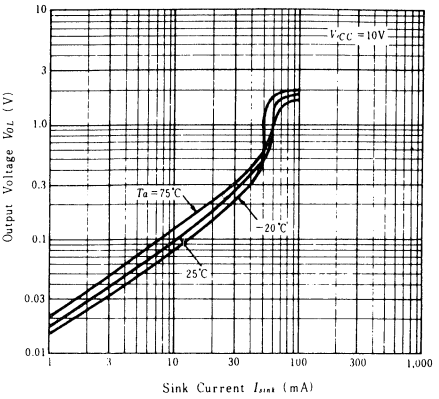
SUPPLY VOLTAGE (V_{CC})-OUTPUT VOLTAGE (V_{OH}) VS. SOURCE CURRENT



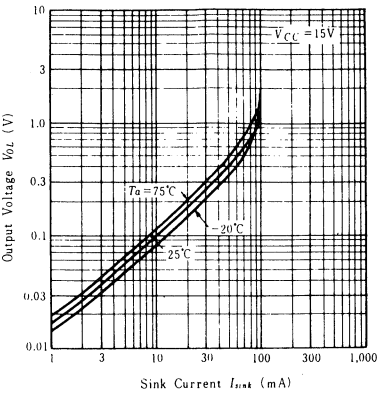
OUTPUT VOLTAGE (V_{OL}) VS. SINK CURRENT (1)



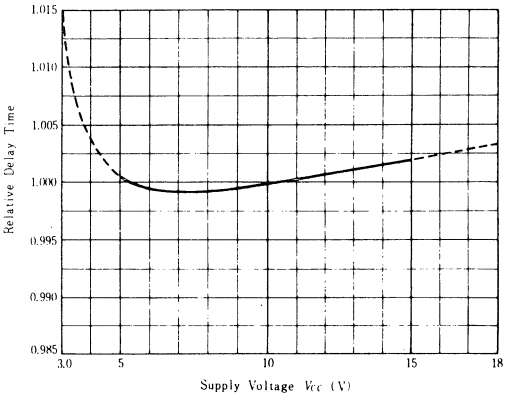
OUTPUT VOLTAGE(V_{OL}) VS. SINK CURRENT (2)



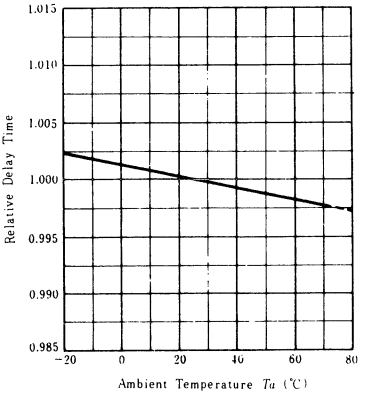
OUTPUT VOLTAGE(V_{OL}) VS. SINK CURRENT (3)



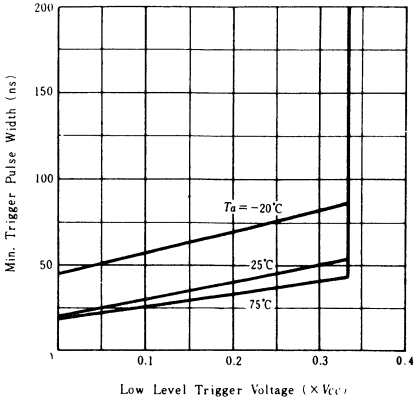
RELATIVE DELAY TIME VS. AMBIENT TEMPERATURE



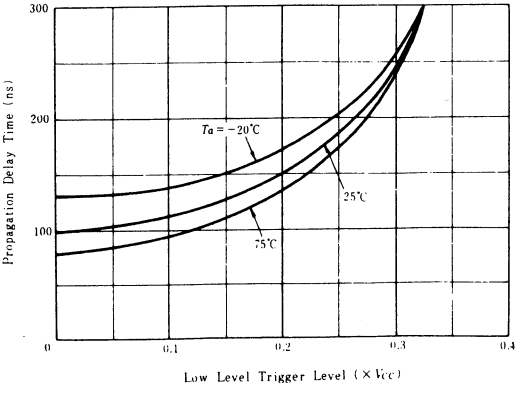
RELATIVE DELAY TIME VS. SUPPLY VOLTAGE



MINIMUM TRIGGER PULSE WIDTH VS. LOW LEVEL TRIGGER VOLTAGE



PROPAGATION DELAY TIME VS. LOW LEVEL TRIGGER VOLTAGE



■DESCRIPTION OF HA17555 OPERATION

HA17555 is an Integrated circuit which can provide accurate a time delay and oscillation. As for time delay or mono multi operation, output pulse width can be determined by an external resistor and a capacitor. At astable operation, oscillation frequency and duty cycle can be controlled by two external resistors and an external capacitor separately. It is possible to attract and induce 200mA current by output. And also, operating voltage can be used at a wide range of supply voltage, 5 to 15V. Particularly when supply voltage is 5V, output level is compatible with TTL input.
HA17555 consists of reference voltage circuit, two kinds of comparators, flip-flop, output circuit, reset and discharge circuits.

1. Reference Voltage Circuit

Supply voltage is divided into three by 5kΩ resistance of R_7, R_8 and R_9. The edge of (2/3) Vcc is connected to comparator A, the edge of (1/3) Vcc is connected to comparator B. And (2/3) Vcc is drown out as a control terminal. By impressing bias at (2/3) Vcc from the outside, it is possible to change threshold level and trigger level of comparator.

2. Comparator A

Comparator A consists of Q_1 and Q_8, R_1, R_2, R_3 and R_5. The base of Q_4 is connected to reference voltage (2/3) Vcc. It switches when voltage of threshold terminal switches (2/3) Vcc off. In other words, when voltage of threshold terminal is beyond (2/3) Vcc, Q_1 and Q_2 which have been cut off is turned "ON", and Q_3 and Q_4 are turned "OFF". So, Q_6 is turned "ON" and resets flip-flop.

3. Comparator B

Comparator B consists of Q_9 through Q_{13}, R_4 and R_6. The base of Q_{13} is connected to reference voltage (1/3) Vcc, it switches when voltage of trigger terminal cuts (1/3) Vcc off. In other words, when voltage of trigger terminal decreased to less than (1/3) Vcc, Q_{10} and Q_{11} which have been cut off are turned "ON". Q_{12} and Q_{13} are turned "OFF". So, trigger is supplied to the set side of flip-flop from the collector of Q_{11}, and flip-flop is set.

4. Flipflop

PS flip-flop consists of Q_{15} through Q_{19}, R_{10} and R_{11}. It is stabilized when Q_{16} is turned "ON" and Q_{17} "OFF", by reset signal from comparator A. On the other hand, it is stabilized when Q_{16} is turned "OFF" and Q_{17} "ON", by set signal from comparator A.

5. Output Circuit

Output circuit consists of Q_{20} through Q_{24}, R_{12} through R_{15}. Output level is determined, according to the state of output transistor Q_{17} of flip-flop. When Q_{17} is "ON", output level is "Higg", and when Q_{17} is "OFF", it is "Low".

6. Reset

By making reset terminal "Low" level, prior to any other input, the reset function can make it "Low" level and starting point of a new cycle.

7. Discharge Circuit

Discharge circuit can discharge or charge timing constant connected to the both edges, by "ON" or "OFF" of Q_{14}. Q_{14} is turned "ON" and discharged at "Low" level or when the above reset is made.

AN EXAMPLE OF OPERATING CIRCUIT

1. Mono Multi Operation

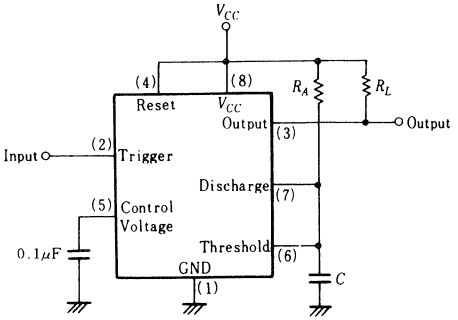


Fig.1 Mono Multi Circuit

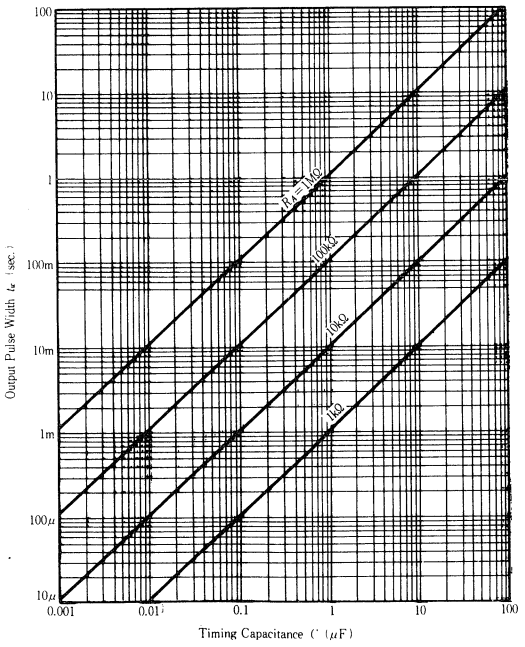


Fig.2 Output Pulse Width vs. Timing Capacitacne

Fig. 1 shows a mono multi circuit using HA17555. It is assumed that the external capacitor C is discharged by discharge transistor Q_{14} inside IC in the beginning.
By adding trigger terminal to negative-going input trigger pulse, flip-flop is set and Q_{14} us turned "OFF". Output is driven to "High".
Capacitor C is charged through resistor R_A at time constant τ = R_AC. When voltage at both edges of capacitor C reach threshold voltage of comparator A, flip-flop is reset and Q_{14} is conducted, capacitor C is discharged. So, output is returned to "Low". Mono multi operation is occurred when negative-going input pulse reaches trigger level. When once mono multi operation is occurred, re-trigger could be made, even if re-trigger signal is added during this period.
According to Fig. 1 and Fig. 2, output pulse width is determined to be tw = 1.1 R_AC. If negative-going pulse is added to reset and trigger terminals at the same time during mono multi operation, capacitor C is discharged and mono multi operation is occurred again at positive edge of reset pulse. Output remains "Low" as long as reset terminal is "Low". When the reset terminal is not used, it is better to connect reset terminal to Vcc in order to prevent miss operation. Fig. 2 shows the characteristics of output pulse width when the values of R_A and C are changed. Operating waveform is shown in Fig. 3. If the reset terminal is connected to mono multi circuit subordinately, it is possible to make sequential timer.

2. Astable Operation

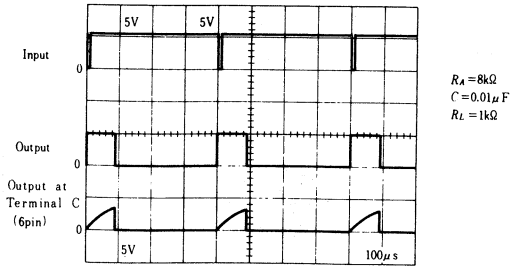
If the second resistor R_B is added to the circuit shown in Fig. 1 and threshold terminal is connected to trigger terminal, HA17555 operates as an astable circuit. Fig. 4 shows the circuit construction of HA17555.
Capacitor C is charged through R_A and R_B, discharged through R_B in this circuit. Therefore, duty cycle can be controlled by R_A and R_B. In Fig. 4, capacitor C charges and discharges between threshold voltage (about 0.67 Vcc) and trigger voltage level (about 0.33 Vcc). Fig. 5 shows a typical example of astable operation. In this figure, time (t_H) when output is "High" level, time (t_L) when output is "Low", oscillation frequency (f) and duty cycle (D) are calculated as follows;

$$t_H = 0.693(R_A + R_B)C$$

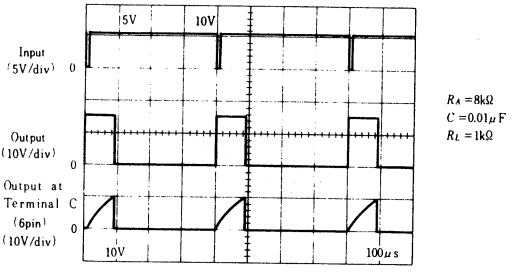
$$t_L = 0.693R_B \cdot C$$

$$f = \frac{1.44}{(R_A + 2R_B)C}$$

$$\text{Duty Cycle} \quad D = \frac{R_B}{(R_A + 2R_B)}$$

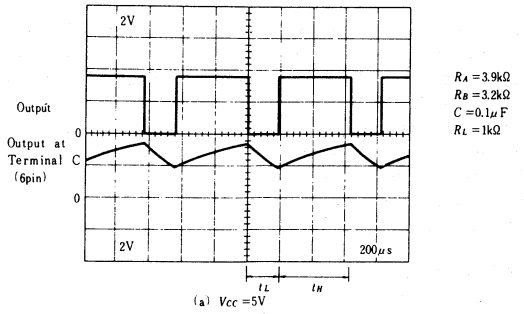


(a) V_{CC} = 5V

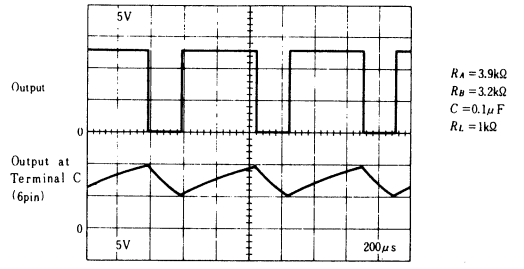


(b) V_{CC} = 15V

Fig.3 Operation Waveform of Mono multi circuit



(a) V_{CC} = 5V



(b) V_{CC} = 15V

Fig.5 Operation Waveform of Astable Circuit

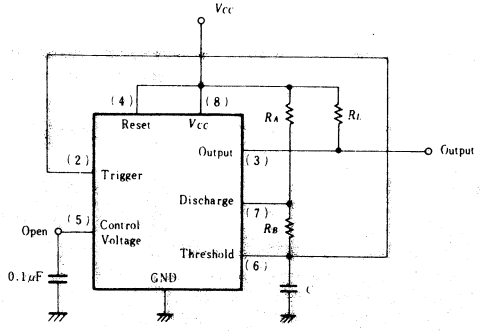
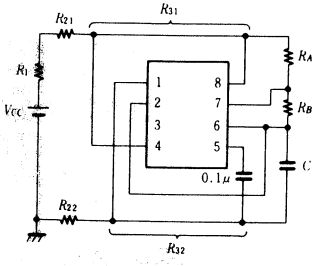


Fig.4 Astable Circuit

3. Cautions in Use

Such integrated circuit for timer as HA17555 type may produce switching noise on power supply and GND line during usage. In this case, abnormal output waveform may be produced by impedance inside power supply or impedance between power supply and GND. So, please take consideration in order to make impedance of each wiring less than the following value at packaging.



R_1 : Power supply output impedance

$R_1 \leqq 50m\Omega$

R_{21}, R_{22} : Lead wiring resistor

$R_{21} + R_{22} \leqq 100m\Omega$

R_{31}, R_{32} : Substrate wiring resistor

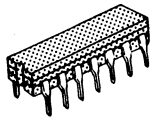
$R_{31} + R_{32} \leqq 20m\Omega$

HA17592 Series ●Differential Video Amplifier —Preliminary—

HA17592 is a video amplifier for wide band with small phasedelay and excellent gain stability. This amplifier eliminates external phase compensation and can fix the gain 100 or 400 without using external elements. If some external elements are used, any gain from 0 to 400 is available. It finds main application in terminal units of computers, interface or video amplifiers.

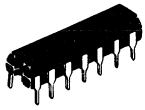
- Industrial Use HA17592G, HA17592P
- Commercial Use HA17592

HA17592G



(DG-14)

HA17592P
HA17592

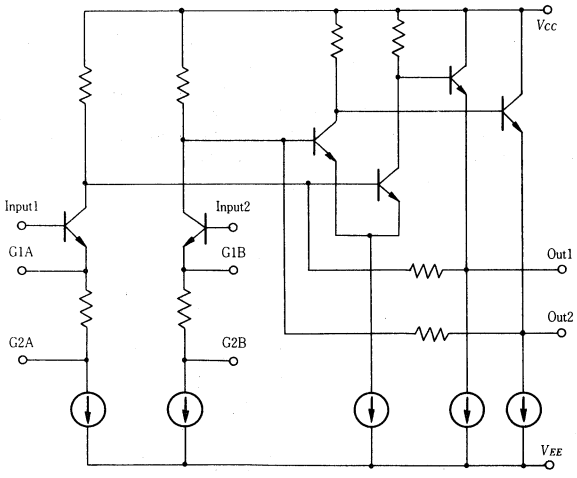


(DP-14)

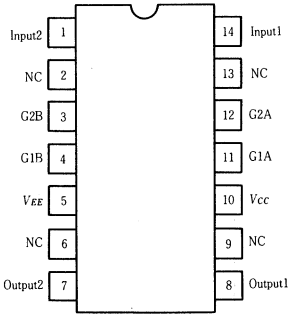
■FEATURES

- Wide Band Width 90MHz
- Good Response.
- Gain is Easily Adjusted in the Range from 0 to 400.
- No External Phase Compensation.

■CIRCUIT SCHEMATIC (1/4)



■PIN ARRANGEMENT



(Top View)

HITACHI

■ABSOLUTE MAXIMUM RATINGS (T_a=25°C)

Item	Symbol	HA17592G	HA17592P	HA17592	Unit
Supply Voltage	V_{CC}	+8	+8	+8	V
	V_{EE}	−8	−8	−8	V
Common Mode Input Voltage	$V_{in(CM)}$	±6	±6	±6	V
Differential Input Voltage	$V_{in(diff)}$	±5	±5	±5	V
Output Current	I_{out}	10	10	10	mA
Power Dissipation	P_T	625*1	625*2	625*2	mW
Operating Temperature	T_{opr}	−20 to +75	−20 to +75	0 to +70	°C
Storage Temperature	T_{stg}	−65 to +150	−55 to +125	−55 to +125	°C

*1 When T_a is 70°C or more. The derating curve will be 7.6mW /°C
*2 When T_a is 50°C or more. The derating curve will be 8.3mW/°C

■ELECTRICAL CHARACTERISTICS (V_{CC} = − V_{EE}=6.0V, T_a=25°C)

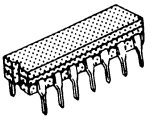
Item		Symbol	Test Condition		min	typ	max	Unit
Operating Supply Voltage Range		V_{CC}	Note 1		3	−	8	V
		V_{EE}			−3	−	−8	
Differential Voltage Gain	Gain 1	A_{VD}	Note 2		250	400	600	
	Gain 2		Note 3		80	100	120	
Bandwidth	Gain 1	BW	R_S=50Ω		−	40	−	MHz
	Gain 2				−	90	−	
Rise Time	Gain 1	t_r	R_S=50Ω,		−	10.5	−	ns
	Gain 2		V_{out}=1Vp-p		−	4.5	12	
Propagation Delay Time	Gain 1	t_p	R_S=50Ω,		−	7.5	−	ns
	Gain 2		V_{out}=1Vp-p		−	6.0	10	
Input Resistance	Gain 1	R_{in}			−	4.0	−	kΩ
	Gain 2				10	30	−	
Input Capacitance	Gain 2	C_{in}			−	2.0	−	pF
Input Offset Current		I_{IO}			−	0.4	5.0	μA
Input Bias Current		I_I			−	9.0	30	μA
Input Noise Voltage		$V_{n(in)}$	R_S=50Ω, BW=1kHz to 10MHz		−	12	−	μVrms
Input Voltage Range		V_I			±1.0	−	−	V
Common Mode Rejection Ratio	Gain 2	CMR	V_{CM}=±1V	f=100kHz	60	86	−	dB
				f=5MHz	−	60	−	
Power Supply Rejection Ratio	Gain 2	$PSRR$	ΔV_{CC}=±0.5V, ΔV_{EE}=±0.5V		50	70	−	dB
Input Offset Voltage	Gain 2	V_{OO}			−	0.2	0.75	V
Output Common Mode Voltage		V_{OCM}	R_L=∞		2.4	2.9	3.4	V
Peak to Peak Output Voltage		V_{OP-P}			3.0	4.0	−	Vp-p
Output Sink Current		I_{sink}			2.5	3.6	−	mA
Output Resistance		R_{out}			−	20	−	Ω
Supply Current		I_{CC}			−	18	24	mA

Notes) 1. In this range, the amplifier can be operating.
2. Connect G_{1A} with G_{1B}.
3. Connect G_{2A} with G_{1B}.

HA17733 Series ●Differential Video Amplifier

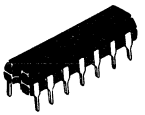
HA17733 is a video amplifier for wide band with small phase-delay and excellent gain stability. This amplifier eliminates external phase compensation and can fix the gain 10, 100 or 400 without using external elements. If some external elements are used, any gain from 10 to 400 is available.
It finds main application in terminal units of computers, interface or video amplifiers.
Industrial Use: HA17733G, HA17733P
Commercial Use: HA17733

HA17733G



(DG-14)

HA17733P, HA17733

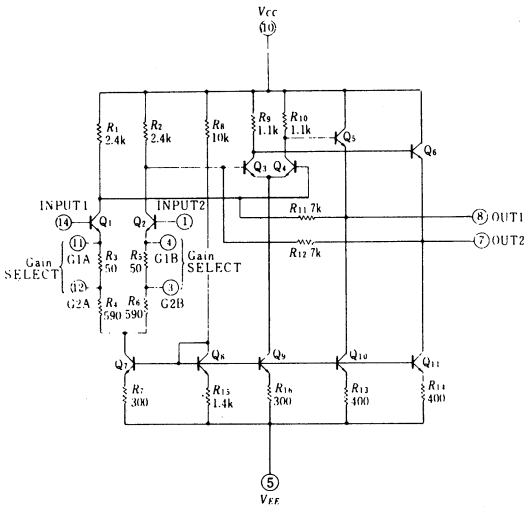


(DP-14)

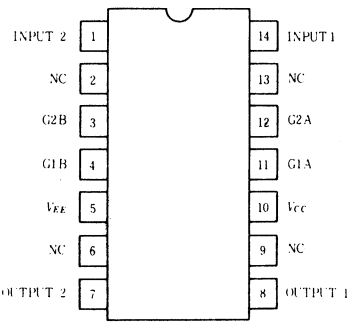
■ FEATURES

- Wide Band Width 120MHz
- Good Response
- Gain is Easily Adjusted in the Range of 10 to 400
- Eliminates External Phase Compensation

■ CIRCUIT SCHEMATIC



■ PIN ARRANGEMENT



(Top View)

■ ABSOLUTE MAXIMUM RATINGS (Ta=25℃)

Item	Symbol	HA17733G	HA17733P	HA17733	Unit
Supply Voltage	V_{CC}	+8	+8	+8	V
	V_{EE}	−8	−8	−8	V
Common Mode Input Voltage	$V_{in(CM)}$	±6	±6	±6	V
Differential Input Voltage	$V_{in(diff)}$	±5	±5	±5	V
Output Current	I_{out}	10	10	10	mA
Power Dissipation	P_T	625 *1	625 *2	625 *2	mW
Operating Temperature	T_{opr}	−20 to +75	−20 to +75	0 to +70	℃
Storage Temperature	T_{stg}	−65 to +150	−65 to +150	−55 to +125	℃

*1 When Ta is 70℃ or more, the derating curve will be 7.6mW/℃.
*2 When Ta is 50℃ or more, the derating curve will be 8.3mW/℃.

■ ELECTRICAL CHARACTERISTICS-1 ($V_{CC}=-V_{EE}=6.0V$, $Ta=25℃$)

Item		Symbol	Test Conditions		min	typ	max	Unit
Operating Supply Voltage Range		V_{CC}	Note 1		3	—	8	V
		V_{EE}			−3	—	−8	V
Differential Voltage Gain	Gain 1	A_{VD}	Note 2		250	400	600	
	Gain 2		Note 3		80	100	120	
	Gain 3		Note 4		8	10	12	
Bandwidth	Gain 1	BW	$R_s=50\ \Omega$		—	40	—	MHz
	Gain 2				—	90	—	
	Gain 3				—	120	—	
Rise Time	Gain 1	t_r	$R_s=50\ \Omega$, $V_{out}=1V_{p-p}$		—	10.5	—	ns
	Gain 2				—	4.5	12	
	Gain 3				—	2.5	—	
Propagation Delay Time	Gain 1	t_p	$R_s=50\ \Omega$, $V_{out}=1V_{p-p}$		—	7.5	—	ns
	Gain 2				—	6.0	10	
	Gain 3				—	3.6	—	
Input Resistance	Gain 1	R_{in}			—	4.0	—	kΩ
	Gain 2				10	30	—	
	Gain 3				—	250	—	
Input Capacitance	Gain 2	C_{in}			—	2.0	—	pF
Input Offset Current		I_{IO}			—	0.4	5.0	μA
Input Bias Current		I_I			—	9.0	30	μA
Input Noise Voltage		$V_{n(in)}$	$R_s=50\ \Omega$, $BW=1kHz$ to $10MHz$		—	12	—	μVrms
Input Voltage Range		V_I			±1.0	—	—	V
Common Mode Rejection Ratio	Gain 2	CMR	$V_{CM}=\pm1V$	$f=100kHz$	60	86	—	dB
				$f=5MHz$	—	60	—	
Power Supply Rejection Ratio	Gain 2	$PSRR$	$\Delta V_{CC}=\pm0.5V$, $\Delta V_{EE}=\pm0.5V$		50	70	—	dB
Input Offset Voltage	Gain 1	$V_{n(off)}$			—	0.6	1.5	V
	Gain 2,3				—	0.35	1.5	
Output Common Mode Voltage		$V_{n(CM)}$			2.4	2.9	3.4	V
Peak to Peak Output Voltage		V_{op-p}			3.0	4.0	—	Vp-p
Output Sink Current		I_{sink}			2.5	3.6	—	mA
Output Resistance		R_{out}			—	20	—	Ω
Supply Current		I_{CC}			—	18	24	mA

■ ELECTRICAL CHARACTERISTICS-2 ($V_{CC}=-V_{EE}=6.0V$, $Ta=0$ to $+70°C$)

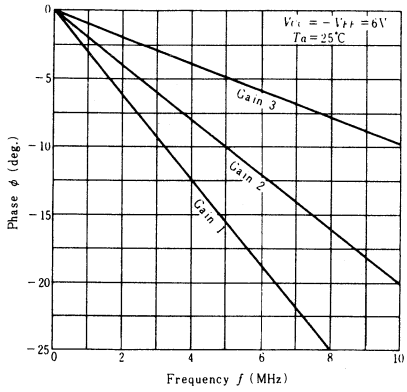
Item		Symbol	Test Conditions	min	typ	max	Unit
Differential Voltage Gain	Gain 1	A_{VD}	Note 2	250	–	600	
	Gain 2		Note 3	80	–	120	
	Gain 3		Note 4	8	–	12	
Input Offset Current		I_{IO}		–	–	6.0	μA
Input Bias Current		I_I		–	–	40	μA
Input Voltage Range		V_I		±1.0	–	–	V
Common Mode Rejection Ratio	Gain 2	CMR	$V_{CM}=\pm1V$, $f\leqq100kHz$	50	–	–	dB
Power Supply Rejection Ratio	Gain 2	$PSRR$	$\Delta V_{CC}=\pm0.5V$, $\Delta V_{EE}=\pm0.5V$	50	–	–	dB
Input Offset Voltage	All Gain	$V_{O(off)}$		–	–	1.5	V
Peak to Peak Output Voltage		V_{op-p}		2.8	–	–	Vp-p
Output Sink Current		I_{sink}		2.5	–	–	mA
Supply Current		I_{CC}		–	–	27	mA
Input Resistance	Gain 2	R_{in}		8.0	–	–	Ω

■ ELECTRICAL CHARACTERISTICS-3 ($V_{CC}=-V_{EE}=6.0V$, $Ta=-20$ to $+75°C$)

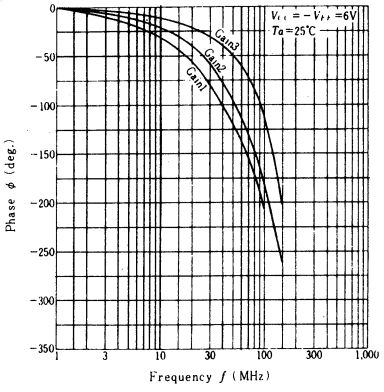
Item		Symbol	Test Conditions	min	typ	max	Unit
Differential Voltage Gain	Gain 1	A_{VD}	Note 2	200	–	700	
	Gain 2		Note 3	70	–	130	
	Gain 3		Note 4	7	–	13	
Input Offset Current		I_{IO}		–	–	7	μA
Input Bias Current		I_I		–	–	50	μA
Input Voltage Range		V_I		±1.0	–	–	V
Common Mode Rejection Ratio	Gain 2	CMR	$V_{CM}=\pm1V$, $f\leqq100kHz$	46	–	–	dB
Power Supply Rejection Ratio	Gain 2	$PSRR$	$\Delta V_{CC}=\pm0.5V$, $\Delta V_{EE}=\pm0.5V$	46	–	–	dB
Output Offset Voltage	All Gain	$V_{O(off)}$		–	–	1.5	V
Peak to Peak Output Voltage		V_{op-p}		2.8	–	–	Vp-p
Output Sink Current		I_{sink}		2.5	–	–	mA
Supply Current		I_{CC}		–	–	29	mA
Input Resistance	Gain 2	R_{in}		7.0	–	–	kΩ

Note) 1. In this range, the apmlifier can be operating.
2. Connect G_{1A} and G_{1B}.
3. Connect G_{2A} and G_{2B}.
4. Open all of the terminals for gain select.

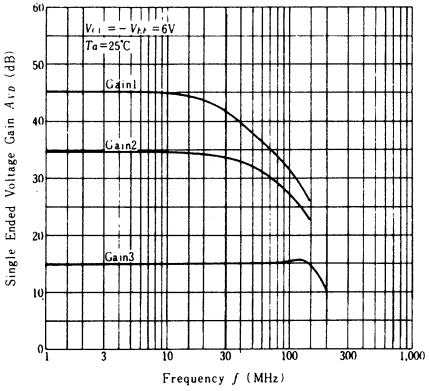
PHASE VS. FREQUENCY (1)



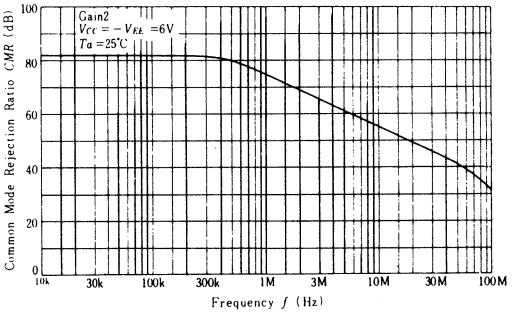
PHASE VS. FREQUENCY (2)



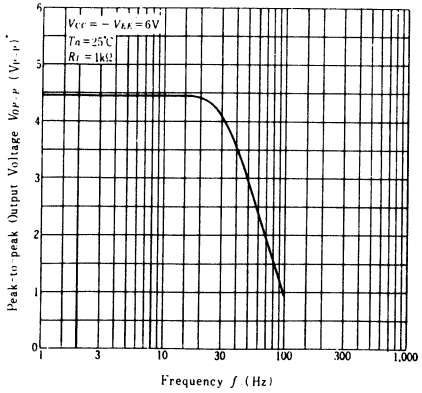
SINGLE ENDED VOLTAGE GAIN VS. FREQUENCY



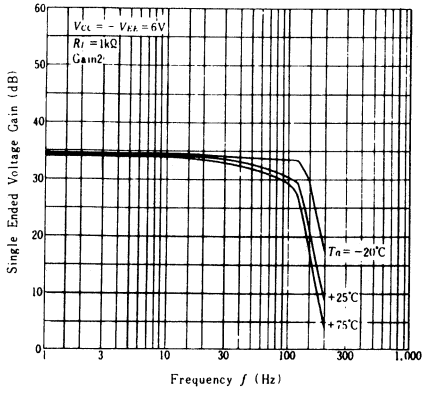
COMMON MODE REJECTION RATIO VS. FREQUENCY



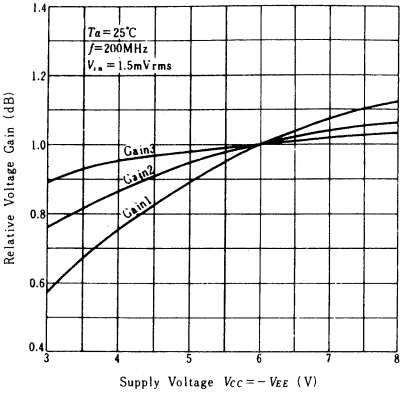
PEAK-TO-PEAK OUTPUT VOLTAGE VS. FREQUENCY



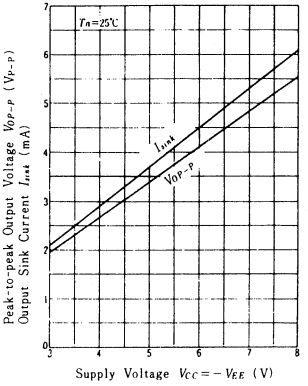
SINGLE ENDED VOLTAGE GAIN VS. FREQUENCY



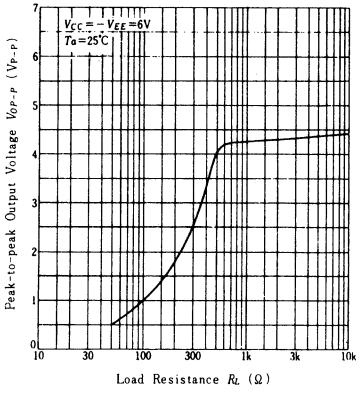
RELATIVE VOLTAGE GAIN VS. SUPPLY VOLTAGE



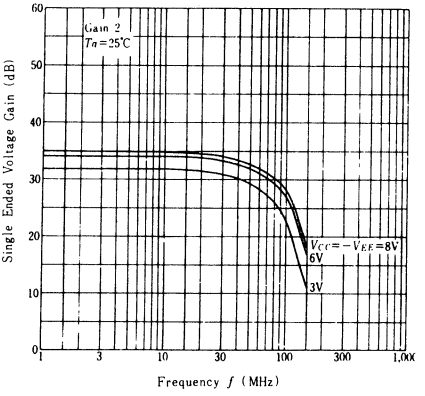
PEAK-TO-PEAK OUTPUT VOLTAGE, OUTPUT SINK CURRENT VS. SUPPLY VOLTAGE



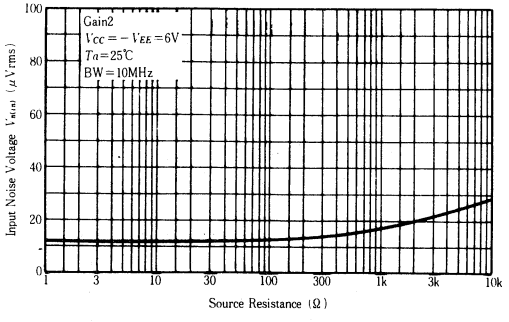
PEAK-TO-PEAK OUTPUT VOLTAGE VS. LOAD RESISTANCE



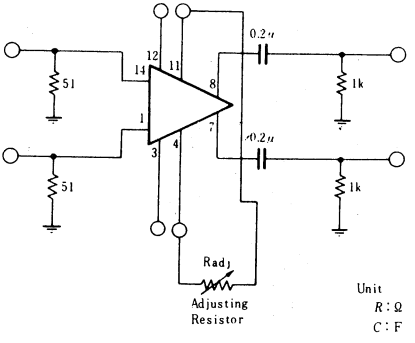
SINGLE ENDED VOLTAGE GAIN VS. FREQUENCY



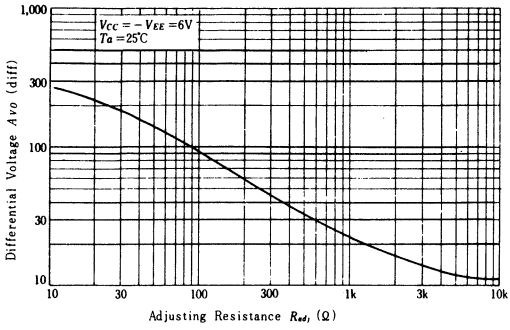
INPUT NOISE VOLTAGE VS. SOURCE RESISTANCE



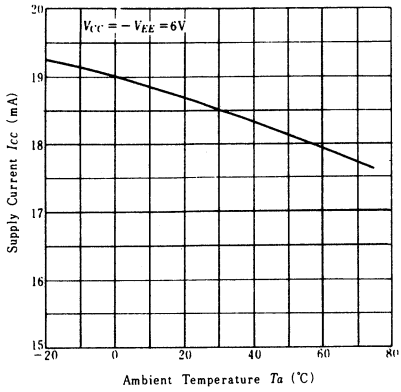
DIFFERENTIAL VOLTAGE GAIN ADJUSTING CIRCUIT



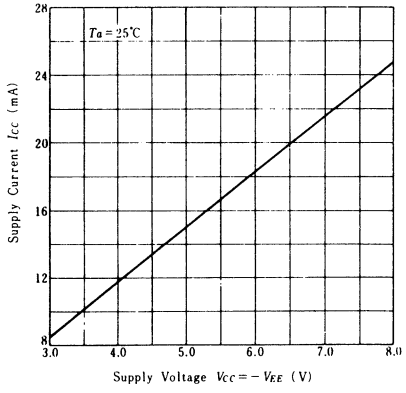
DIFFERENTIAL VOLTAGE GAIN VS. ADJUSTING RESISTANCE



SUPPLY CURRENT VS. AMBIENT TEMPERATURE



SUPPLY CURRENT VS. SUPPLY VOLTAGE



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HITACHI

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